Graz University of Technology

Master Thesis

Performance characteristics & evaluation of an Analog-to-Digital Converter for RF applications

conducted at the
Signal Processing and Speech Communications Laboratory
Graz University of Technology, Austria

in co-operation with
Infineon Technologies AG
DC Graz
Sense & Control

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Graz, 25.10.2012

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

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Abstract

A sigma-delta analog-to-digital converter (SD-ADC) has been implemented for a linear radio receiver architecture. The SD-ADC is evaluated and characterised in this thesis. Performance measures are defined to characterise the ADC in wireless communications applications. According to those measures, the implemented SD-ADC has been evaluated and a comparison with specifications has been accomplished. Harmonic and intermodulation distortion specifications are not met by the designed SD-ADC. All other specification parameters have been achieved by the implemented SD-ADC design. Furthermore, a behavioural model has been derived for the integrated SD-ADC from measurement data, taking linear and non-linear behaviour into account. A comparison is presented as a conclusion between measurement results and simulation results for the model. The model is capable of representing the small scale behaviour of the SD-ADC. For large-scale input the simulation output is too optimistic compared to measurement results.

Kurzfassung

In einem linearen Hochfrequenzempfänger wurde ein Sigma-Delta Analog-Digital-Umsetzer implementiert, der in dieser Diplomarbeit vermessen und charakterisiert wurde. Zu diesem Zwecke wurden die wichtigsten Messparameter eines ADC für drahtlose Übertragungssysteme definiert. Der implementiere SD-ADC wurde anhand der definierten Parameter evaluiert und charakterisiert und ein Vergleich zu den spezifizierten Eigenschaften wurde erbracht. Intermodulationsprodukte und harmonische Oberwellen liegen über den spezifizierten Werten. Alle anderen Spezifikationswerte werden vom implementierten SD-ADC Design erreicht. Weiters wurde das lineare und nichtlineare Verhalten des integrierten SD-ADC anhand der erzielten Messwerte in einem Modell abgebildet. Als Abschluss wurde eine Gegenüberstellung der gemessenen Ergebnisse und der simulierten Resultate des Modells erbracht. Das Model bildet das Verhalten des implementierten SD-ADCs für kleine Eingangssignale gut nach. Für Signale nahe an den Grenzen des SD-ADC Eingangsbereiches, wird das Ergebnis der Simulation zu optimistisch im Vergleich zu den Messresultaten.

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To my parents, family and friends for all the kind support during my studies.

Contents

Nomenclature

f_{clock}	Clock frequency
f_{signal}	Signal frequency
ADC	Analog-to-Digital Converter
BPF	Bandpass Filter
CT-SD-ADC	Continuous-Time Sigma-Delta analog-to-digital converter
DAC	Digital-to-Analog Converter
dBc	decibel to carrier
dBfs	decibel to full scale
dBV	decibel to Volt
DC	Direct Current
DFT	Discrete Fourier Transformation
DR	Dynamic Range [dB]
DSP	Digital Signal Processor
DSSS	Direct Sequence Spread Spectrum
DUT	Device Under Test
ENOB	Effective Number of Bits [Bit]
EV	Electrical Vehicle
FFT	Fast Fourier Transformation
FS	Full scale
GPIB	General purpose interface bus
I/O	Input/Output
I_{ADC}	ADC supply current
IF	Intermediate Frequency
IIP2	2^{nd} order Input Intercept Point
IIP3	3^{rd} order Input Intercept Point
ISM	Industry Scientific Medical

LNA Low-Noise Amplifier

NAD Noise and Distortion

NTF Noise Transfer Function

OPAMP Operational Amplifier

PA Power Amplifier

PC Personal Computer

RC-Tuning Resistor-Capacitor Tuning

RKE remote-keyless entry

rms root-mean-square

RSP Receive Signal Processor

SFDR Spurious-Free-Dynamic Range [dBc]

SIB System Interface Board

SNDR Signal-to-Noise-and-Distortion Ratio [dB]

SNR Signal-to-Noise Ratio [dB]

STF Signal Transfer Function

TC Testchip

THD Total harmonic distortion [dBc]

TPMS Tire Pressure Monitoring System

TSP Transmit Signal Processor

V_{ADC} ADC supply voltage

V_{CM} common mode voltage

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1 Introduction

1.1 POLLUX Project

The objective of POLLUX (*Process Oriented eLectronic controL Units for Vehicles Developed on a Multi-System Real-Time Embedded Platform*) is to develop a distributed real time embedded systems platform for next generation electric vehicles, by using a component and programming-based design methodology. Reference designs and embedded systems architectures for high efficiency innovative mechatronics systems will be addressed with regard to requirements on composability, networking, security, robustness, diagnosis, maintenance, integrated resource management, evolvability, and self-organisation.
Next generation EVs will endeavour the convergence between computer and automotive architectures: future automobiles will be mechatronic systems comprising a multitude of plug-and-play and self configurable peripherals. Peripherals will be embedded systems containing hardware, algorithms and software. The architecture will be based on distributed energy while the propulsion systems will adopt radical new control concepts. Sensing, actuation, signal processing and computing devices will be embedded in the electronic equipment, electrical motors, batteries, and also in the mechanical parts.
The systems used to control the chassis and the power train will form the „computing engine“ that automates lower level tasks during vehicle use (driver assistance, terrain evaluation, predictive battery management) and will enable future higher level functionalities (auto pilot), by means of novel human-machine interfaces.
Development of design tools and associated runtime support to enable composability, predictability, parallelisation, aggregation and management of systems according to a service driven or data-centric approach. Furthermore this shall also support performance and energy modelling and analysis, verification and scalability in electrical vehicle design, while preserving systemlevel predictability and appropriate levels of safety.
Pollux addresses the embedded system needs for the next generation electric vehicles by exploiting the synergy with the ENIAC E3Car project, which aims to develop nanoelectronics technologies, devices, circuits, and modules for EVs in preparation for the launch of a massive European EV market by 2015-2020.

The POLLUX project addresses the industrial priority area of reference designs and architectures in order to offer common architectural approaches (standardised and interoperable) for

future electrical vehicles.
This general project definition and description is taken from [4] to give an overview on the POLLUX objectives. The goal of Infineon Technologies Austria AG within this project was to define a wireless interface to the electrical control unit. This interface should account for

- Convenience: Remote Keyless Entry, Passive Entry
- Diagnostics: Maintenance
- Non-mission critical sensors connected in a mesh network
- Smart Grid / Vehicle-to-grid communication

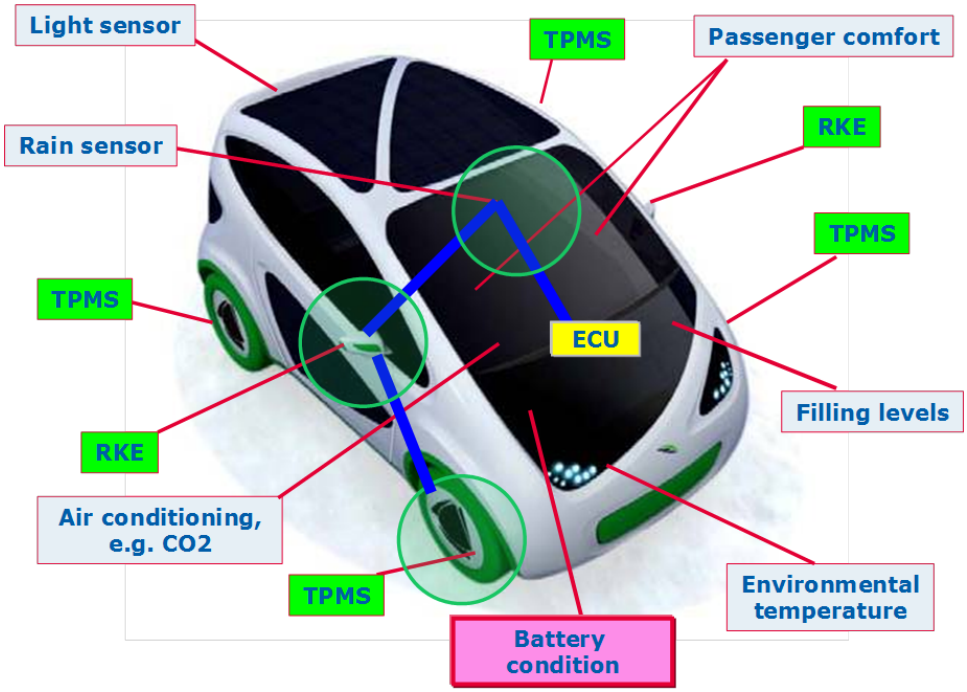


Figure 1.1: Electrical Vehicle

Fig. 1.1 is presenting an abstract view of the components, which should interact on a wireless basis with the electrical control unit and electrical vehicle. There are several challenges with respect to wireless communication between a now common car and an electrical vehicle in the future. The two main aspects are

- Large current surges in cables
- Large magnetic fields near in-wheel/hub electronic motors

To overcome these challenges, there have been two different strategies proposed: on the one hand the common used technique of shielding, and on the other hand an adaptation and extension of the wireless physical layer, e.g. introduce redundancy and use spread spectrum techniques. To implement this adaptation and extension of the wireless physical layer a linear receiver architecture has been implemented, utilising a recently developed Sigma-Delta Analog-to-Digital Converter (SD-ADC). A short introduction to low-IF (intermediate frequency) linear receiver architecture is presented in the next Section 1.2.

1.2 An ADC in a linear low-IF sampling architecture

As an alternative receiver structure to the commonly known heterodyne receiver with baseband A/D conversion, the linear low-IF sampling receiver architecture has become more popular in the last decade. In a heterodyne receiver with IF digitizing, the ADC is shifted towards the receive antenna and is digitising the received signal at a moderate intermediate frequency. This inherits linearity in the receiver chain and a wideband sampling of the received spectrum, such that channel filtering, tuning and separation can be performed by a high speed digital signal processor in the digital part of the receiver. By sampling the received spectrum at an intermediate frequency, several stages of down conversion can be omitted. More flexible and lower-cost solutions are possible. The ADC performance requirements are defined by particular air standards. As it is discussed in further chapters, high linearity measures, dynamic range and speed requirements have to be applied to an ADC in such a receiver architecture. In Fig. 1.2 low-IF sampling receiver architecture with only one mixer is shown. As mentioned in the Figure caption, this receiver structure is often used in software defined radio (SDR) applications.[1, 5]

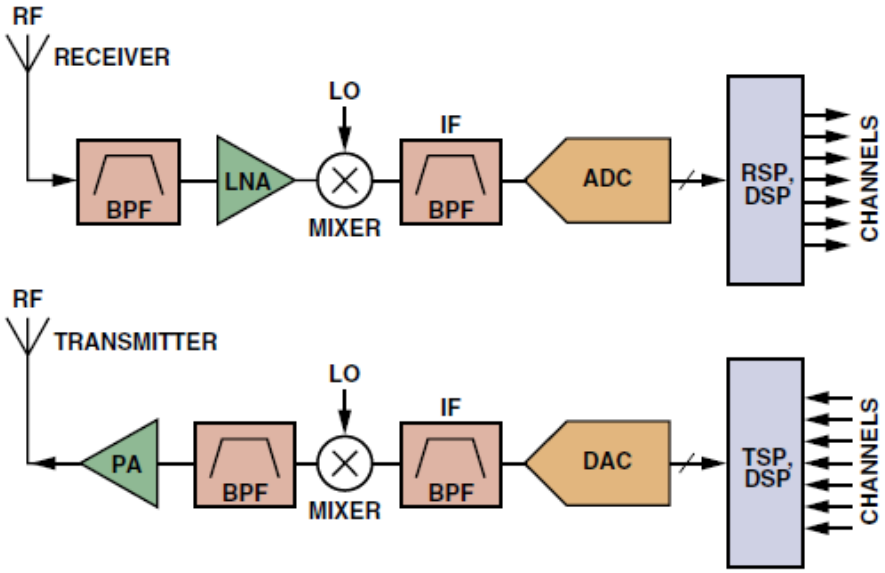


Figure 1.2: Generic IF-sampling wideband software radio transceiver [1]

In the POLLUX transceiver testchip a linear architecture is chosen, in order to benefit from

- higher sensitivity
- receive channels in parallel
  - higher link reliability
  - lower system current consumption
- digital bandpass filtering
  - lower production spread
- less area consumption
  - lower cost

Therefore the POLLUX transceiver can fulfil the requirements for automotive electronic devices in future electrical vehicles.

1.3 Structure of this work

In Chapter 2 (*POLLUX Sigma-Delta ADC*) the architecture of the integrated SD-ADC is described and some definitions and details regarding the implementation are given.
In Chapter 3 (*Measurement Environment*) a measurement setup and tooling, which was used to measure the performance characteristics of the given SD-ADC is presented.
In Chapter 4 (*ADC characterisation*) an integrated Sigma-Delta Analog-to-Digital Converter (SD-ADC) is characterised. In Section 4.1 (*Characterisation Measurements*) the characterisation measurement results are presented and in Section 4.2 (*Discussion and Conclusion*) the obtained results are compared with the specification.
In Chapter 5 (*ADC modelling*) a behavioural ADC model is derived. In Section 5.1 (*Linear Model*) a linear behavioural SD-ADC model is developed by given design parameters of the underlying integrated SD-ADC. In Section 5.2 (*Non-linear Model*) a non-linear behaviour model is developed by adding a weak non-linearity to the linear model, parametrised by results of Chapter 4. In Section 5.3 (*Model vs. Measurement*) the SD-ADC output obtained by measurement and the SD-ADC model output obtained by different model parameters are compared against each other by means of calculated performance measures.

In Chapter 6 the results of this work are summarised and some outlook for future work, regarding ADC characterisation and performance measurement is presented.

1.4 Goal of this work

The goal of this thesis is to characterise the integrated SD-ADC described in Chapter 2 and derive a good-fit behavioural model to describe the SD-ADC implemented in the POLLUX transceiver. This is done in Chapter 4 and Chapter 5

2 POLLUX Sigma-Delta ADC

2.1 Sigma-Delta ADC architecture

In the POLLUX transceiver testchip an integrated CT-SD-ADC is implemented to perform direct IF conversion. SD-ADC architecture provides several advantages such as:

- High dynamic range
  - low noise floor because of noise shaping capability
  - high ENOB / resolution
- Discrete and continuous time implementation possible
  - CT implementation: low power consumption
- High oversampling ratio
  - Simple Anti-Aliasing Filter possible
  - Saving power + area
  - Digital post filtering

The POLLUX transceiver testchip is designed as a wireless communication device working in the ISM band. It should be capable of handling very large signals and interferes. At the same time high sensitivity should be maintained to be able to detect small signals. It is intended to operate on battery powered devices such as wireless sensor nodes. Additional application areas can be found in the automotive and multimedia sector. Taking into account the list of advantages given above, an CT-SD-ADC seems to be perfectly suitable for a wireless communication device such as the POLLUX transceiver testchip.

2.2 POLLUX ADC specification

In the POLLUX receiver chain, the IF is chosen to be at 500kHz. The SD-ADC should have high dynamic range in a narrow band mode and a reduced dynamic range is allowed in a wider

band mode. Fig. 2.1 gives a schematic overview of these two specified modes. For classic remote-keyless entry (RKE) applications a frequency band of 500kHz is desired. In order to be more robust in interferer scenarios a direct sequence spread spectrum technique (DSSS) as briefly mentioned in Chapter 1 is specified. This DSSS is planned to occupy 1.2MHz of bandwidth. Fig. 2.1 schematically shows the relation of bandwidth and dynamic range for both , classic RKE and DSSS.

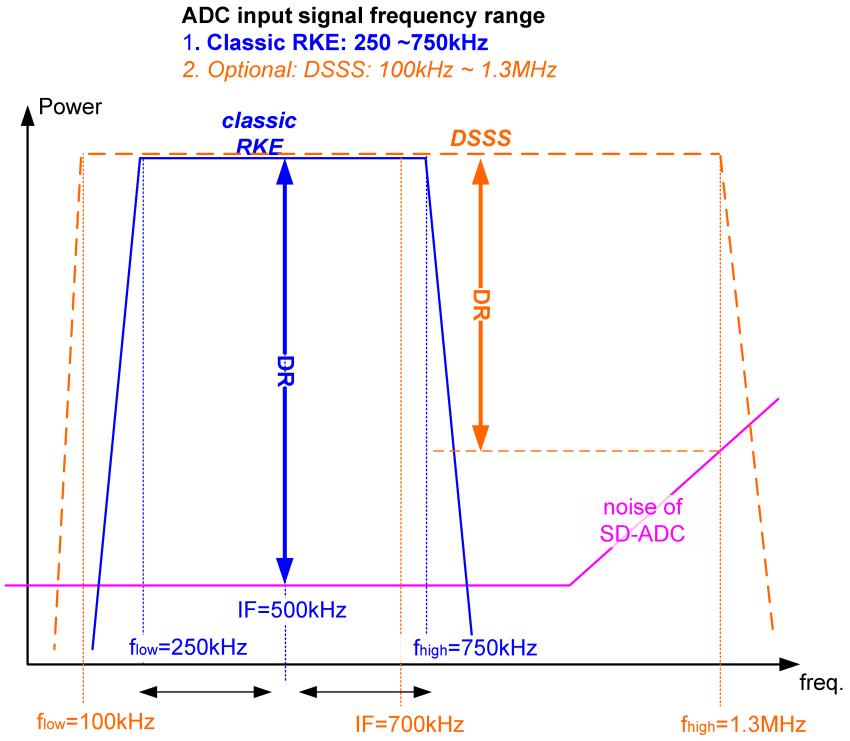


Figure 2.1: Schematic drawing depicting dynamic range vs. frequency

Tab. 2.1 gives a short summary of the specified operation conditions for the SD-ADC:

I_{ADC}	$\leq$ 3 mA
V_{ADC}	1.4 ... 1.6 V
$FS_{\text{differential input}}$	2 V
V_{CM}	700 mV
Temperature Range	-40 °C... 135 °C

Table 2.1: Operating conditions

In Tab. 2.2 a summary of dynamic specifications for the desired SD-ADC is presented.

f_{signal}	250 - 750kHz	high performance
f_{signal}	100 - 1300kHz	reduced performance
f_{clock}	50MHz	
DR	84 dB	at 10kHz Bandwidth
SNDR	66 dB	at 300kHz Bandwidth
2^{nd}Harmonic	<60 dB	
Input	Intermodulation Distortion	
at -12 dBfs	<-62 dBfs	at 250kHz
at -9 dBfs	<-59 dBfs	at 400kHz

Table 2.2: POLLUX SD-ADC Specifications

A continuous time 4^{th}-order feedback structure (see Fig. 2.2) with one resonator has been chosen for the ADC filter.

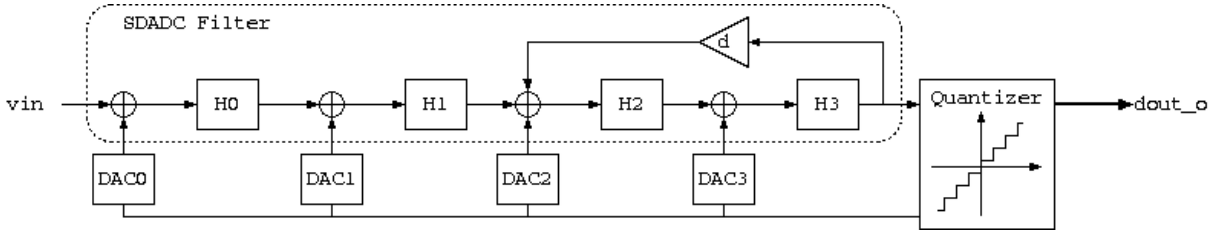


Figure 2.2: POLLUX Architecture

According to [6] the signal transfer function (STF) and the shaped noise transfer function (NTF) can be calculated with following expressions:

$$STF(s) = \frac{g\,H_3(s)\,H_2(s)\,H_1(s)\,H_0(s)}{\{[(H_0(s)+1)\;g\,H_1(s)+g]\;H_2(s)+g\}\;H_3(s)\,G_{dac}+1+H_2(s)\,d\,H_3(s)} \tag{2.1}$$

$$NTF(s) = \frac{1+H_2(s)\,d\,H_3(s)}{\{\{[(H_0(s)+1)\;g\,H_1(s)+g]\;H_2(s)+g\}\;H_3(s)\,G_{dac}+1+H_2(s)\,d\,H_3(s)\}\;k} \tag{2.2}$$

g is a modelling parameter for the quantizer gain.
k is the number of quantizer levels. (e.g. $k = 16$).
The blocks H_0 to H_3 are integrators described by (2.3). The RC-values are selected according to the desired bandwidth.

$$H_x(s) = \frac{1}{R_x \cdot C_x \cdot s} \tag{2.3}$$

Every integrator stage has a programmable RC product (C-tuning possible) in order to perform fine tuning of the filter poles.
A resonator is used to achieve better inband noise shaping. The operational amplifiers (OPAMP) are Miller compensated OPAMP's. Their gain and bandwidth depends on the filter poles position. The noise of the first OPAMP and of the first DAC is not shaped, therefore they are the major noise contributors in the design, together with the input resistor. A poor jitter performance can also add noise to the output value.

The used quantizer is an improved 4-bit tracking quantizer. The implemented quantizer has an equivalent resolution of a 4-bit flash converter. 0000_2 is the minimum value achieved when the most negative differential voltage is applied at the input. 1111_2 is the maximum value achieved when the most positive differential voltage is applied at the input. For the differential input signal a common mode voltage of 700mV is selected.

3 Measurement Environment

3.1 Hardware Tools

In this Section the measurement setup used for evaluation of the performance of the integrated SD-ADC is introduced. A printed circuit board (PCB) was designed and manufactured for evaluation of the POLLUX Testchip. The POLLUX TC has been designed and produced by Infineon Technologies Austria. In Fig. 3.1 the entire measurement setup is displayed schematically.

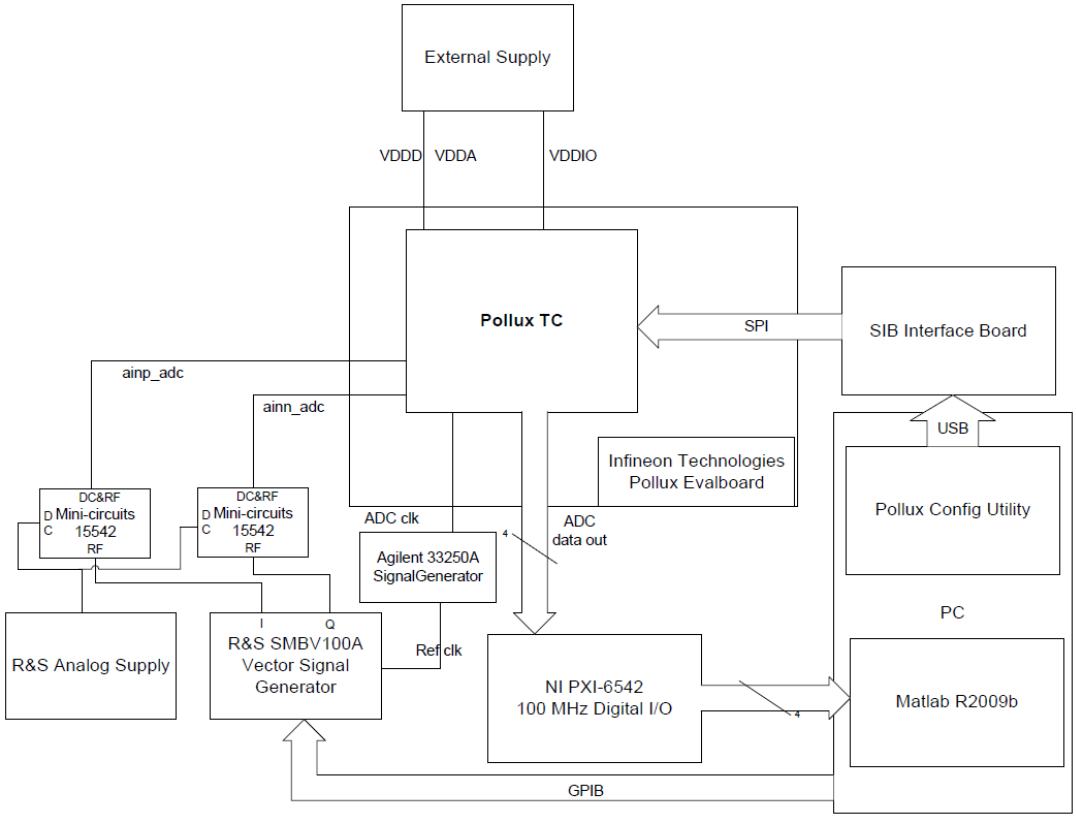


Figure 3.1: Measurement Setup schematic overview

Input signal generation

As a signal generator a *Rhode & Schwarz SMBV100A Vector Signal Generator* is used. Its baseband signal generator unit is utilised to generate a differential signal used as an input to the SD-ADC. The input pins to the integrated SD-ADC are available at the POLLUX Testchip. To add a common mode voltage to the input signal DC & RF coupling *minicircuits* are utilised. The common mode voltage of approx. 700mV is generated by an analog supply. It is important to have an analog supply to get a clean input signal. Fig. 3.2 schematically shows the input signal generation section of the measurement setup.

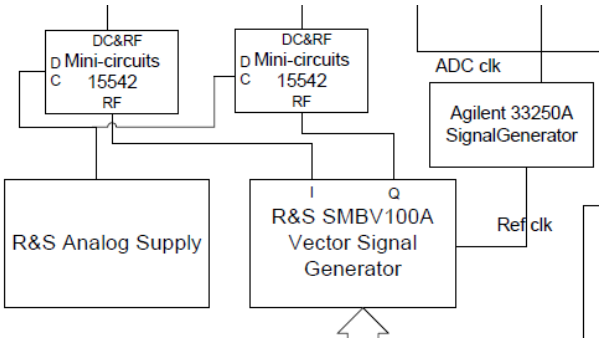


Figure 3.2: A close-up on the input signal generation setup and sample clock generation

Sample clock generation

The 50 MHz SD-ADC clock is generated externally by an *Agilent Arbitrary Waveform generator*. This ADC clock generator is connected by a 10 MHz reference clock to the input-signal signalgenerator to ensure coherent signal generation and sampling.

Supply voltage generation

For evaluation purposes the analog, digital and input/output blocks of the POLLUX Testchip are supplied externally. Only the reference voltage of 1.5 V for the SD-ADC is generated on-chip.

Pin Connections

As mentioned above the input pins of the integrated SD-ADC have been made available as testpins for evaluation purposes. Also a 4 bit digital output is available. The 4 bit digital output introduces some trouble mainly caused by a raise of the noise floor. This phenomena is especially relevant when doing evaluation measurements of the POLLUX Testchip with the integrated analog-frontend, since in this case the noise is amplified by the LNA. Therefore the evaluation of the integrated SD-ADC has been done without the integrated analog-frontend. Only block level testing of the integrated SD-ADC is done.

Data sampling and post processing

The 4 bit digital output is sampled by a *National Instruments PXI-6542 100 MHz Digital I/O device*. The digital I/O device is connected by a fast serial connection to a personal computer. At the PC data post processing is done by Matlab R2009b (Version 7.9).

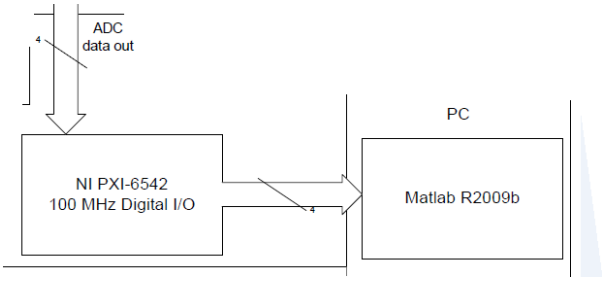


Figure 3.3: ADC output data sampling and post processing

Configuration of the DUT

Configuration of all signal and clock generation units is done by Matlab over GPIB (IEEE-488). Configuration of the POLLUX TC registers is done by an application running at the PC. This application is utilising a System Interface Board (SIB) designed by Infineon Technologies Austria. Communication between the SIB and the POLLUX TC is done by Serial Peripheral Interface (SPI) Bus. Fig. 3.4 is presenting the configuration flow schematically.

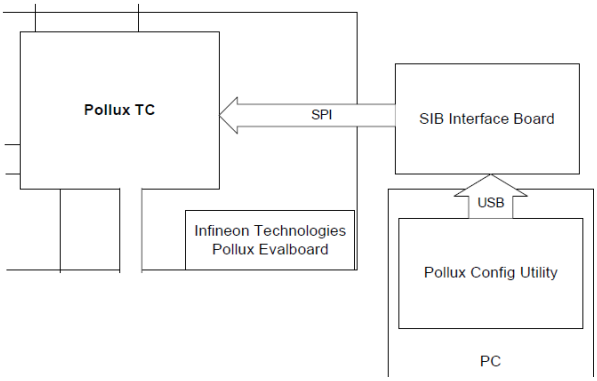


Figure 3.4: ADC configuration flow

In frequency domain analysis it is important to ensure coherent sampling. This is done by the measurement setup: both, by the hardware setup described in this section, and by the software setup described in the following Section 3.2.

3.2 Software Tools

Testbench

A universal ADC testbench has been developed in Matlab in a previous project. This testbench has been adapted to the newly developed SD-ADC and some missing characterisation tests have been added. All configuration steps of signal and clock generation units are done by the testbench. As mentioned in Section 3.1 the National Instruments Digital I/O device is configured to sample in the 4 bit SD-ADC output data, and Matlab (i.e. the developed testbench) is used as a data post processing tool.
The testbench is set up to be very flexible, based on an object oriented approach in Matlab: Signal generation, data sampling and data evaluation are separated in different class definitions and sub-functions. By means of a fast fourier transformation frequency domain evaluation and

parameter extraction is performed on sampled output data. Several different test-cases are defined and included in this testbench. Matlab is used in Version 7.9 (R2009b).

Configuration Tool

POLLUX TC registers are written and read by simple SPI bus communication. For the purpose of easier configuration a *Configuration Utility Tool* has been designed in an application development environment developed by Infineon Technologies Austria. A screen capture of the *Configuration Utility Tool* is shown in Figure Fig. 3.5. The Pollux Testchip is configured before each measurement run and held in reset after the measurement has been finished to ensure correct measurement results.

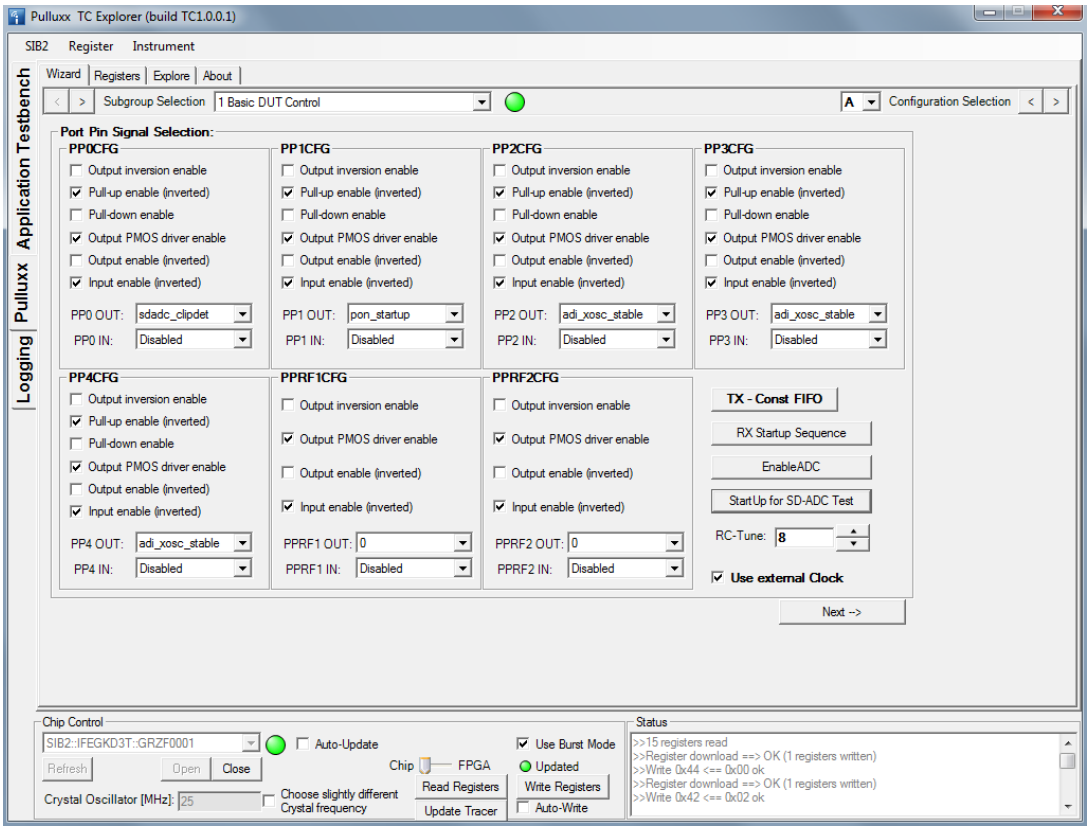


Figure 3.5: POLLUX Configuration Utility

4 ADC characterisation

4.1 Characterisation Measurements

In the following sections the performance of the integrated POLLUX TC SD-ADC is evaluated. The characterisation parameters for a SD-ADC under test are defined according to literature [7–10]. In most cases the definitions are very similar across literature. Therefore mainly [7] is taken as reference.
In each of the following sections a definition of the desired parameter is given. Then the characterisation measurement results are given structured into input level sweep and behaviour across frequency.
The integrated SD-ADC has been tested for linearity. A linearity statement for a device can be done according to the results of the two tone test. To ensure the linearity of the signalgenerator used to generate input signal to the device-under-test (DUT), a two-tone evaluation has been performed with a spectrum analyser. The results of the signalgenerator linearity test are presented at the beginning of Section 4.1.5.
For completeness an evaluation on power consumption and a Figure of Merit compared with implementations found in literature are presented in Section 4.1.6.

In Tab. 4.1 some general measurement parameters, which are in common for all measurements performed, are given.

VDDD	3.3 V
VDDA	3.3 V
VDDIO	3.3 V
VDD_{ADC}	1.5 V
VDD_{VCM}	710 mV
$f_{ADCclock}$	50 MHz

Table 4.1: Measurement parameters - same for all measurements

In Tab. 4.2 an overview of variable measurement conditions in different characterisation setups is given. As already mentioned in Chapter 2, the RC-tuning values are utilised to compensate for manufacturing tolerances in the integrators and OPAMP stages of the SD-ADC. A CT

implementation of an SD-ADC is very sensitive to mismatches in the integrator stages and therefore this tuning capabilities are very useful.

	input level sweep	frequency sweep
f_{input}	fixed at 500kHz	100 - 2500 kHz
input level	variable -120 to 9 dBV	fixed at 3 dBV
RC-Tune Value	fix at 8	varied 0,3,5,8,10,15

Table 4.2: Measurement parameters - variable according to characterisation setup

Coherent sampling and FFT computation [7]

ADC's are typically tested at several different frequencies. As mentioned earlier, it is important to ensure for coherent sampling in frequency domain testing. The recommended approach by [7] is to use a record of length M and a frequency f_i such that J uniformly distributed phases are sampled. This is accomplished by choosing f_i according to (4.1).

$$f_i = \frac{J}{M} f_s \tag{4.1}$$

J is an integer which is relatively prime to M
f_s is the sampling frequency
M is the record length

So there are exactly J cycles in a record of length M. M should be set to a power of two for ease of computation when using a FFT algorithm. This has also the advantage that any odd value for J meets the relatively prime condition.

For all the following characterisation measurements the same principle procedure is undertaken: A data set of $K = 10$ records with $M = 2^{19}$ points from the SD-ADC at sample frequency $f_s = 50$MHz is acquired. $x_k[n]$ represents the k^{th} record of sine-wave data for $k = 1, 2, \ldots, K$. For each $x_k[n]$ the DFT $X_K[m]$ is computed. m is defined as integer from 0 to $M - 1$. The K sets of data are used to compute an averaged magnitude spectrum of the DFT at each basis frequency f_m:

$$X_k[m] = DFT\{x_k[n]\} \tag{4.2}$$

$$X_{avm}[m] = \frac{1}{K} \sum_{k=1}^{K} |X_k[m]| \qquad m = 0, 1, 2, \ldots, M-1 \tag{4.3}$$

The averaged spectral magnitude X_{avm} is used. It has a smaller variance than the non-averaged spectral magnitude.
Characterisation parameters are extracted from this averaged spectrum. Definitions and detailed measurement results of the characterisation parameters are given in the next sections.
Fig. 4.1 gives an impression of the SD-ADC behaviour and its noise shaping. Details are described in the next sections.

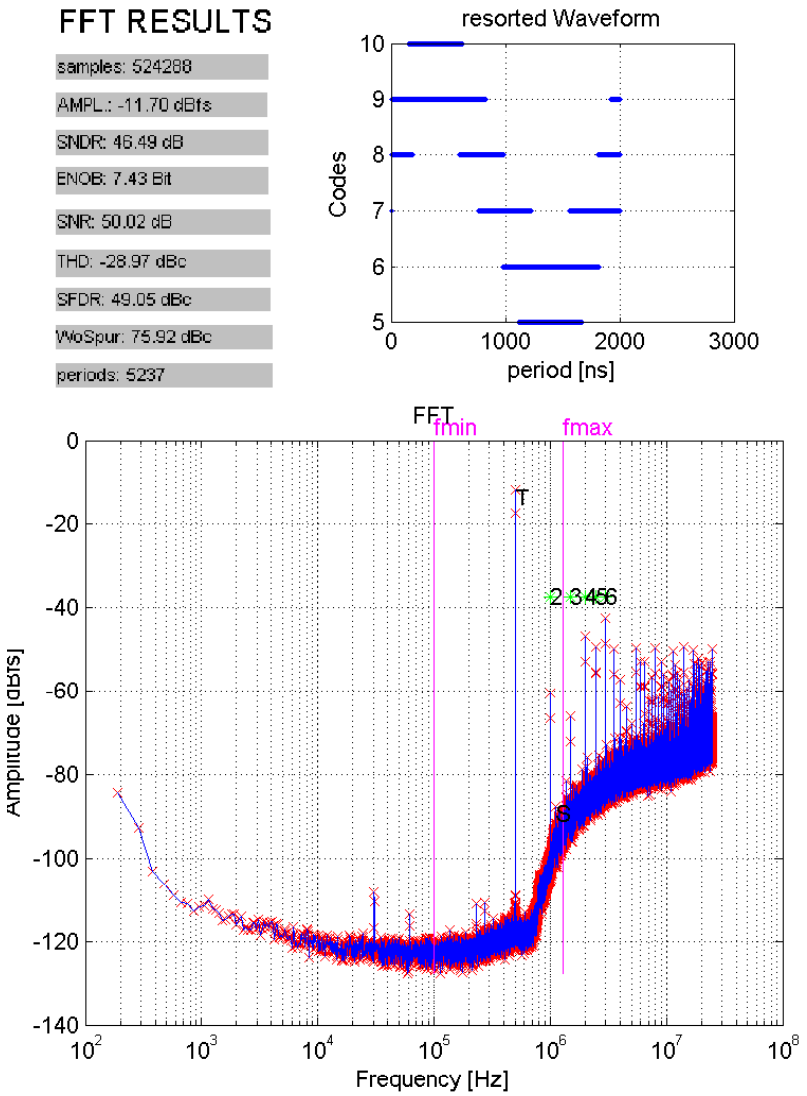


Figure 4.1: FFT output plot @-11dBV input level

4.1.1 Output level behaviour

Definition

In (4.4) the rms value of the input sine wave is defined. It is computed as the squared sum of the FFT bin at the input frequency and its aliased frequency bin. X_{avm} is described by (4.3).

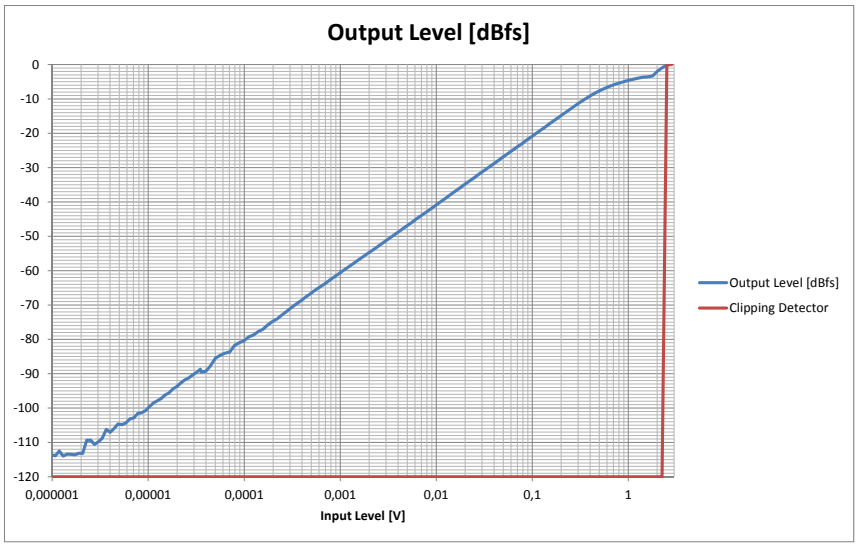
$$A_{rms} = \frac{1}{M}\sqrt{\left(X_{avm}\left(f_i\right)\right)^2 + \left(X_{avm}\left(f_s - f_i\right)\right)^2} \tag{4.4}$$

In the following section the peak-output value in dB is presented. It is calculated according to (4.5).

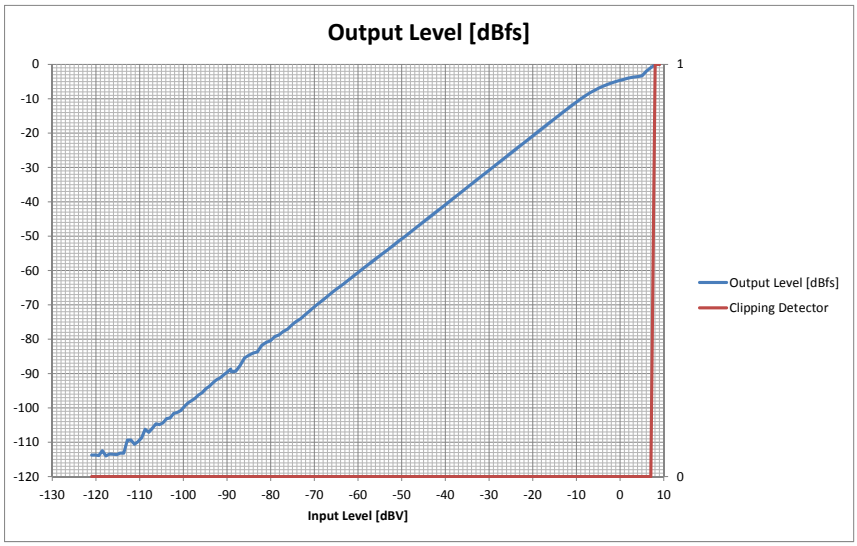
$$A_{peak} = 20\lg\left(\sqrt{2}A_{rms}\right) \tag{4.5}$$

Linear input level sweep

In Fig. 4.2(a) the input/output characteristic of the SD-ADC is shown. A specified FS Range of 2 V_{pp} is reached. An integrated clip-detector is detecting an overload situation of integrators in the SD-ADC. If an overload is detected, the clip-detector output pin is set to a logical high. This is evaluated during measurement. In Fig. 4.2(b) the clip-detector output is depicted versus input level. Once again a FS Range of 2 V_{pp} can be seen, demonstrated as an overload detection above 2 V_{pp} at the differential input pins.



(a) Input Level as Voltage

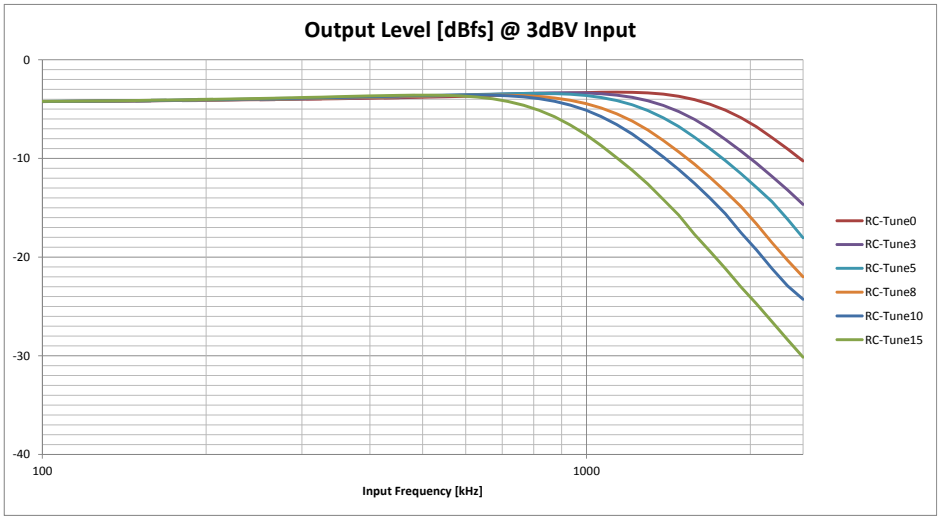


(b) Input Level as dBV

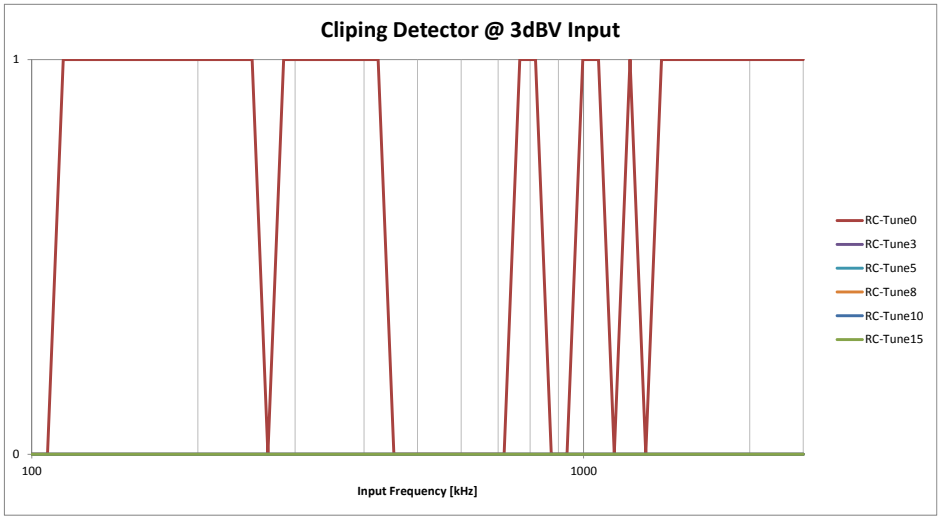
Figure 4.2: Output Level and Clipping Detector

Linear input frequency sweep

In Fig. 4.3(a) output level variation due to different RC-Tuning values is presented over frequency. The nominal RC-Tune value is specified as 8. A -3dB cutoff frequency of about 1290kHz can be seen. This and all other -3dB cutoff frequencies are in line with specification. The dependence of the clipping detector's output from the chosen RC-tuning value is shown in Fig. 4.3(b). A clipping of the SD-ADC with RC-Tune value 0 is expected due to the large input bandwidth. All other RC-Tune values seem to be stable and do not force the integrated SD-ADC into clipping. Therefore RC-Tune value 0 should not be used with large scale input signals.



(a) Output Level



(b) Cliping Detector

Figure 4.3: Output Level and Clipping Detector vs. input frequency

4.1.2 Signal-to-Noise-and-Distortion Ratio, Signal-to-Noise Ratio and Effective Number of Bits

Definition [7]

SNDR

Signal-to-noise-and-distortion ratio (SNDR) is defined as the ratio of rms signal to rms noise and distortion. SNDR is measured using sine-wave input signal. SNDR is depending on the amplitude and frequency of the applied sine wave, therefore these two are specified.
To obtain only the noise and distortion parts of the sampled spectrum the bins at DC and at the fundamental frequency and its alias are deleted (set to zero). Afterwards noise and distortion (NAD) is found by summing up the remaining Fourier components (4.6). [7]

$$NAD = \frac{1}{\sqrt{M\,(M-3)}} \sqrt{\sum_{m \in S_0} X_{avm}\,[f_m]^2} \tag{4.6}$$

$$SNDR = \frac{A_{rms}}{NAD} \tag{4.7}$$

Then SNDR is calculated by (4.7).

X_{avm}	is the averaged spectral magnitude as defined in (4.3)
S_0	is the set of frequency indices in the specified measurement bandwidth excluding the fundamental and DC
A_{rms}	is found by (4.4)
m	integer running from 1 to $M-1$

SNR

The signal-to-noise ratio (SNR) is described as the ratio of the rms signal to the rms noise of a sine-wave input signal of a specified frequency and amplitude. The rms noise is determined by calculating the rms noise and distortion as described in (4.6), and then determining the distortion as described in (4.12). The SNR is given by (4.9).

$$\eta = \sqrt{NAD^2 - A_{rms}^2 THD^2} \tag{4.8}$$

$$SNR = \frac{A_{rms}}{\eta} \tag{4.9}$$

ENOB [9]

A_{rms}	is the rms signal found by (4.4)
η	is the rms noise as determined by (4.8)
THD	Total harmonic distortion as described in (4.12)

The effective number of bits (ENOB) is defined as a measure of the signal-to-noise and distortion ratio using bits. Sometimes it is also referenced as resolution and defined as given in (4.10).

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{4.10}$$

$SNDR$	is the signal-to-noise-ratio in dB as defined by (4.7)

Linear input level sweep

Fig. 4.4 and Fig. 4.5 show the SNDR and SNR respectively. In a 10 kHz measurement bandwidth, a maximum SNR and SNDR of 84 dB are measured. The difference of the measured SNDR between 300 kHz and 10kHz measurement bandwidth is about 15 dB in the linear region of the plot. This is well in line with theory $b = 10 \cdot \lg \frac{300\text{kHz}}{10\text{kHz}} \approx 15dB$
Higher measurement bandwidth, such as the full input bandwidth of 1200 kHz already include some harmonics of the fundamental input frequency at 500 kHz. There a difference between the SNR and the SNDR can be seen clearly, where in the later also harmonic distortion is included. A Sigma-Delta ADC has its maximum SNR and respective its maximum SNDR not at maximum input level. In literature it is common to define the DR as the input range, where the SNDR exceeds 0dB. For the integrated POLLUX SD-ADC a DR of 106 [dBfs] at 10kHz measurement bandwidth is seen in Fig. 4.4. In Fig. 4.6 the ENOB is shown. Due to its nature of calculation, it shows similar behaviour as SNDR and is also dependent on the measurement bandwidth.

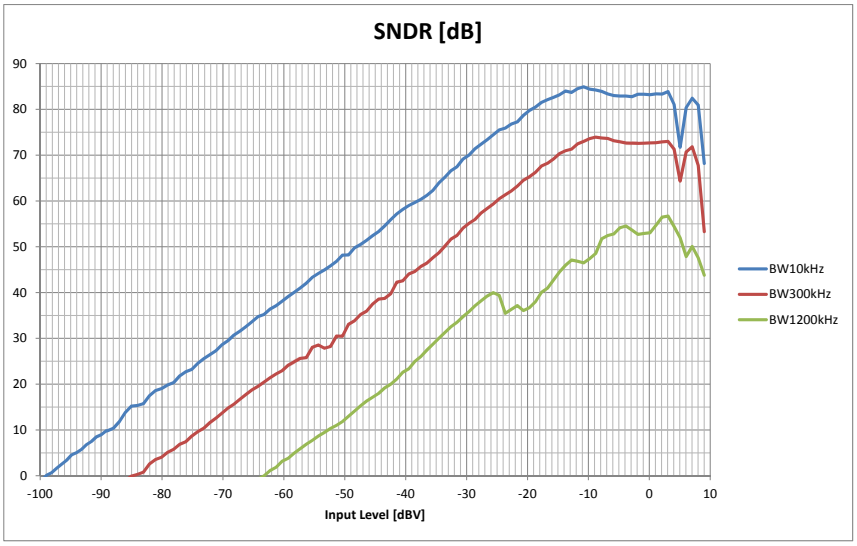


Figure 4.4: Signal-to-Noise-and-Distortion Ratio [dB]

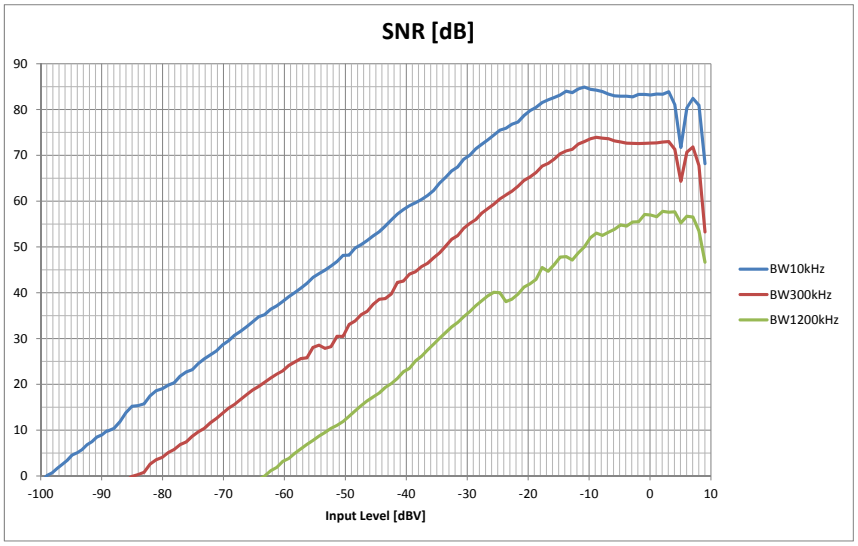


Figure 4.5: Signal-to-Noise Ratio [dB]

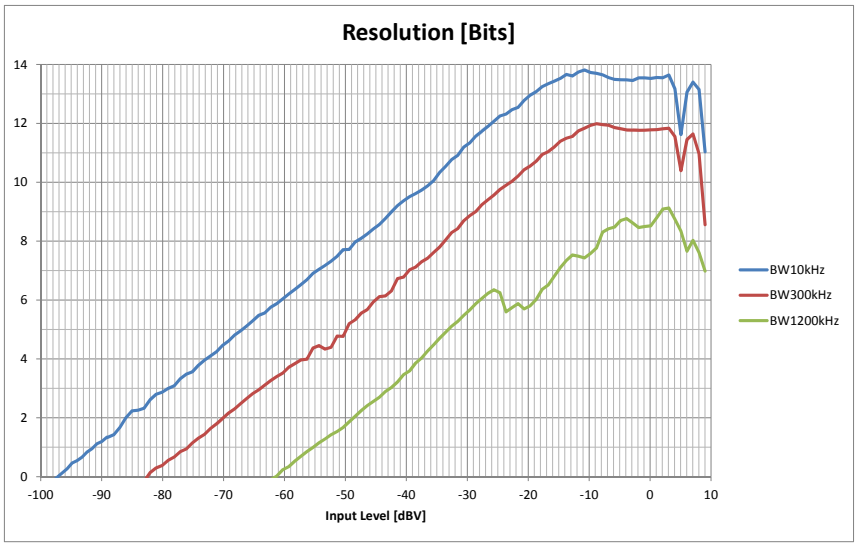


Figure 4.6: Resolution [Bit]

Linear input frequency sweep

For the following measurements, a measurement bandwidth of 300kHz is used. (asymmetrical to the center frequency, $f_{lower} = f_{center} - 50\text{kHz}$, $f_{upper} = f_{center} + 250\text{kHz}$). (See Fig. 4.7 and Fig. 4.8) Therefore for lower input frequencies the 2^{nd} and 3^{rd} harmonics are still in the measurement bandwidth and therefore the SNDR is diminished up to 250kHz. The SNR is aligned with measurements done in Section 4.1.2 at 73 dB at 500kHz. All *RC-Tune 0* curves are showing similar behaviour, due to a heavily distorted output signal caused by clipping of the integrated tracking ADC as mentioned above. ENOB is not plotted again. It has a similar behaviour across frequency as the SNDR due to (4.10).

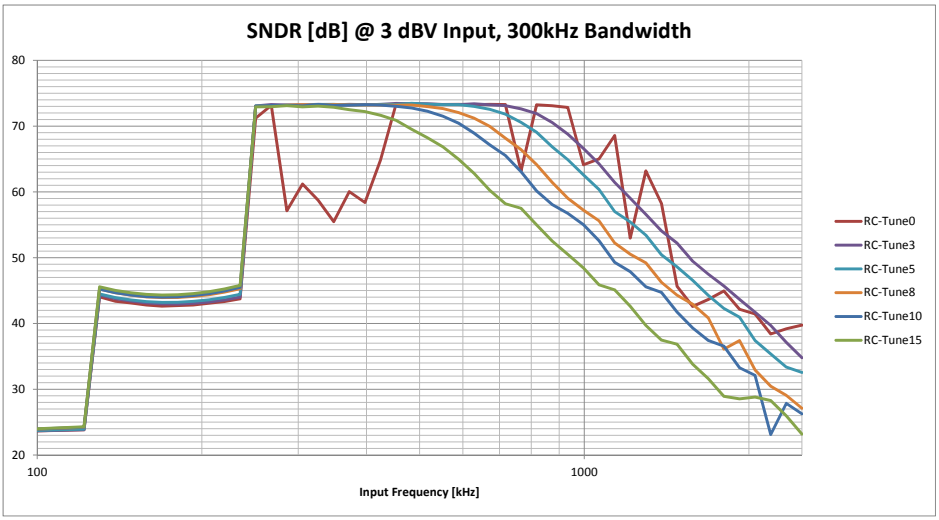


Figure 4.7: Signal-to-Noise-and-Distortion Ratio [dB]

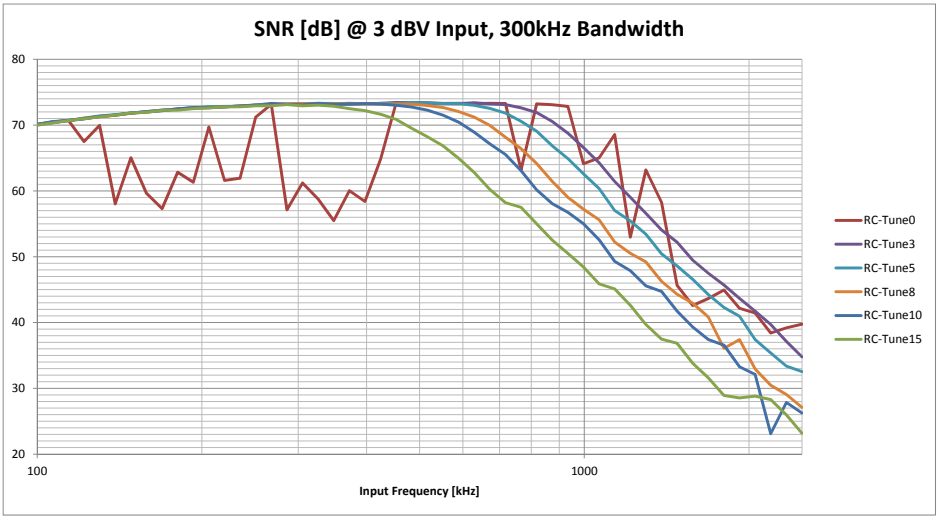


Figure 4.8: Signal-to-Noise Ratio [dB]

4.1.3 Spurious Free Dynamic Range

Definition [7]

The spurious free dynamic range (SFDR) is the frequency domain difference in decibels between the input signal level and the level of the largest spurious or harmonic component for a large, pure sine-wave signal input. [7] By this parameter the ADC's usable dynamic range is indicated.

Beyond this usable dynamic range, problems occur in spectral analysis. SFDR is a function of both amplitude and frequency of the input sine wave. Therefore amplitude and frequency of the measurement input sine wave are specified.

$$SFDR = 20 \lg \left(\frac{X_{avm}[n_1]}{\max\limits_{n \in N_{nf}} (X_{avm}[n])} \right) \tag{4.11}$$

$X_{avm}[n]$	is the averaged magnitude of the spectral component at frequency index n see (4.3)
N_{nf}	is the set of frequency indices in the specified measurement bandwidth excluding the fundamental and DC
n_1	is the index for the fundamental frequency

For the following plots the SFDR is calculated for a specified measurement bandwidth. This should reflect the bandwidth used later in different applications.

Linear input level sweep

In Fig. 4.9 the SFDR is presented as a linear sweep over input level range. According to the definition given in (4.11) it accounts for the usable dynamic range in a specific bandwidth. For the two lower bandwidths SFDR stays more or less the same over the whole input level range. In a wider bandwidth (e.g. the whole input bandwidth of 1200kHz), SFDR is degenerated due to starting noise shaping curvature and other spurs like harmonics, see as reference Fig. 4.1.

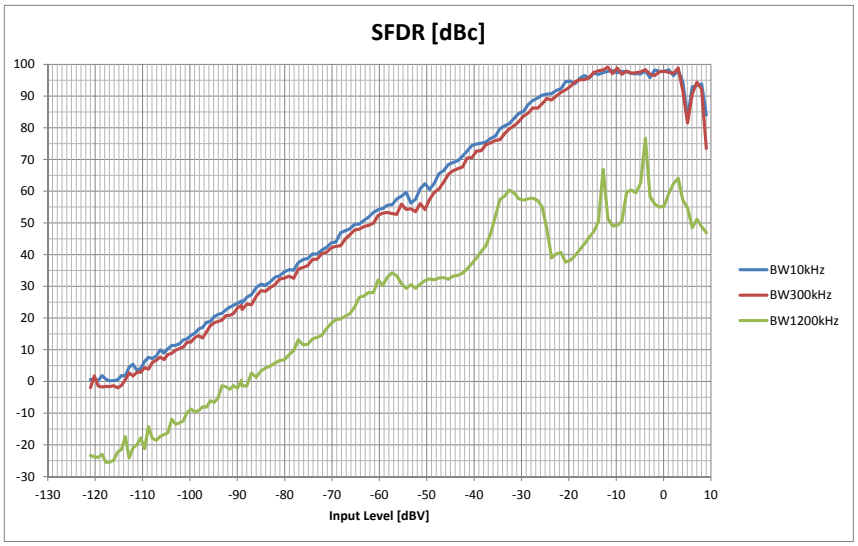


Figure 4.9: Spurious free dynamic range [dBc]

4.1.4 Harmonic Distortion

Definition [7]

Dynamic errors and integral non-linearities are contributing to harmonic distortion (HD) whenever an ADC is sampling a periodic signal. For a pure sine-wave input the output harmonic distortion components are found at spectral values, whose non-aliased frequencies are integer multiples of the applied sine-wave. Generally their amplitudes are given as a decibel ratio with respect to the fundamental amplitude (dBc). Their frequencies are usually expressed as a multiple of the frequency of the applied sine wave.
Total harmonic distortion (THD) is computed by (4.12)

$$THD = \frac{\sqrt{\frac{1}{M^2}\sum_{h=2}^{6}\left|X\left[f_h\right]\right|^2}}{A_{rms}} \tag{4.12}$$

$X\left[f_h\right]$	is the complex value of the spectral component at frequency f_h
f_h	is the h^{th} harmonic frequency of the DFT of the ADC output data record
M	is the record length
A_{rms}	is the rms value of the input sine wave, see (4.4)

All harmonics up to the 6^{th} harmonic are summed up.

In (4.13) the amplitude of the h^{th} harmonic is computed. In (4.14) it is related to the rms value of the input sine wave to give HD_h as the harmonic distortion at $h \times f_{in}$.

$$A_h = \frac{1}{M}\sqrt{\left(X_{avm}\left(f_h\right)\right)^2 + \left(X_{avm}\left(f_s - f_h\right)\right)^2} \tag{4.13}$$

$$HD_h = \frac{A_h}{A_{rms}} \tag{4.14}$$

Linear input level sweep

Harmonic distortion measurement results are shown in Fig. 4.10 (THD up to 6th harmonic) and Fig. 4.11 (2^{nd} and 3^{rd} harmonic). 2^{nd} harmonic was specified to 60 dB below carrier respective the fundamental output tone (see Tab. 2.2). As it is shown in Fig. 4.11 the 2^{nd} harmonic is not in specification. But this was a known problem at design review step. Overall it can be seen, harmonic distortion and respectively THD is lowest at about *-6dBfs* (see Fig. 4.10). Main contribution may come from 2^{nd} and 3^{rd} harmonics according to Fig. 4.11. So forcing input level beyond -6dBfs should be not considered, due to heavily distorted signals at SD-ADC output.

Figure 4.10: Total Harmonic distortion up to 6th harmonic [dBc]

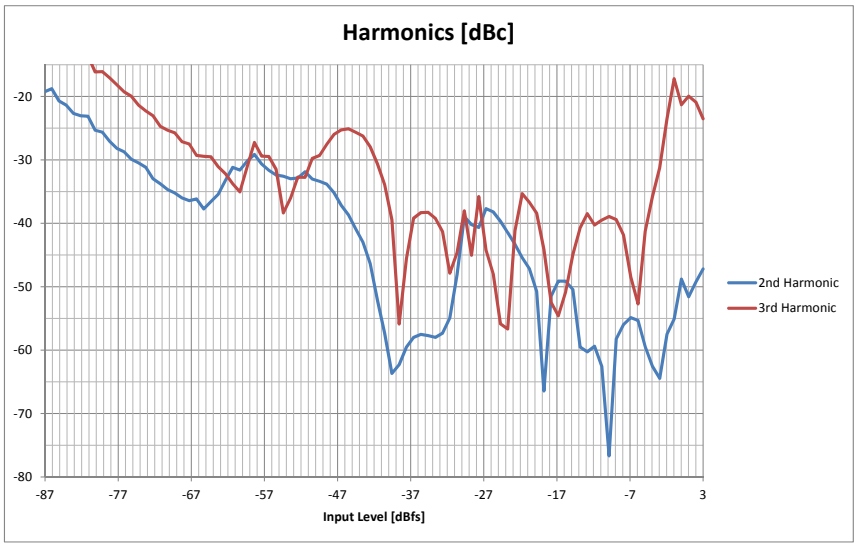


Figure 4.11: 2nd and 3rd Harmonic Distortion [dBc]

Linear input frequency sweep

Harmonic distortion measurements are presented in Fig. 4.12 to Fig. 4.14. Harmonic distortion is seen lower at higher frequencies for a certain frequency band as presented in Fig. 4.12. This frequency band is moving to higher frequencies with lower RC-Tuning values. (Moving of the lowpass-cutoff frequency of the SD-ADC towards higher frequencies).

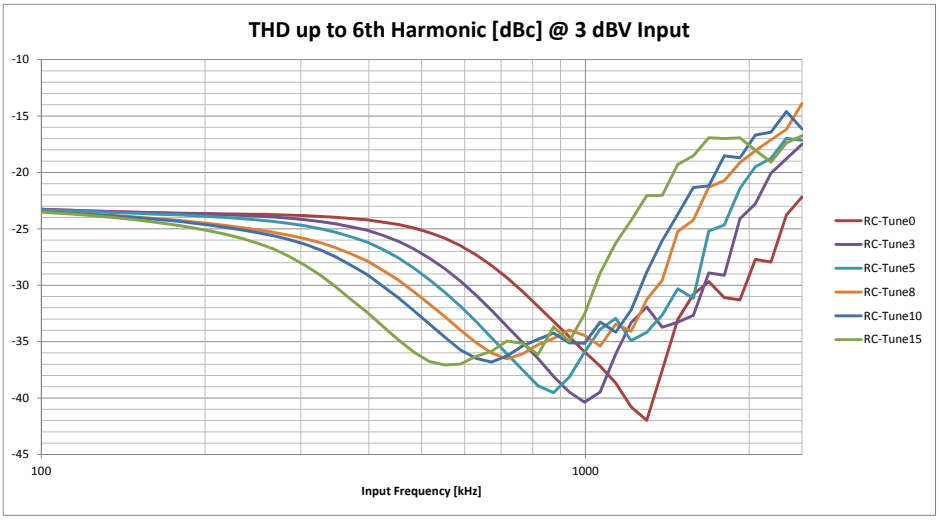


Figure 4.12: THD up to 6th harmonic

For the 2ndharmonic a pitch in all RC-Tuning curves can be seen from 550kHz to about 650kHz where the 2nd harmonic is below -60dBc and therefore could be stated as *in specification*. For the 3rd harmonic a similar behaviour to the THD can be stated and so it is in line with measurements in Section 4.1.4, where it is said the 3rd harmonic is the major contribution to the THD up to 6th harmonic.

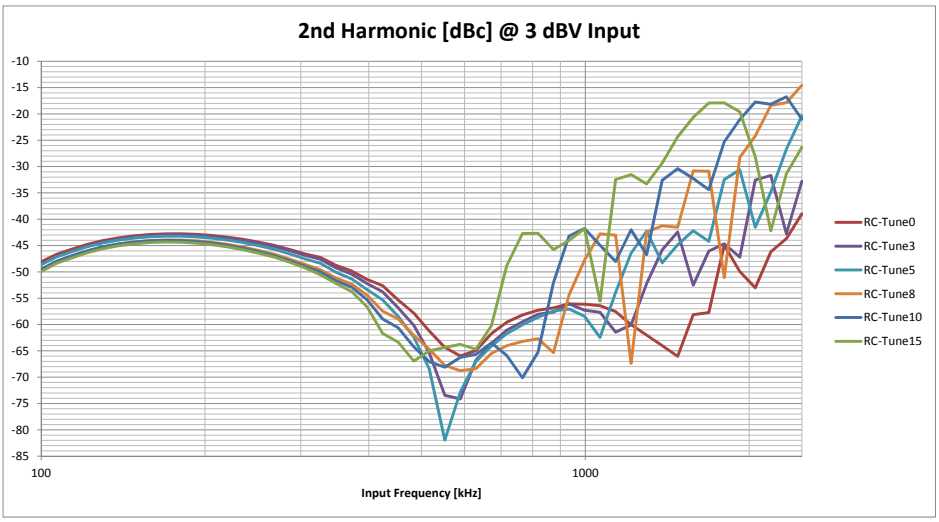


Figure 4.13: 2nd harmonic distortion [dBc]

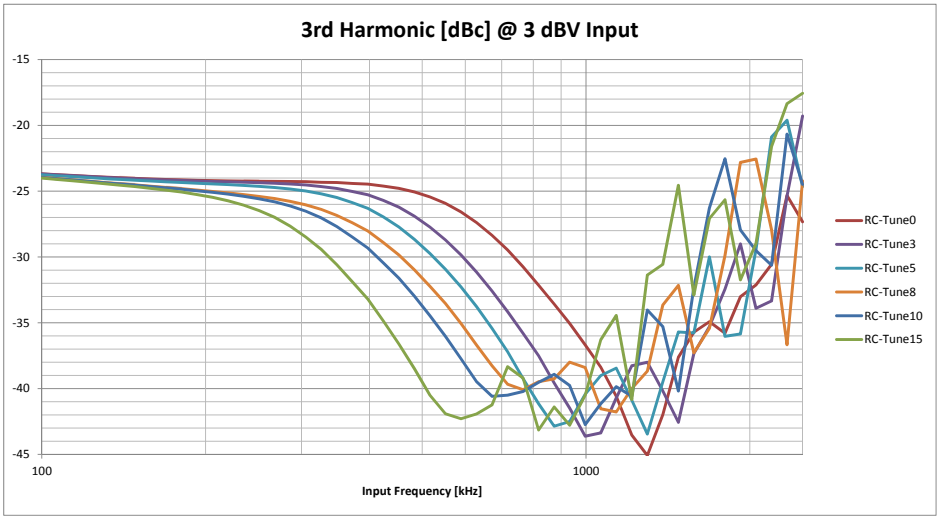


Figure 4.14: 3rd harmonic distortion [dBc]

4.1.5 Two Tone Characterisation

In this section the integrated SD-ADC is tested for linearity by a two tone test.

Rhode & Schwarz Signalgenerator SMBV100A

At first the signal generator R&S SMBV100A, used for generating the differential input signal, is tested for its linearity. For this purpose, the input-intermodulation-intercept-point of 3rd order is derived in a two tone test setup. Two sinusoidal input tones at frequencies 600 & 700 kHz are swept logarithmically by their input level. The 3rd order intermodulation product is located at 500 and resp. 800 kHz. In Figure 4.15 a output tone and the 3rdorder intermodulation product at 800 kHz are linearly interpolated and as an intercept point an *IIP3* of *+47 dBm* is found.

So far can be stated the R&S SMBV100A is sufficient linearly for testing the integrated POLLUX SD-ADC and the weak non-linearity will be taken into account for modelling in Section 5.2.

POLLUX Testchip - Sigma-Delta ADC

The linearity test in form of a two tone measurement has been specified at two different input frequency pairs and respective input level for the integrated SD-ADC. Therefore in Figure 4.16 a two tone intermodulation product of 2nd order at frequency of 250kHz is shown. In Figure 4.17 a similar two tone measurement is performed at 800 & 1200kHz and their 2nd order intermodulation product at 400kHz is shown. The wanted specification for each intermodulation frequency is plotted into the result plot to give a feeling for required linearity performance of the integrated SD-ADC. At input frequencies 500 & 750kHz and an input level of -12dBfs the 2nd order intermodulation product at 250 kHz should be below -62dBfs. In a same way it was defined for an input frequency pair of 800 & 1200kHz at an input level of -9dBfs to have an intermodulation product of 2nd order at 400kHz below -59dBfs.

Additionally to the specified two tone measurements above, a more meaningful measurement was done for input frequencies of 600 & 700kHz. Meaningful in a way, to get independent

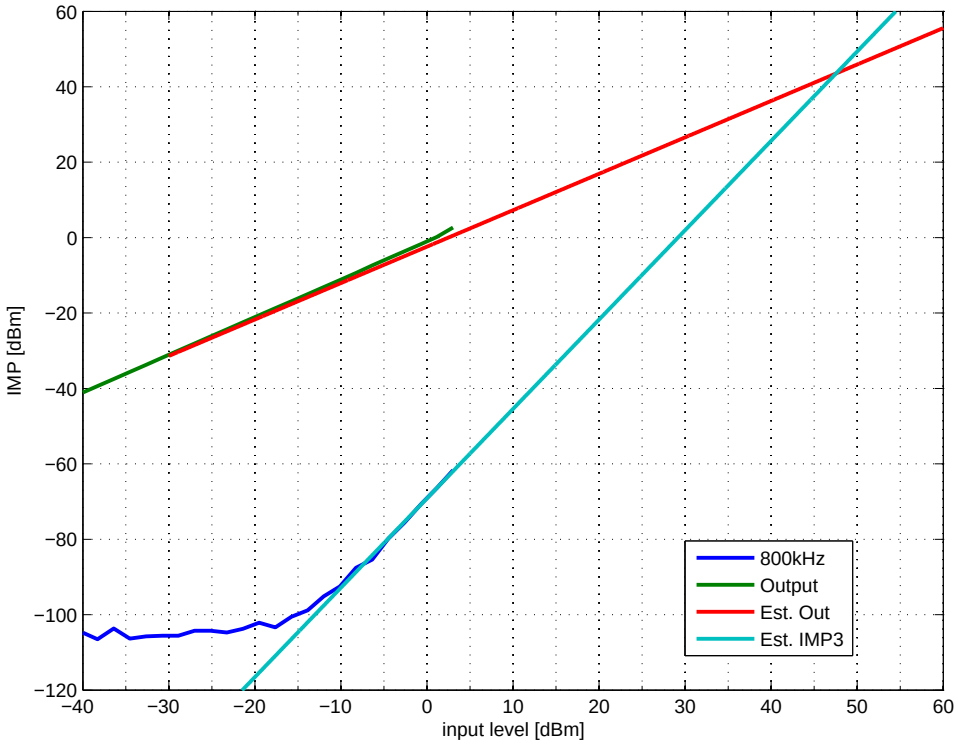


Figure 4.15: Intermodulation Interceptpoint 3^{rd} order

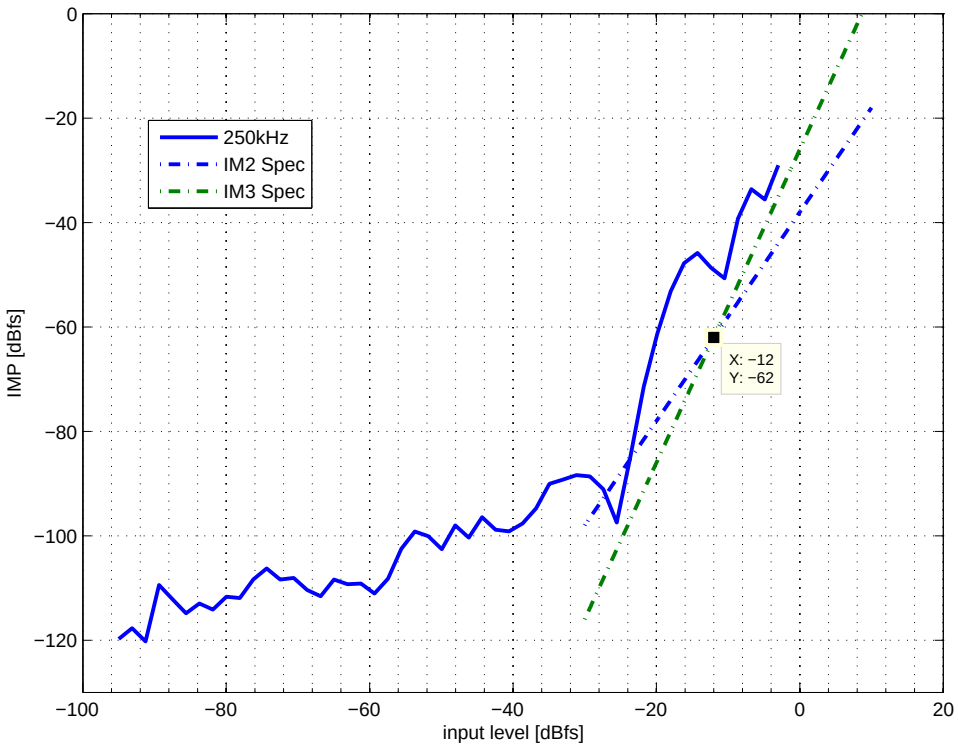


Figure 4.16: Intermodulation Product 500 & 750 kHz

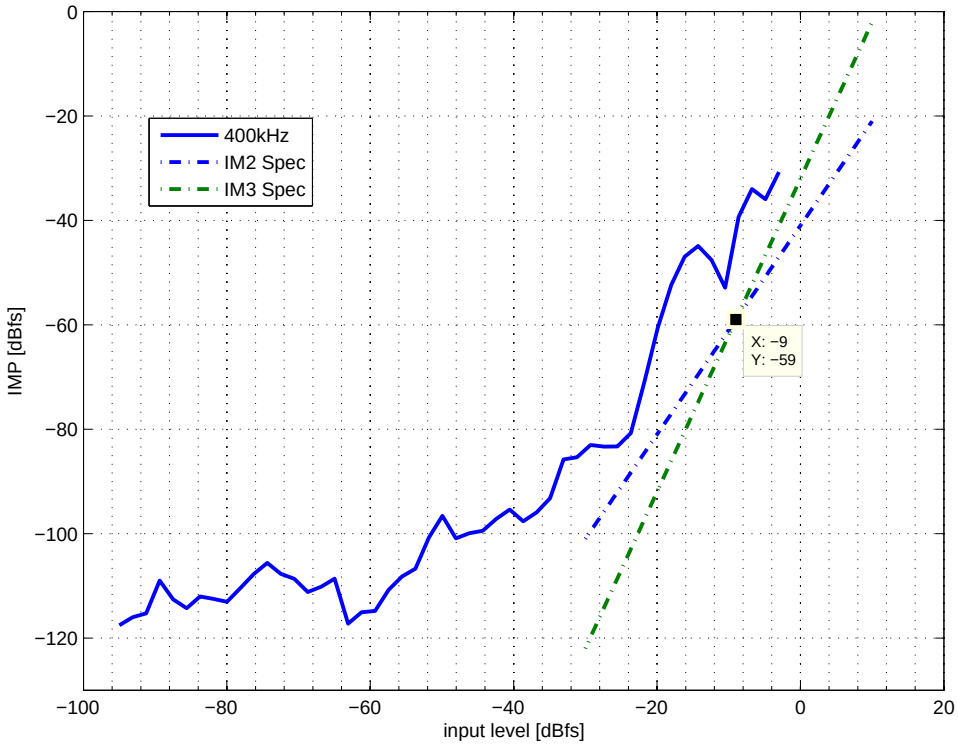


Figure 4.17: Intermodulation Product 800 & 1200 kHz

measurements for intermodulation products of 2nd and 3rd order, because in measurements as described above the two intermodulation products come together at the same frequencies.

In Figure 4.18 the derivation of an input-intermodulation-intercept-point (IIP) 2nd and 3rd order is shown. A best fit straight line with slope 2 and respectively 3 is plotted into measurement data and compared to straight line extrapolation of output at the fundamental frequency. In Equation 4.15 the straight line fit for the 2nd order IMP at 100kHz is presented. Equation 4.16 is representing a straight line fit to measurement data of IMD of 3rd order at 500kHz. Equation 4.17 is extrapolating a straight fit line to the output data at fundamental frequency of 600kHz.

$$IMP_2 = 2.0719 \cdot input - 41.4476 \tag{4.15}$$

$$IMP_3 = 2.9009 \cdot input - 23.9686 \tag{4.16}$$

$$output = 0.977 \cdot input - 3.5101 \tag{4.17}$$

From this Equations 4.15 - 4.17 IIP_2 and IIP_3 could be derived by simple rewriting. This is also done for data presented in Figure 4.19 by a two tone measurement at frequencies 250 & 300kHz. The slightly difference in IIP_2 and IIP_3 between these two measurements can be argued with slightly different fit to measurement data. But it can be stated from that two tone measurements a good linearity over frequency in the pass band.

In Table 4.3 measurement results for Two Tone measurements as described above are summarized. For the two input frequency pairs in passband a similar result in *Input-Intermodulation-*

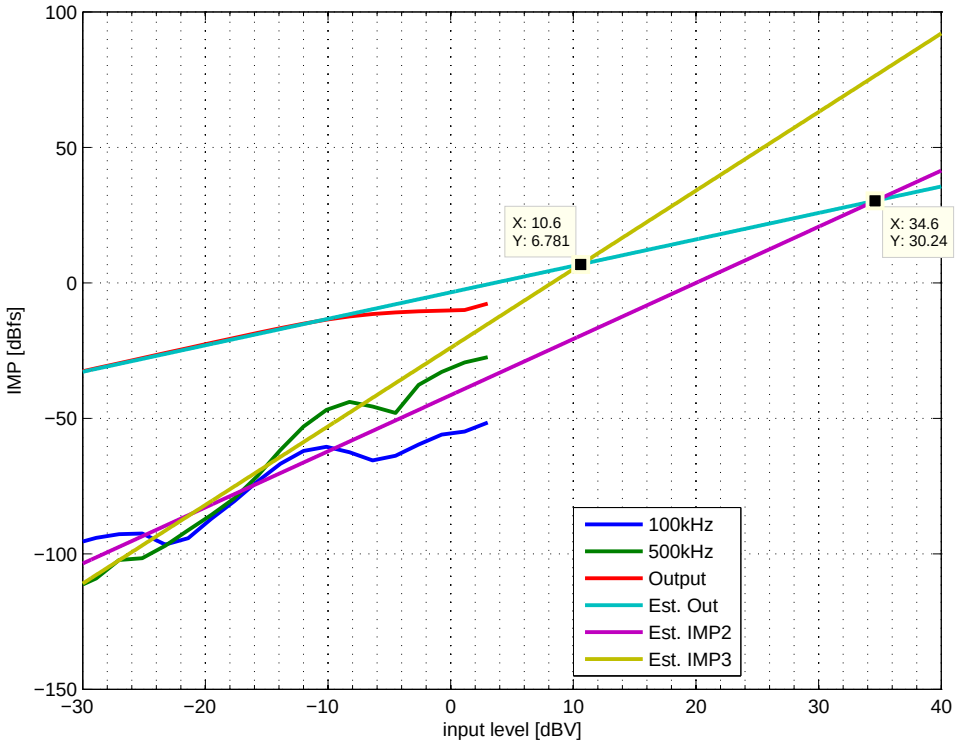


Figure 4.18: Intermodulation Product 600 & 700 kHz

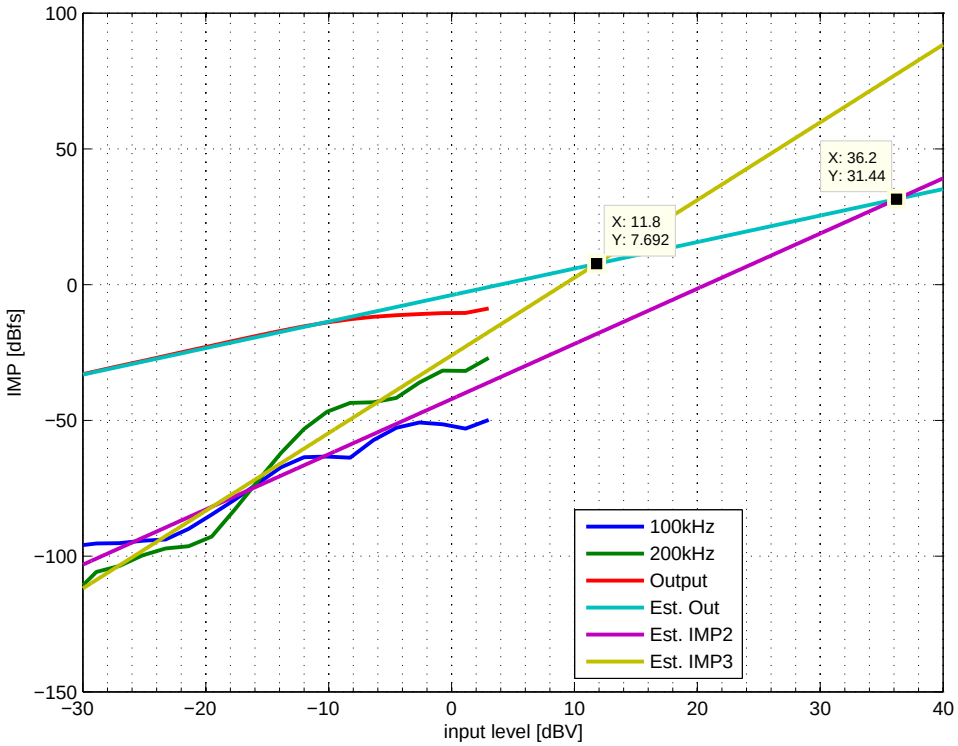


Figure 4.19: Intermodulation Product 250 & 300 kHz

Intercept-Point can be seen. These results are used in Chapter 5 to model the non-linearity in feedback path of the integrated SD-ADC.

f_{IN} [kHz]	IIP_2 [dBV]	IIP_3 [dBV]
250 & 350	34.65	10.63
600 & 700	36.25	11.79

Table 4.3: Input-Intermodulation-Intercept-Points

4.1.6 Figure of Merit

A Figure of Merit (FOM) should reflect the trade off between the three main design goals *Energy Consumption*, *Speed* and *Resolution*, which an ADC design has to deal with. In Literature, [2], [11], there can be found a huge variety of definitions for different Figure of Merits for ADC comparison. In the following subsection the integrated POLLUX SD-ADC is compared to a number of ADC which can be found in an regular update ADC survey by *Murmann [2]* and a newly encountered ADC survey by *Jonsson [11]*.
In Equation 4.18 the so-called Walden FOM is shown. The Walden FOM is more suitable for low resolution and Nyquist-ADC, whereas the Schreier FOM shown in Equation 4.19 is more suitable for high resolution designs which also push bandwidth [2]. Table 4.4 show the measurement results which are taken as input parameters by Equation 4.18 and 4.19. Results are shown in Table 4.5 and in Figure 4.20 and 4.21. f_{snyq} in Table 4.5 is given as the doubled effective bandwidth of the SD-ADC specified as 1.3MHz, which is labeled as BW_{plot}.*Murmann* has added a dotted line to his FOM_W plot, Figure 4.20, which marks a 1 fJ per conversion-step line and goes up with higher frequencies, since it is more challenging to get a fast and energy efficient design. This line and also the one in 4.21 could be seen as a lower resp. upper bound to reach and it is representing the data set quiet well. Recently published papers approach e.g. exceed this drawn border already.

Year	Technology	SNDR [dB]	SNR [dB]	DR [dB]	SFDR [dB]	P [mW]	f_s [MHz]
2003	-	56.7	57.7	69	76.6	3.28	50

Table 4.4: Figure of Merit - parameters

$$FOM_W = \frac{P}{2^{ENOB} \cdot f_s} = \frac{P}{2^{\frac{SNDR-1.76}{6.02}} \cdot f_{synq}} \tag{4.18}$$

$$FOM_S = SNDR + 10 \cdot \lg \frac{BW}{P} = SNDR + 10 \cdot \lg \frac{BW_{plot}}{P} \tag{4.19}$$

f_{snyq} [MHz]	P/f_{synq} [pJ]	BW_{plot} [MHz]	FOM_W [fJ/conversion-step]	FOM_S [dB]
2.6	1260	1.3	2253.9	142.7

Table 4.5: Figure of Merit - results

In Figure 4.22 and 4.23 it was the general idea to have two separated plots for energy efficient and on the other hand fast designs, where one or the other can respectively shine. It is

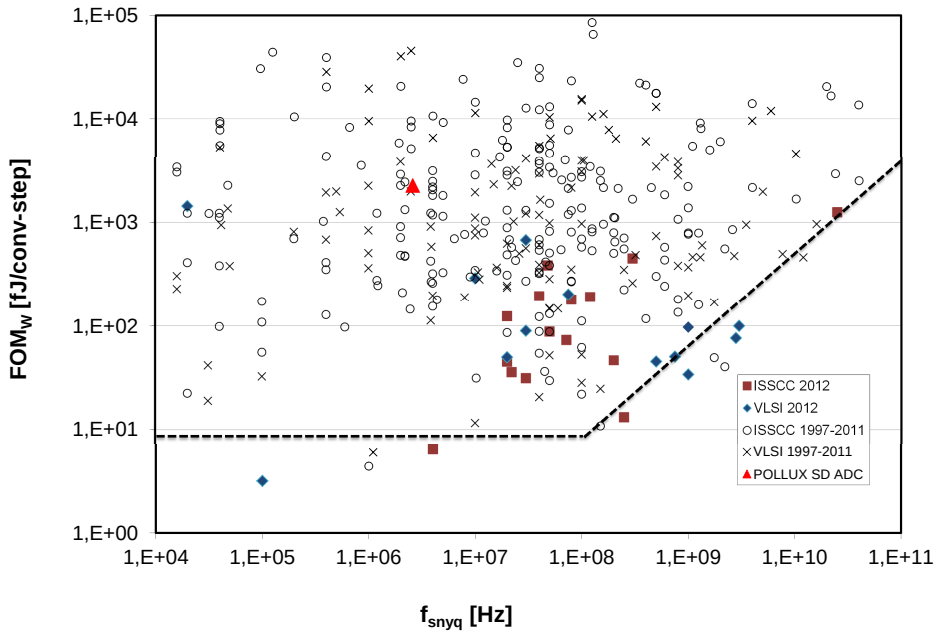


Figure 4.20: Walden Figure-of-Merit [2]

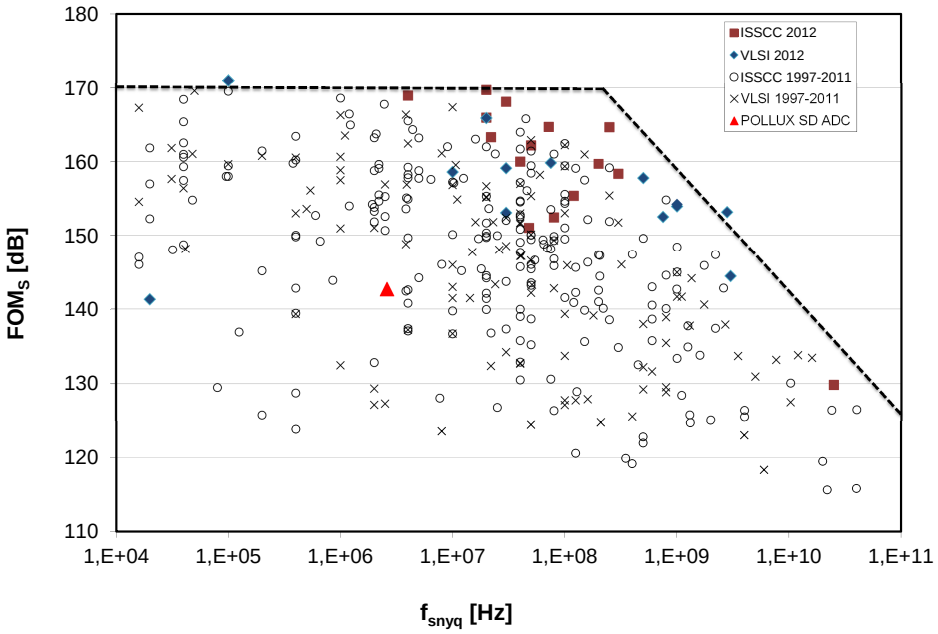


Figure 4.21: Schreier Figure-of-Merit [2]

usually not common to have designs which look good in both plots.[2] [12]. In Figure 4.23 both plotted performance lines are fictive sampler with only the specified jitter numbers and no other nonidealities like quantization noise, . . . are taken into account. In Figure 4.22 the dashed line is representing a Walden FOM at 10 fJper conversion-step and the solid line is showing a Schreier FOM where it is assumed that the ADC power is limited by thermal noise and so for increasing the precision (SNDR) by 6 dB the power consumption quadruples. There can be seen as in the former case a alignment with the data set.

From the result table and the resulting plots it can be seen the evaluated POLLUX SD-ADC is in every aspect in a resp. good position, compared to the more recently published papers. It should be kept in mind, that this integrated SD-ADC was designed at the begin of the last decade.

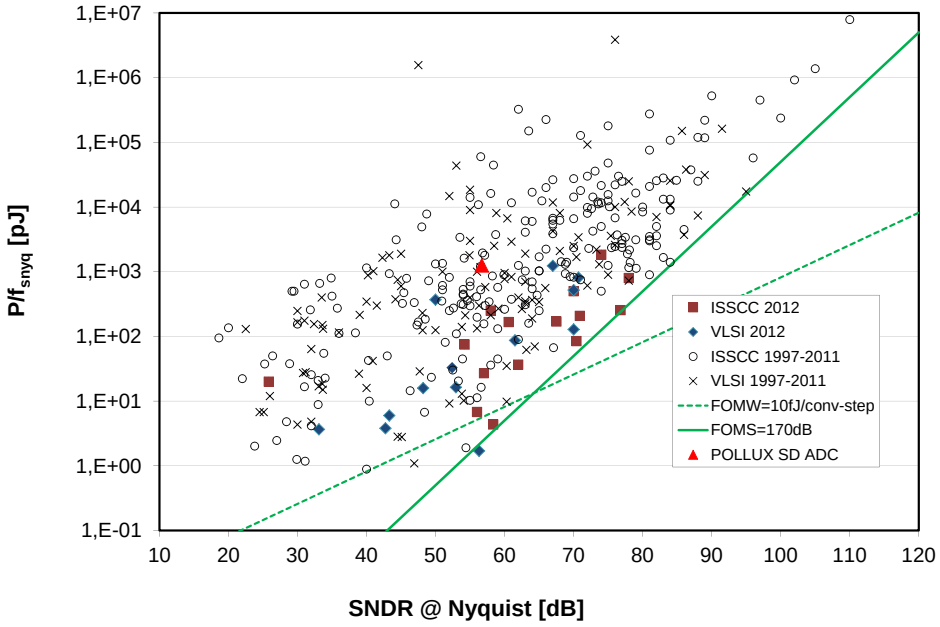


Figure 4.22: Energy optimized highlighting FoM [2]

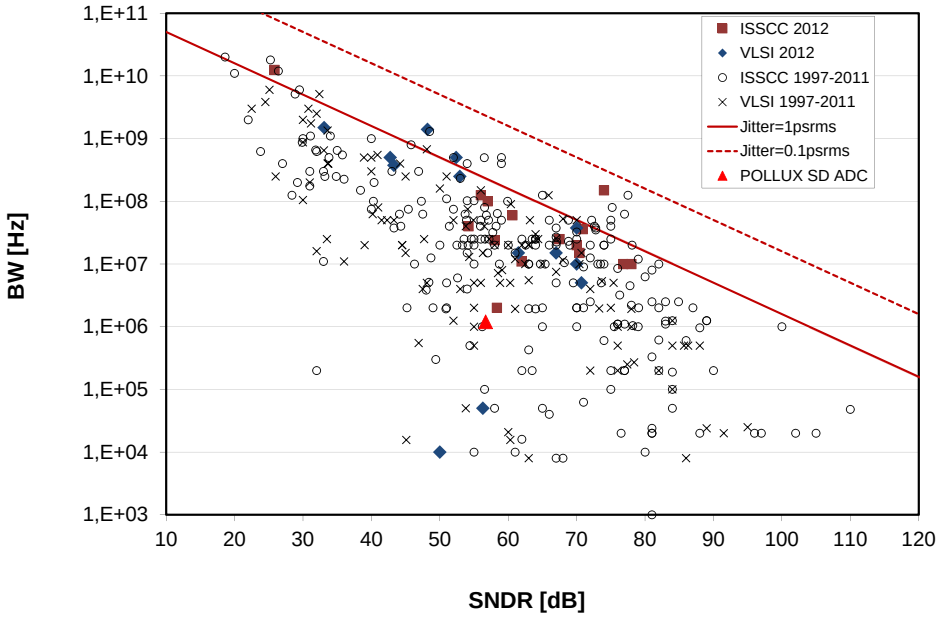


Figure 4.23: Speed optimized highlighting FoM [2]

A slightly different FOM, the so-called Thermal FOM [13] which is presented in 4.20, is introduced to encounter for high-resolution ADC mainly limited by thermal noise. A similar

idea was also introduced with the former mentioned Schreier-FOM. As in above descriptions for FOMs, f_s is the Nyquist-Sampling Rate, e.q. the Nyquist Bandwidth, ENOB the ENOB and P the power consumption of the ADC.

$$FOM_{Thermal} = \frac{P}{2^{2 \cdot ENOB}} \cdot f_s \tag{4.20}$$

The $FOM_{Thermal}$ is improving by 4 × for every additional bit of resolution, as it is also seen in Schreier-FOM. This matches the theoretical 4 × increase in power if the ENOB is limited by thermal noise. In [13] Nyquist-ADCs and Sigma-Delta ADCs are threaten separately. In Table 4.6 only the later state of the art is given.

FOM [aJ]	From	Architecture	Reference
1.1	Sept. 2011	DT-DSM	[14]
3.1	Sept. 2007	CT-DSM	[15]
4.4	2003	CT-DSM	POLLUX integrated SD-ADC

Table 4.6: DSM ADCs state of the Art Thermal-FOM

For the integrated POLLUX SD-ADC equation 4.20 is filled with values from table 4.4 and as result the Thermal-FOM is given as $FOM_{Thermal} = 4.04\,pJ$.

4.2 Discussion and Conclusion

In this chapter the integrated POLLUX SD-ADC has been characterized according to definitions found in literature and tested against specifications defined in Chapter 2. For convenience in Tab. 4.8 again known design specifications are given. In Tab. 4.7 measurement results obtained in preceding subsections are presented in a short summary. They can be compared easily to design specifications. Therefore it can be seen, the integrated POLLUX SD-ADC has met in most cases the required specifications. From Subsection 4.1.5 we know already the missed intermodulation and linearity requirement, defined by intermodulation distortion and harmonic distortion. The former is about 15 dB higher than specified and the latter is very frequency dependent. As outcome it can be stated, the characterized SD-ADC can be used in an linear transceiver as defined, with marginal loss on linearity performance. This was known already from a design review step. These loss in linearity has to be accounted for in frequency and level planning of the analog frontend of the radio-frequency receiver chain and also in the digital backend. The integrated POLLUX SD-ADC is reaching a resolution of ≈ 14 bit in the specified high performance mode of 10kHz bandwidth and is also designed very efficiently with respect to power consumption, which is shown in Section 4.1.6. It can score even the hard specification of current consumption below 3mA. All together it can be stated the integrated POLLUX Sigma-Delta Analog-to-Digital Converter is a well and according to specification designed high performance Analog-to-Digital converter.

Measurement Bandwidth	10kHz	300kHz	1200kHz
SNDR [dB]	84.9	73.9	56.7
Resolution [Bit]	13.81	11.98	9.12
Dynamic Range [dB]	99	84	63
SFDR [dBc]	99	99	76
I_{ADC}	2.18 mA		
VDD_{ADC}	1.5 V		

Table 4.7: Measurement results summary

f_{signal}	250 - 750kHz	high performance
f_{signal}	100 - 1300kHz	reduced performance
FullScale	2 V	at differential inputs
f_{clock}	50MHz	
DR	84 dB	at 10kHz Bandwidth
SNDR	66 dB	at 300kHz Bandwidth
I_{ADC}	<3 mA	
V_{dd}	1.4 . . . 1.6 V	
Temperature Range	-40 ℃. . . 135 ℃	

enhanced linearity performance

2^{nd}Harmonic	<60 dB	
Input	Intermodulation Distortion	
at -12 dBfs	<-62 dBfs	at 250kHz
at -9 dBfs	<-59 dBfs	at 400kHz

Table 4.8: POLLUX SD-ADC Specifications

5 ADC modelling

In literature many different approaches for modelling a system showing linear and non-linear behaviour can be found. However, especially for an Analog-to-Digital converter in most cases just a linear assumption is used to get a good fit behaviour model on a first shot. For an ADC used in radio-frequency and communication applications as the integrated POLLUX SD-ADC also the non-linear behaviour is of interest. Therefore one of the goals of this thesis is to characterise and fit a model to the non-linear behaviour of this integrated SD-ADC. In Section 5.1 a linear state space model is derived from known design specifications. That linear state space behavioural model is describing the main low pass characteristics of the integrated SD-ADC quite well. In Section 5.2 the linear model is refined for modelling non-linear behaviour such as harmonic and intermodulation distortion. Refinement of the model is done by including measurement data and utilising the System Identification Toolbox included in Matlab [3]. In subsection 5.3 a comparison between model output and related measurement data is given to get an idea of the quality of the model.

5.1 Linear Model

Fig. 5.1 is representing the implemented architecture of the integrated POLLUX SD-ADC in discrete time. The sampling process is implemented in the 4 bit quantizer, but for ease of calculation and presentation the architecture is presented in discrete time. Any linear system can be described by a set of linear difference or differential equations.

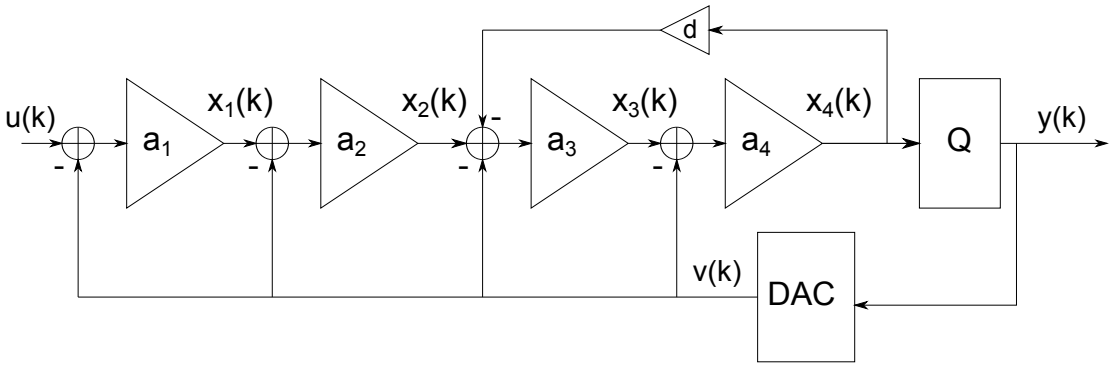


Figure 5.1: POLLUX Architecture

A set of linear difference equations in (5.1) to (5.4) is describing the behavioural structure of the integrated SD-ADC utilising state space variables. The discrete time equations and coefficients can be found by impulse-invariant transformation from continuous time representation. Following Schreier et. al. [6]. These discrete difference equations are formed to matrix notation in form of (5.5) and (5.6). Some interpretation of each matrices in (5.5) can be done, where as x(k) is $n \times x$ state vector at time k (n is the order of the system, in case of this work $n = 4$), $\boldsymbol{A}$ is an $n \times n$ matrix describing the interconnections within the loop filter, $\boldsymbol{B}$ is an $n \times 2$ matrix describing how the input u(k) and the feedback output v(k) are applied to the loop filter, while $\boldsymbol{C}$ and $\boldsymbol{D}$ are $1 \times n$ and 1×2 matrices describing how y(k), the output of the loop filter, is computed from x(k), u(k) and v(k). [6]

$$x_1(k+1) = (u(k) - v(k)) \cdot a_1 \tag{5.1}$$
$$x_2(k+1) = (x_1(k) - v(k)) \cdot a_2 \tag{5.2}$$
$$x_3(k+1) = (x_2(k) - v(k) - d \cdot x_4(k)) \cdot a_3 \tag{5.3}$$
$$x_4(k+1) = (x_3(k) - v(k)) \cdot a_4 \tag{5.4}$$

$$x(k+1) = \boldsymbol{A}\, x(k) + \boldsymbol{B} \begin{bmatrix} u(k) \\ v(k) \end{bmatrix} \tag{5.5}$$
$$y(k) = \boldsymbol{C}\, x(k) + \boldsymbol{D} \begin{bmatrix} u(k) \\ v(k) \end{bmatrix} \tag{5.6}$$

In equations (5.7) and (5.8) matrices $\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}$ and $\boldsymbol{D}$ are given as they are utilised by the POLLUX integrated SD-ADC architecture. The parameters a_1 to a_4 and d are calculated by given design parameters according to equations (5.9). Parameters a_1 to a_4 are representing the four integrator stages integrated into the loop filter stage of the integrated SD-ADC. Parameter d is describing the feedback resonator integrated into the loop filter at the 4th integrator stage. It is used to enhance the noise shaping performance of the loop filter.

$$\boldsymbol{A} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ a_2 & 0 & 0 & 0 \\ 0 & a_3 & 0 & -a_3\, d \\ 0 & 0 & a_4 & 0 \end{bmatrix} \qquad \boldsymbol{B} = \begin{bmatrix} a_1 & -a_1 \\ 0 & -a_2 \\ 0 & -a_3 \\ 0 & -a_4 \end{bmatrix} \tag{5.7}$$

$$\boldsymbol{C} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \qquad \boldsymbol{D} = \begin{bmatrix} 0 & 0 \end{bmatrix} \tag{5.8}$$

$$a_n = \frac{1}{f_s\, R_n\, C_n} \qquad d = \frac{R_3}{R_{resonator}} \tag{5.9}$$

5.2 Non-linear Model

The main contributor to non-linear behaviour in a N-Bit SD-ADC ($N > 1$) is located in the feedback path of the SD-ADC. In the feedback path a N-Bit Digital-to-Analog converter can be found. Capacitor mismatch and other non-linearities in such a multi bit DAC are the biggest contributors to non-ideal and non-linear behaviour of the overall SD-ADC system architecture. Beside this non-ideality in the feedback path, the hard saturation at the quantisation stage is another main contributor to the overall system non-ideality.
In literature [16, 17] the Hammerstein model is a well known and commonly applied non-linear dynamic modeling approach. A separation between the non-linearity and the dynamics of a process is assumed. A non-linear static block followed by a linear dynamic block is called the Hammerstein model. The non-linear element may account for non-linear effects that can be brought to the input of the system. The static non-linearity is approximated by a polynomial. In this work the polynomial is parametrised by measurement data obtained, which are obtained in Chapter 4.
If the sequence of non-linear and linear block is exchanged, and a linear block is followed by a non-linear block, such a model can be found as a Wiener model in literature. In this model structure any type of non-linearity, which can be brought to the output of a system, is represented by the non-linear block in sequence to the linear block. This can be for example a saturation effect of the quantization stage as it is in the case for the SD-ADC in this work.
In literature a combination of these two model structures is known as so called Hammerstein-Wiener system (see Fig. 5.2).

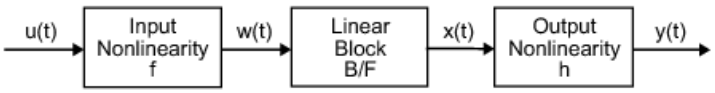


Figure 5.2: Hammerstein-Wiener Model Structure [3]

In this work the Hammerstein-Wiener model structure (as depicted in Fig. 5.3) is utilised to describe the non-linear model approach to the POLLUX integrated SD-ADC:

- The linear state space model is followed by a quantisation block, which implicitly represent the quantization noise and saturation effects occurring at the output of an Analog-to-Digital converter. Saturation effects are caused due to limited digital output and limited analog input range given by parameter fullscale range and reference voltage.

- At the positive input port of the linear state space model a non-linear block is accounting for the output non-linearity of the signalgenerator used in the measurement setup. Usually this is modelled by a weak polynomial non-linearity.
- As already mentioned above the main contributor to non-linear behaviour of the SD-ADC is understood to be in the feedback path, caused by a mismatch of capacitor arrays in the feedback Digital-to-Analog converter. This non-linearity is modelled by a polynomial block at the second (e.g. subtracting) input port of the linear state space model.

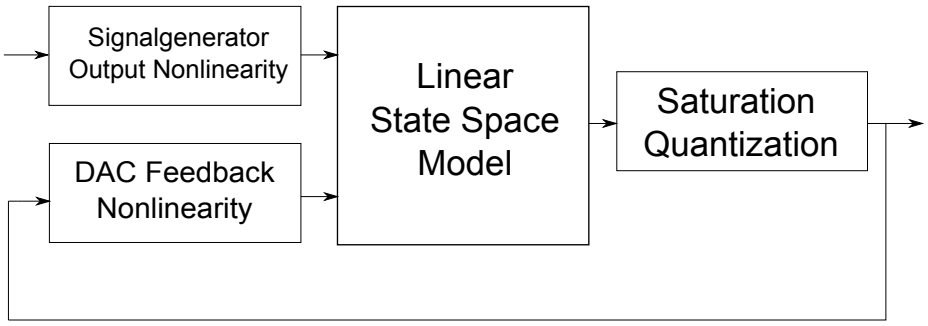


Figure 5.3: Non-linear Model Structure

The two polynomial non-linear block structures are parametrised by IIP2 and IIP3 values, as obtained in Section 4.1.5 for the signalgenerator output non-linearity and for the feedback path non-linearity respectively. In (5.10) to (5.16) the polynomial structure and parameters utilised in the non-linear blocks are given.[18]

$$y = a_0 + a_1\, x + a_2\, x^2 + a_3\, x^3 \tag{5.10}$$

$$a_0 = 0 \tag{5.11}$$

$$a_1 = 1 \tag{5.12}$$

$$a_2 = \frac{1}{ip_2} \tag{5.13}$$

$$a_3 = -\frac{4}{3} \cdot \frac{1}{{ip_3}^2} \tag{5.14}$$

$$ip_2 = \sqrt{10^{\frac{IP2dBV}{20}}} \tag{5.15}$$

$$ip_3 = \sqrt{10^{\frac{IP3dBV}{20}}} \tag{5.16}$$

5.3 Model vs. Measurement

In preceding Section 5.1 and Section 5.2 the model structure is explained and in subsection 4.1 measurement data is described. In the following subsections results obtained by the simulation model are compared to the obtained measurement data. This is done in a similar structure as used in Chapter 4 for the description of the measurement data, divided into a linear input level sweep, an input frequency sweep and three two tone scenarios. This should cover the main applications of the utilised model.

In the simulation runs, the feedback path non-linearity block was parametrised with different IIP2 and IIP3 values, to be able to compare the influence of different IIP2 and IIP3 values on the model output. The signalgenerator output polynomial was parametrised with the same values as obtained by measurement for all simulation runs.

5.3.1 Linear Input Level Sweep

In this subsection the non-linear polynomial in the feedback path is parametrised with different values, and an input level sweep with a single input tone at 500kHz is done. The results are presented in Fig. 5.4 to Fig. 5.6. These figures show a good small scale behaviour of the obtained model and a similar large scale behaviour in terms of output level and SNDR for parametrised feedback non-linearity. For the model without non-linearity in the feedback path and non-linearity only at the positive input port of the linear state space model only an influence of the saturation non-linearity at the output of the linear state space model can be seen. The simulation results for THD (Fig. 5.6) and for the SNDR (Fig. 5.5) show a trend, which is in most of the points too optimistic compared to measurement data.

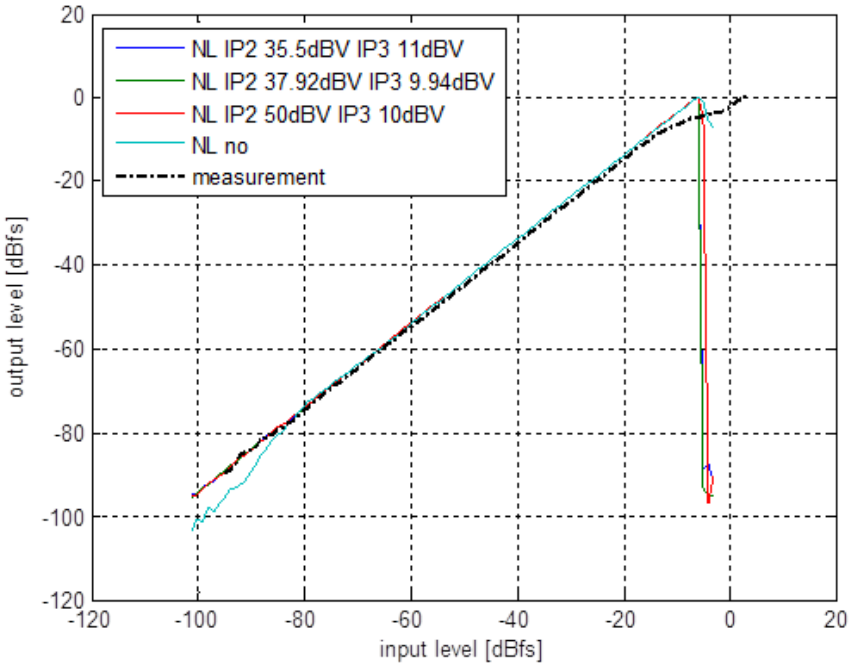


Figure 5.4: Level Sweep Output [dB]

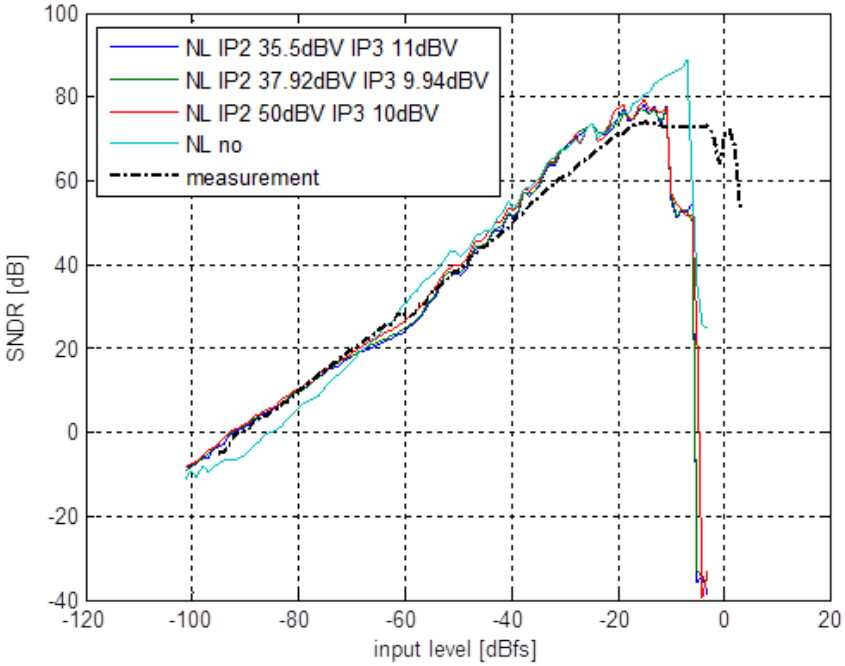


Figure 5.5: Level Sweep SNDR [dB]

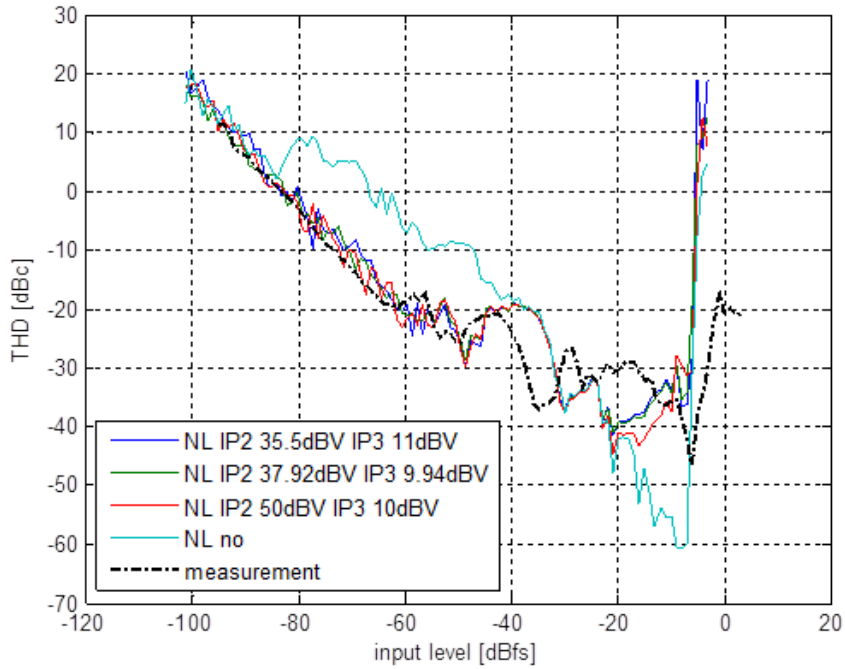


Figure 5.6: Level Sweep THD [dB]

5.3.2 Linear Input Frequency Sweep

In this subsection the frequency of the sinusoidal input signal is increased from 100kHz to 2500kHz similar to the measurement for frequency characterisation described in Chapter 4. This time the input level is kept constant at -19dBfs, to obtain a so called small scale frequency behaviour. The small scale behaviour of the model is more interesting, as in the previous section it is seen to be very inaccurate for large scale inputs. Fig. 5.7 to Fig. 5.9 are representing the model output data compared to measurement results. From these figures it can be seen that the simulated output level is similar to the obtained measurement data. However, for the interesting parameters SNDR and THD the model could only obtain a trend and is, as mentioned above often too optimistic as compared to the measurement data. From Fig. 5.9 it can be seen that a good fit around 500kHz(i.e. the application frequency) is obtained.

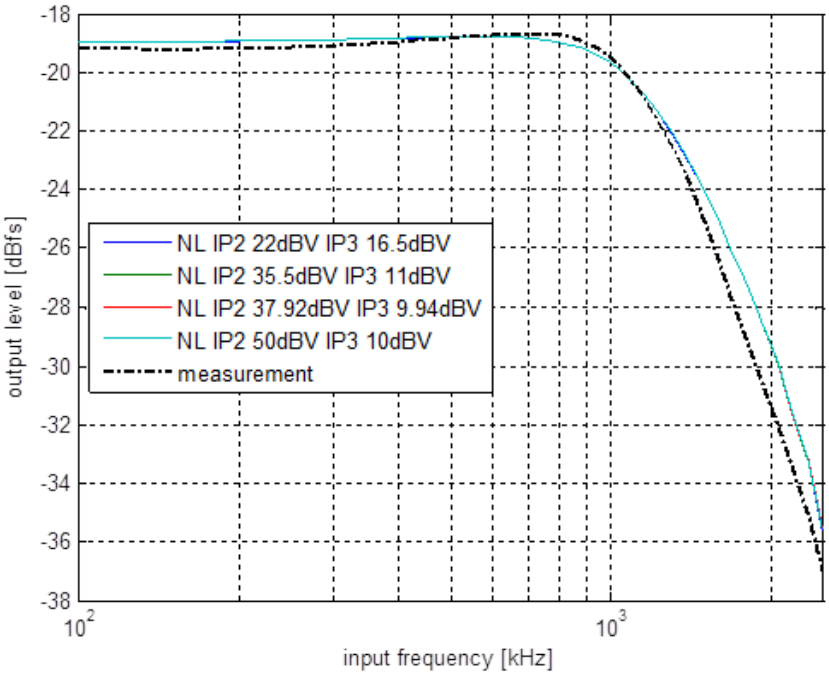


Figure 5.7: Frequency Sweep Output [dB]

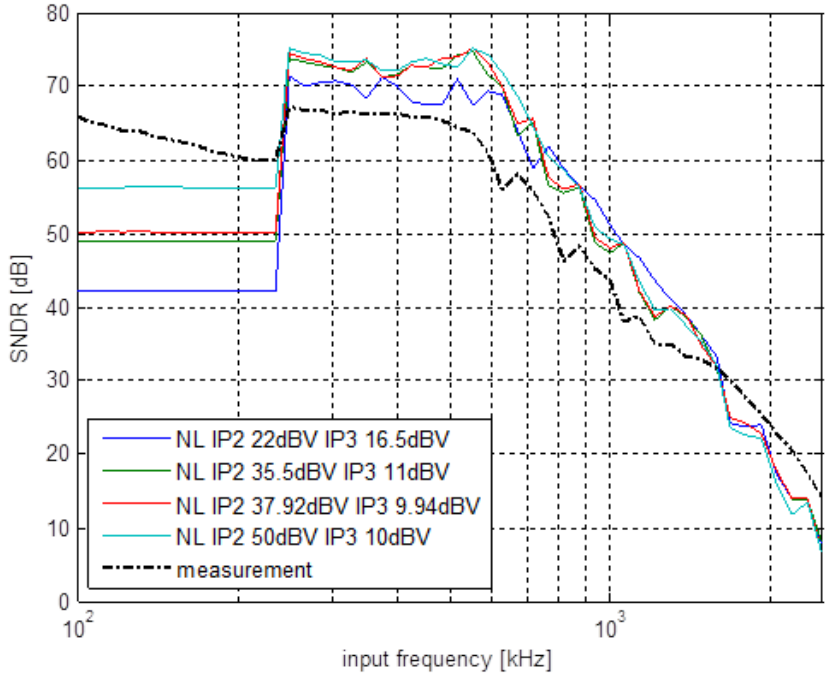


Figure 5.8: Frequency Sweep SNDR [dB]

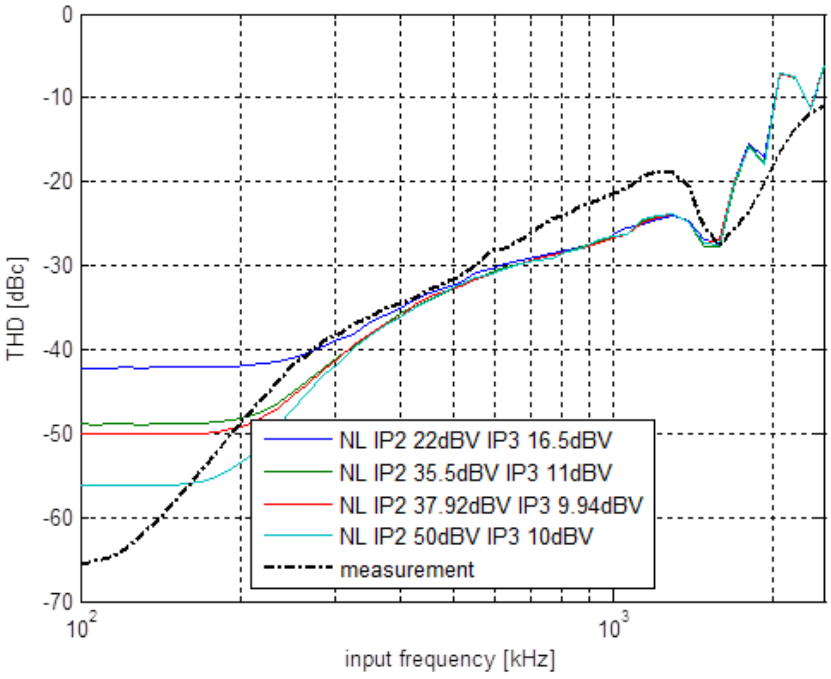


Figure 5.9: Frequency Sweep THD [dB]

5.3.3 Two Tone Scenarios

500 and 750kHz

Two tone scenarios, as done in the measurement section 4.1.5, are simulated in this subsection. In Fig. 5.10 the intermodulation distortion caused by two tones at 500 and resp. 750kHz at 250kHz is shown. The input level is increased linear and the intermodulation products at 250kHz are increasing with a slope of 2 following the theory of 2^{nd} order intermodulation distortion. The obtained measurement data is picturing a mixture of 2^{nd} and 3^{rd} order intermodulation distortion and has therefore a different slope compared to the simulation results. Simulation results obtained by only linear model and output saturation could not even model the trend of the intermodulation distortion. The simulated results are in most points more pessimistic than the measurement data and therefore better suited for simulation purposes.

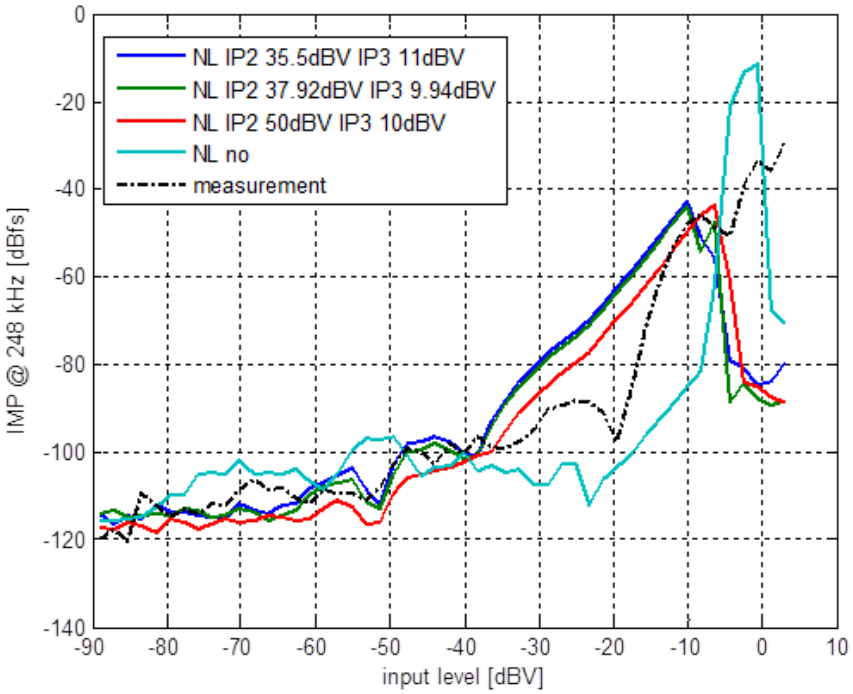


Figure 5.10: Intermodulation Distortion [dB], 250kHz

800 and 1200kHz

A similar picture is obtained for the 800 and 1200kHz scenario with an intermodulation product at 400kHz Fig. 5.11. Here again more optimistic simulation results compared to measurement results can be seen.

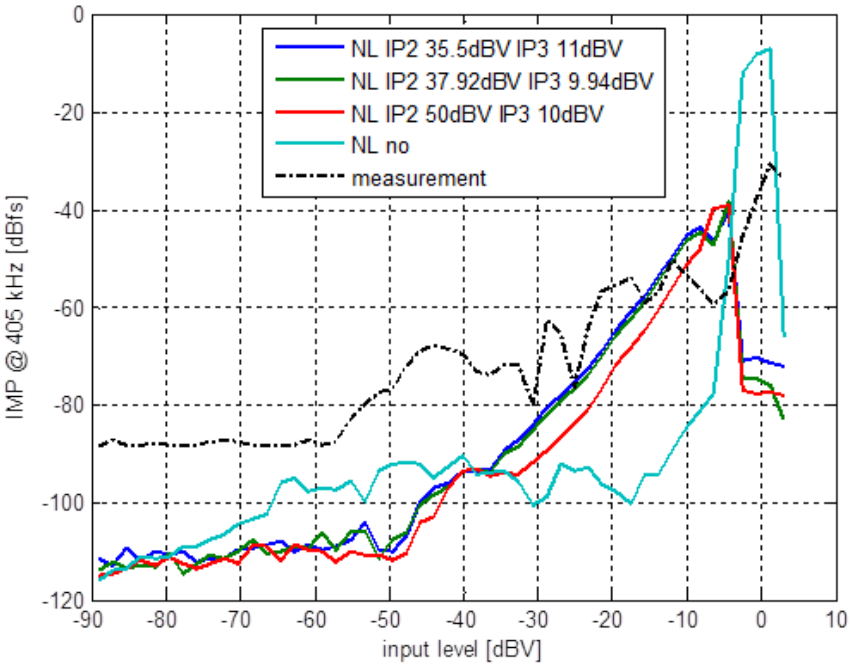


Figure 5.11: Intermodulation Distortion [dB], 400kHz

600 and 700kHz

In Fig. 5.12 the 2nd order intermodulation distortion from two tones at 600 and 700kHz is presented. Here the same could be stated as for Fig. 5.10. Fig. 5.13 is presenting the 3rd order intermodulation product of the above mentioned two tone scenario at 500kHz. In this figure the slope of 3 for a 3rd intermodulation product is in line with theory, and the measurement results are well covered by the obtained simulation results.

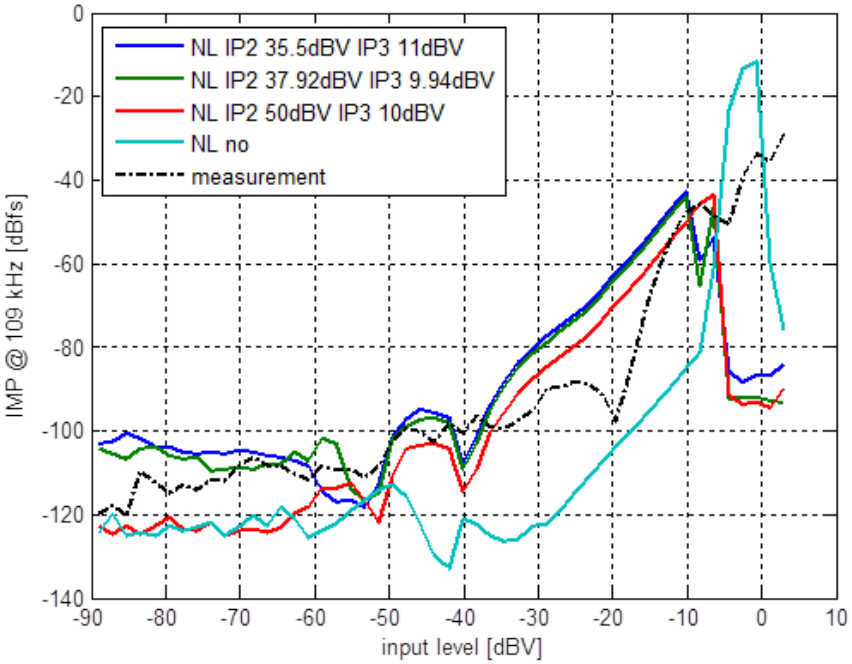


Figure 5.12: Intermodulation Distortion [dB], 100kHz

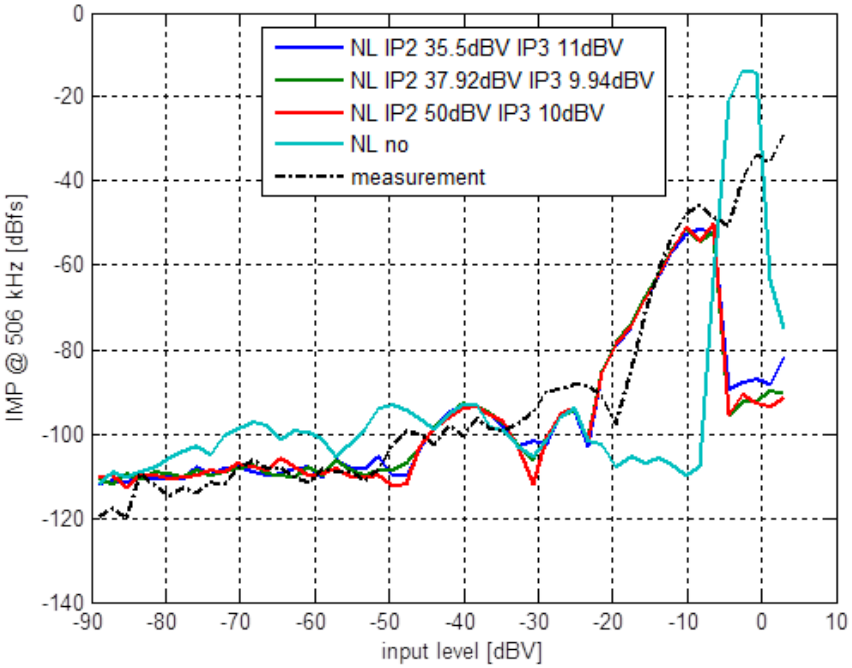


Figure 5.13: Intermodulation Distortion [dB], 500kHz

6 Conclusion and Outlook

The POLLUX testchip has been designed to work as a highly integrated transceiver platform for sensor, monitoring and security applications in an automotive environment. The transceiver has been built to work in a densely occupied RF spectrum. The communication is set up on a robust physical layer,thus a linear architecture is chosen. Some additional advantages of a linear architecture as lower energy consumption and less occupied area are described in Section 1.2.
Stringent conditions are taken in account for an ADC in such a linear receiver chain. In Chapter 2 an SD-ADC architecture is found to be a good choice for this type of application. These conditions are defined as specification parameters in Section 2.2. Furthermore these measures are described as it is found in literature, derived and resp. measured by this guidelines in Chapter 4. The implemented SD-ADC is found to be well designed according to specification. Some discrepancy is found with respect to linearity performance. This has been a known issue from a design review step.
Modelling aspects are concluding this work in Chapter 5. At first some general thoughts on the modelling approach are given in an introduction. The linear behavioural model of the integrated SD-ADC is derived in Section 5.1. To improve this linear model, a Hammerstein-Wiener model structure is introduced in Section 5.2. I.e. the linear model is extended by a non-linearity in the feedback path. The introduced Hammerstein-Wiener model is simulated with similar input parameters as the measurements have been done. A comparison of measurement data and simulation model results is given in Section 5.3. The obtained model parameters are found to represent the measured SD-ADC in a coarse way. It is a challenge to find a good behavioural model for an SD-ADC to represent its dynamic behaviour. The linear state space model introduced in this work represents the dynamic behaviour of the implemented SD-ADC quiet good. Even more challenging is finding a model picturing the nonidealities resp. non-linearities of a SD-ADC. This difficult task is covered in this work by the introduced Hammerstein-Wiener structure and namely by the polynomial non-linearity in the feedback path and the hard-saturation non-linearity at the output of the model structure. As found in the last section of this work, this task is hard to accomplish. The target to create a behavioural model for the integrated POLLUX SD-ADC by characterisation measurement results is not fully accomplished. The model is stated in Section 5.3 to account good for small scale input. It pictures also the harmonic and intermodulation behaviour very well for the target application area.
To model the mismatch in the digital-to-analog converter in the feedback path of the integrated SD-ADC more accurately, a deeper insight into the design would have been necessary. A more

optimal modelling approach would have been to model the mismatch in the feedback path by a random process model. The polynomial non-linearity model is not able to picture the mismatch correctly. This type of modelling approach is more useful to account for input nonidealities at the input of the model structure. The output of the model structure is found to be modelled pretty well as a saturation model.
The integrated POLLUX SD-ADC is characterized quite well. To get a more accurate and better behavioural model of the integrated SD-ADC the random process modelling approach, as shortly described above, should be targeted in further work.

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