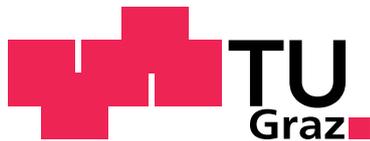


Switched Capacitor DC-DC Converter

Thomas Santa

Master's Thesis
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Institute of Electronics
University of Technology, Graz
Inffeldgasse 12
A-8010 Graz, Austria

Supervisor: DI Dr. Mario Auer

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Kurzfassung

Diese Arbeit präsentiert einen “Switched Capacitor DC-DC Converter”, der beim nominalen Ausgangsstrom von 30 mA einen Wirkungsgrad von 95% erreicht. Dieser ist als Abwärtswandler realisiert, welcher mit einer konstanten Eingangsspannung von 1,83 V versorgt wird und eine Ausgangsspannung von 1,2 V liefert. Die Ladung wird in zwei Phasen von der Eingangsquelle zum Ausgangskondensator transportiert. Dazu wird ein Netzwerk aus Schaltern und zwei sogenannten fliegenden Kondensatoren verwendet. Diese Art der Spannungswandlung ist in einer 65 nm low power CMOS Technologie implementiert und ist für den Einsatz in Mobiltelefonen vorgesehen. Das Ergebnis dieser Arbeit ist ein Testchip, welcher in Zusammenarbeit mit Infineon Technologies Austria AG erzeugt wurde. Der Testchip wurde im Labor vermessen und die theoretischen Erkenntnisse werden durch Messergebnisse im Labor bestätigt.

Abstract

This master's thesis presents a switched capacitor DC-DC converter, which supplies a nominal output current of 30 mA with an efficiency of 95%. A buck converter is implemented, which operates with a constant input voltage of 1.83 V and produces an output voltage of 1.2 V. The charge is transported in two phases from the input supply to the output capacitor. Therefore, a network consisting of switches and two so-called flying capacitors is used. This conversion technique is implemented in a 65 nm low power CMOS process and is intended to be used for mobile phones. The result of this master's thesis is a test chip, which was designed in collaboration with Infineon Technologies Austria AG. The test chip is evaluated in the lab and the measurement results confirm the theoretical findings.

Contents

1	Introduction	1
1.1	Task	1
1.2	Motivation	2
1.3	DC-DC Converters in General	2
1.4	Existing Solutions	4
2	Fundamentals	7
2.1	Efficiency	7
2.2	Charging a Capacitor	7
2.3	Basics of the Switch-Capacitor Network	9
	2.3.1 Common Mode	9
	2.3.2 Gain Mode	10
2.4	Switch Network	13
2.5	Non Overlapping Phases	14
2.6	Control Strategies	14
2.7	Switches	15
3	Implementation	17
3.1	Block Diagram	17
3.2	Capacitors	19
3.3	Resistive Voltage Divider	20
3.4	Voltage Comparator	22
3.5	Clock Manipulation Block	24
3.6	Start Up Block	26
3.7	Controller	27
3.8	Non Overlapping Phases	30
	3.8.1 Non Overlapping Phases with Buffer and Gates	30
	3.8.2 Asymmetrical Driver	30
3.9	Switch Network	31
3.10	Frequency	33
4	Simulation Results	35

4.1	Buffer	35
4.2	Resistive Voltage Divider	36
4.3	Voltage Comparator	37
4.4	Asymmetrical Drivers	38
4.5	Switches	39
4.6	Frequency	40
4.7	Switched Capacitor DC-DC Converter	42
	4.7.1 Ramp Up of the Power Supply	42
	4.7.2 Start Up	43
	4.7.3 Efficiency	43
	4.7.4 Transient Behavior	47
	4.7.5 Current Consumption	48
4.8	Conclusion of the Simulation Results	49
5	Layout and Test Chip	51
6	Measurements	53
	6.1 Test Board	53
	6.2 Measurement Results	54
	6.2.1 Efficiency for Different External Frequencies	55
	6.2.2 Efficiency for Different Output Currents	55
	6.2.3 Transient Behavior	57
7	Conclusion	59
8	Outlook	61
9	Appendix	63

Chapter 1

Introduction

1.1 Task

This master's thesis is part of an industry project with Infineon Technologies Austria AG. The task is to design a switched capacitor DC-DC converter in a 65 nm low power CMOS process. The buck converter is intended to be used in power management units for mobile phones. But there is no previous work in the power management unit department. The resulting test chip is designed from scratch.

Table 1.1: Electrical Characteristics

Parameter	Symbol	Values			Unit	Note Test Condition
		min.	typ.	max.		
Input voltage	V_{IN}	1.815	1.83	1.845	V	
Output voltage	V_{OUT}	1.145	1.2	1.255	V	
Absolute ripple	ΔV_{out}		TBD		mV	peak to peak
External frequency	f_{ext}		TBD		MHz	external clock
Efficiency	η		90		%	$I_{OUT}=30\text{ mA}$ $V_{IN}=1.83\text{ V}$
			TBD		%	$I_{OUT}=100\text{ mA}$ $V_{IN}=1.83\text{ V}$
			TBD		%	$I_{OUT}=200\text{ mA}$ $V_{IN}=1.83\text{ V}$
Start up time	t_{Start}			1	ms	
Start up current	I_{Start}			100	mA	$I_{OUT}=30\text{ mA}$

Table 1.1 gives an overview over the electrical characteristics of the test chip. The converter operates with a constant input supply of $1.83\text{ V} \pm 15\text{ mV}$. Typically, converters

have not a constant input voltage, since the voltage of a battery drops over time. A higher input voltage could be supported with adequate devices, which can handle the higher voltage. The process offers adequate devices for the given input voltage. The produced output voltage is $1.2\text{ V} \pm 55\text{ mV}$. The nominal output current is 30 mA and the required efficiency is 90% or higher. The converter supplies output currents up to 200 mA. The temperature range is from -20°C to $+125^\circ\text{C}$ with a nominal temperature of 85°C .

1.2 Motivation

Nowadays many people own mobile phones, PDAs or notebooks. The integration of functionality like camera, radio or wireless applications in such devices is increasing. All of them are battery powered devices and have a lot of integrated transistors which consume power. The standby time is a selling point and depends on the power consumption and the capacity of the battery. In order to provide a maximum standby or run time with a given battery, it is necessary to use appropriate strategies within the power management unit to keep power consumption as low as possible. Power down unused blocks, changing the clock frequency and provide adequate voltages are part of such strategies. The supply voltage V should be as low as possible because the power consumption P of a digital block depends strongly on the supply voltage:

$$P = V \cdot I = \frac{V \cdot Q}{T} = V^2 \cdot C_{mean} \cdot f \quad ,$$

whereby C_{mean} denotes the average capacitance, which is loaded in each period of frequency f . The power consumption is proportional to the square of the applied voltage. The voltage of a battery drops over time as charge is delivered, but electronic devices require almost a constant voltage. The challenge is to generate from a variable battery voltage a constant voltage for the power supply or to convert a constant voltage into another constant voltage and this as efficient as possible. Furthermore, a specified range of output current must be supported as well.

1.3 DC-DC Converters in General

Table 1.2 [9] gives an overview over three different power supply devices and their advantages and disadvantages. The differences between them are the used elements and the techniques to keep the output voltage in the specified range. If external components are needed, additional costs and area on the PCB (PCB = Printed Circuit Board) are required. Depending on the application and constraints like efficiency, cost, output ripple, EMI (EMI = Electro Magnetic Interference), load capability or transformation type, a compromise is necessary.

Table 1.2: Comparison of the Different Power Supply Devices [9]

	LDO	Charge Pump	Switching Regulator
Efficiency	Bad	Good	Best
Cost	Best	Moderate	Most expensive
Difficulty in Design	Easy	Moderate	Most difficult
PCB Area	Very small	Small	Large
Output Ripple	Very low	Moderate	Moderate
EMI	Very low	Low	Moderate
Load capability	Moderate	Moderate	Best
Transformation Type	Step down	Step up, step down, inverter	Step up, step down, inverter

LDO stands for Low Drop Out linear voltage regulator but is often used for all linear voltage regulators even if they have not a low drop out voltage. The efficiency η is slightly less than the ratio of output voltage to input voltage, because the control unit consumes power too [9]:

$$\eta \approx \frac{V_{OUT}}{V_{IN}} \quad . \quad (1.1)$$

The big disadvantage is the efficiency, as the ratio of output voltage to input voltage decreases. The cost is very low since only one small external capacitor is necessary. Even LDOs with no external capacitor are possible and so the required area on the PCB is very small. To supply low noise circuits with a constant output current, only analog controlled LDOs can be used because they have no voltage ripple on the output. The load capability depends on the application, mainly on the maximum power dissipation. The output voltage is always lower than the input voltage.

Switched capacitor DC-DC converter (charge pumps) can reach good efficiencies but with higher costs. External capacitors are required to support moderate output currents. The area on the PCB increases due to the external components. The big switches inside the chip consume a lot of area too. Depending on how the external capacitors are switched, a step up, step down or inverter can be build. The efficiency can be high, if the ratio of output to input voltage is similar to a gain, realizable with the flying capacitors [9]:

$$\eta \approx \frac{V_{OUT}}{V_{IN} \cdot \text{gain}} \quad . \quad (1.2)$$

The number of gains which can be realized depends on the number of external capacitors. An overview over the different gain configurations with three flying caps is given in [8].

Inductor based switching regulators consist of switches, a compensator and an output filter. The output filter is often made up of a capacitor and a coil. Efficiency up to 95 %

is possible. The design is difficult because the regulation is complex. The coil is almost always external since a good quality factor is beneficial for the efficiency. This costs area on the PCB and external components. High output currents can be supported and step up, step down and inverter can be realized.

1.4 Existing Solutions

Table 1.3 gives an overview over some existing solutions, including master's theses, commercial devices and one recent publication. The table provides information regarding type of conversion, input and output range, number of flying capacitors, output ripple at a certain output current, switching frequency, peak efficiency for a certain output current and the maximum output current.

The type of conversion is given by the requirements regarding input range and output range. Master's thesis [10] is an example for a switched capacitor DC-DC buck converter with a constant input voltage of 12 V. The converter presented in this work is a buck converter with a constant input voltage too. Figure 1.1 [10] depicts a typical efficiency vs. output current curve for a constant input voltage.

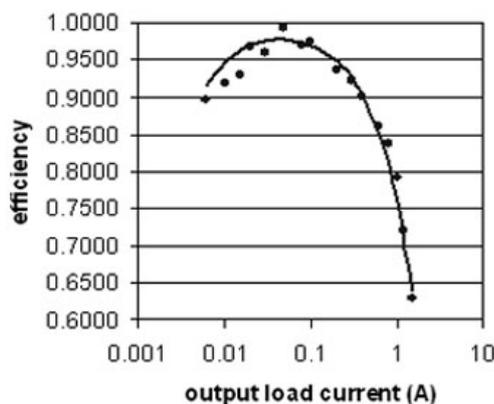


Figure 1.1: Typical Efficiency vs. Output Current Curve for a Constant Input Voltage [10]

Usually, the input voltage is supplied by a battery. This voltage drops during operation. Therefore, the input range is typically from 2.7 V to 5.5 V for the devices listed in table 1.3. Master's thesis [8] is a helpful introduction to switched capacitor DC-DC converter with a variable input voltage. It describes a possible implementation of a commercial device. Figure 1.2 [12] depicts the efficiency vs. input voltage of the LM2770 [12] for different output currents and shows which gain modes are applied. The converter described in this work is a buck converter which is supplied with a constant input voltage of 1.83 V and delivers a constant output voltage of 1.2 V.

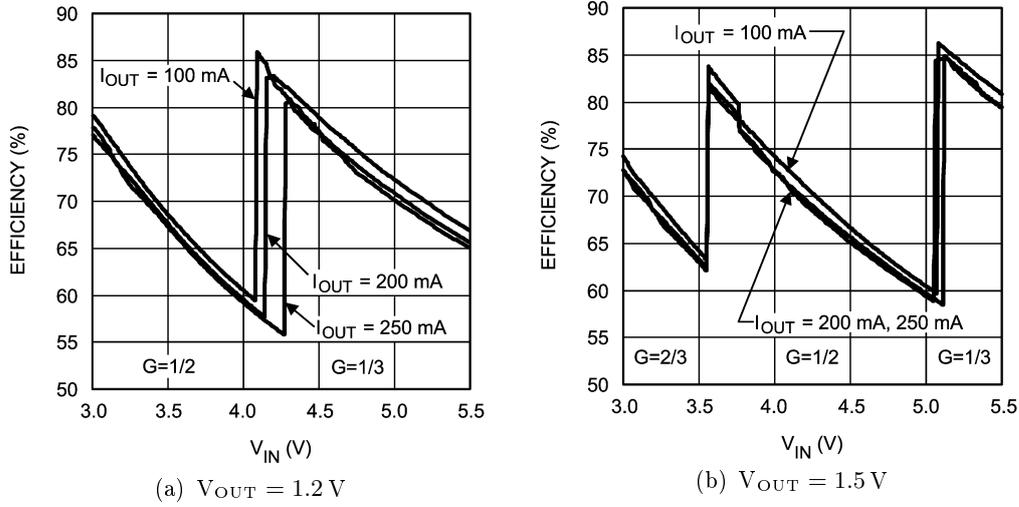


Figure 1.2: Typical Efficiency vs. Input Voltage Curve for Different Output Voltages and Output Currents with used Gain Configuration of LM2770 [12]

The capacitors of a switched capacitor DC-DC converter are typically MLCCs (= Multi-Layer Ceramic Capacitors), because the flying capacitors can become reverse-biased. A further advantage is the low ESR (ESR = Equivalent Series Resistor), which is beneficial regarding efficiency. The typical size of a flying capacitor is $1\mu\text{F}$. The size of the input capacitor covers typically a range from $1\mu\text{F}$ to $10\mu\text{F}$. The output capacitor is typically $10\mu\text{F}$ and covers a range from $4.7\mu\text{F}$ [13] to $24\mu\text{F}$ [10]. The size of the flying capacitors used in this project is $1\mu\text{F}$ and the input and output capacitors are $22\mu\text{F}$ each.

There are basically 2^n possibilities with n being the number of flying capacitors to connect them together [8]. The number of flying capacitors and the input and output range limit the applicable gain modes. The circuit [13] with one flying capacitor applies gain 1 and gain $1/2$. With two flying capacitors, gain $1/3$, gain $1/2$, gain $2/3$ and gain 1 can be applied. The circuit [14] with three flying capacitors applies gain $1/2$, gain $2/5$ and gain $1/3$. Circuit [6] can additionally work with a LDO conversion mode, if the gains give a lower efficiency. The converter presented in this master's thesis operates with two flying capacitors and applies gain $2/3$ and gain 1.

The ripple (peak-peak) of the output voltage depends on the size of the output capacitor, the output current and the switching frequency. The ripple of the output voltage increases as the output current increases, because more charge is removed from the output capacitor during one period. A big output capacitor is beneficial for a lower output ripple, since the voltage does not drop as much in a certain time as with a smaller capacitor. This time can be made shorter by increasing the switching frequency, which results in a lower output ripple as well. The typical range of the switching frequency is from 250 kHz [9] to 2 MHz [15].

Table 1.3: Comparison with Existing Solutions

Source	Type of Conversion	Input Range	Output Range	Flying Capacitors	Output Ripple	Switching Frequency	Peak Efficiency	Max. Output Current
Master's thesis [10]	buck	12V constant	1.5V, 1.8V, 2V	12 (0.47 μ F to 2.2 μ F)	100mV @1A	1MHz	98% for 50 mA	1.5 A
Master's thesis [8]	buck	2.7V to 5.5V	1.5V	2 \times 1 μ F	40mV @0.2A	1MHz	97% for 10 mA	200 mA
LM2770 [12]	buck	2.7V to 5.5V	1.2V, 1.5V, 1.575V	2 \times 1 μ F	25mV @0.2A	typ. 0.7MHz	85% for 100mA	250 mA
LM2788 [11]	buck	2.6V to 5.5V	1.5V, 1.8V, 2V	2 \times 1 μ F	20mV @0.12A	0.5MHz	90% for 10 mA	120 mA
LM2771 [13]	buck	2.7V to 5.5V	1.5V	1 \times 1 μ F	8mV @0.25A	1.1MHz	81% for 200 mA	250 mA
LM2772 [14]	buck	2.7V to 5.5V	1.2V	3 \times 1 μ F	8mV @0.15A	1.1MHz	80% for 150mA	150 mA
TPS60503 [6]	buck/boost, LDO mode	1.8V to 6.5V	1.5V, 1.8V, 3.3V	2 \times 1 μ F	30mV @0.15A	typ. 0.8MHz	90% for 50 mA	250 mA
LTC3251-1.5 [15]	buck	2.7V to 5.5V	1.2V, 1.5V	2 \times 1 μ F	15mV @50mA	typ. 1MHz	88% for 200 mA	500 mA
Paper [9]	buck/boost	2.9V to 5.5V	5V	2 \times 1 μ F	7mV @4mA	250kHz	88% for 4mA	48 mA
This master's thesis	buck	1.83V constant	1.2V	2 \times 1 μ F	5.6mV @30mA	0.5MHz (external)	97% for 10 mA	200 mA

Chapter 2

Fundamentals

This chapter explains the fundamentals of a switched capacitor DC-DC converter. It starts with the definition of the efficiency and explains why an efficiency of 100 % is not possible. Then, charging a capacitor will be discussed. Based on these findings, a strategy is presented to transport charge in two phases with a high efficiency. A therefore adequate switch–capacitor network is developed and the non overlapping switching of the two phases is described. The chapter ends with a discussion about switches.

2.1 Efficiency

The efficiency is defined as the ratio of output power to input power:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} \quad . \quad (2.1)$$

With ideal capacitors and ideal switches, according to equation 1.2, the theoretically reachable efficiency for a switched capacitor DC-DC converter could be 100 %. But due to the real components, the efficiency is always less than 100 %. The main power dissipations are coming from the capacitances of the drivers and switches, which need to be loaded and unloaded each time a switch turns on or off. Further, parasitic resistance in the connecting metal and bond wires, the ESR of the capacitors and the R_{ON} of the switches consume power. Finally, also the control unit consumes power.

2.2 Charging a Capacitor

Consider a circuit, where the capacitor C is charged via a resistor R by a source with the constant voltage V_0 . The time constant τ is the product of R and C . The voltage of

the capacitor at $t = 0$ is denoted as $v_{C(0)}$. Voltage and current of a capacitor are defined as [5]:

$$v_C(t) = (V_0 - v_{C(0)})\left(1 - e^{-\frac{t}{\tau}}\right) + v_{C(0)} \quad (2.2)$$

$$i_C(t) = I_0 \cdot e^{-\frac{t}{\tau}} = \frac{V_0 - v_{C(0)}}{R} \cdot e^{-\frac{t}{\tau}} \quad (2.3)$$

The energy transported to the capacitor can be calculated from equation 2.2 and 2.3 as follows:

$$\begin{aligned} W_C &= \int_0^{+\infty} v_C(t) \cdot i_C(t) dt \\ &= \int_0^{+\infty} \left(V_0 - V_0 \cdot e^{-\frac{t}{\tau}} + v_{C(0)} \cdot e^{-\frac{t}{\tau}} \right) \cdot \frac{V_0 - v_{C(0)}}{R} \cdot e^{-\frac{t}{\tau}} dt \\ &= V_0 \cdot \frac{V_0 - v_{C(0)}}{R} \cdot \int_0^{+\infty} e^{-\frac{t}{\tau}} dt - \frac{(V_0 - v_{C(0)})^2}{R} \cdot \int_0^{+\infty} e^{-\frac{2t}{\tau}} dt \\ W_C &= C \cdot (V_0 - v_{C(0)}) \cdot \left(V_0 - \frac{V_0 - v_{C(0)}}{2} \right) \quad (2.4) \end{aligned}$$

The energy dissipation in the resistor is given by:

$$\begin{aligned} W_R &= \int_0^{+\infty} v_R(t) \cdot i_R(t) dt \\ &= \int_0^{+\infty} R \cdot \frac{V_0 - v_{C(0)}}{R} \cdot e^{-\frac{t}{\tau}} \cdot \frac{V_0 - v_{C(0)}}{R} \cdot e^{-\frac{t}{\tau}} dt \\ &= \frac{(V_0 - v_{C(0)})^2}{R} \cdot \int_0^{+\infty} e^{-\frac{2t}{\tau}} dt \\ W_R &= (V_0 - v_{C(0)})^2 \cdot \frac{C}{2} \quad (2.5) \end{aligned}$$

If $v_{C(0)} = 0$, according to equation 2.4 and 2.5,

$$W_R = W_C = \frac{V_0^2 \cdot C}{2} \quad (2.6)$$

Equation 2.6 shows that 50% of the energy supplied by the source is transported to the capacitor. The rest of the energy is dissipated in the resistor, independent of the value of the resistor.

If $v_{C(0)} = \frac{3}{4} \cdot V_0$, the ratio of W_C to W_C+W_R is:

$$\frac{W_C}{W_C + W_R} = \frac{\left(V_0 - \frac{V_0 - \frac{3}{4} \cdot V_0}{2}\right)}{\left(V_0 - \frac{V_0 - \frac{3}{4} \cdot V_0}{2}\right) + \frac{1}{2} \cdot (V_0 - \frac{3}{4} \cdot V_0)} = \frac{7}{8} \quad . \quad (2.7)$$

Equation 2.7 emphasizes the fact that if the capacitor is precharged, more than 50% of the delivered energy is transported to the capacitor. In this case 87.5% of the delivered energy is transported to the capacitor and only 12.5% is dissipated in the resistor.

If $v_{C(0)} \rightarrow V_0$, the limit of the ratio of W_C to W_C+W_R is given by:

$$\lim_{v_{C(0)} \rightarrow V_0} \frac{W_C}{W_C + W_R} = \lim_{v_{C(0)} \rightarrow V_0} \frac{\left(V_0 - \frac{V_0 - v_{C(0)}}{2}\right)}{\left(V_0 - \frac{V_0 - v_{C(0)}}{2}\right) + \frac{1}{2} \cdot (V_0 - v_{C(0)})} = 1 \quad . \quad (2.8)$$

The limit in equation 2.8 shows that if $v_{C(0)} \rightarrow V_0$ and so the transported energy is infinitesimally small, this energy is transported to the capacitor and is not dissipated in the resistor.

Equation 2.7 and 2.8 emphasize that it is possible to transport most of the energy from the input supply to a capacitor, if this capacitor is charged and discharged only a little bit with respect to its static value. This is the key for a highly efficient switched capacitor DC-DC converter.

2.3 Basics of the Switch-Capacitor Network

To make use of the findings above, a network made of switches and so-called flying capacitors is applied to transfer charge from the input supply to the output capacitor. This happens in two phases. The two phases are referred to as “common mode” and “gain mode”. This sequence is referred to as one pump.

In the following, a switch-capacitor network is developed, which operates with one common mode and two different gain modes.

2.3.1 Common Mode

The first phase is referred to as common mode. Figure 2.1 depicts how the flying capacitors are connected during common mode. The flying capacitors are charged to the difference between input voltage and output voltage $V_{IN}-V_{OUT}$. Charge is stored on the flying capacitors.

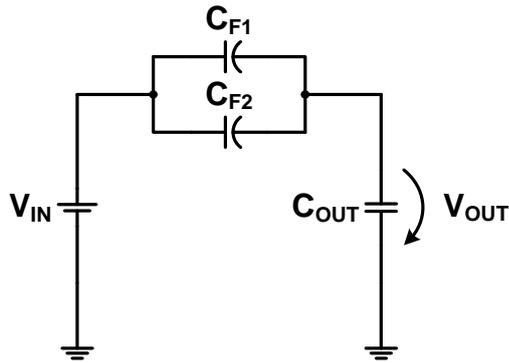


Figure 2.1: Applied Common Mode in this Converter

2.3.2 Gain Mode

The second phase is referred to as gain mode. The flying capacitors are connected to the output capacitor to deliver the charge, stored in the previous common mode phase. The capacitors can be combined with the input supply or among each other. Depending on the combination, different gain modes can be achieved. Figure 2.2 depicts gain 2/3 and gain 1, which are applied in this converter.

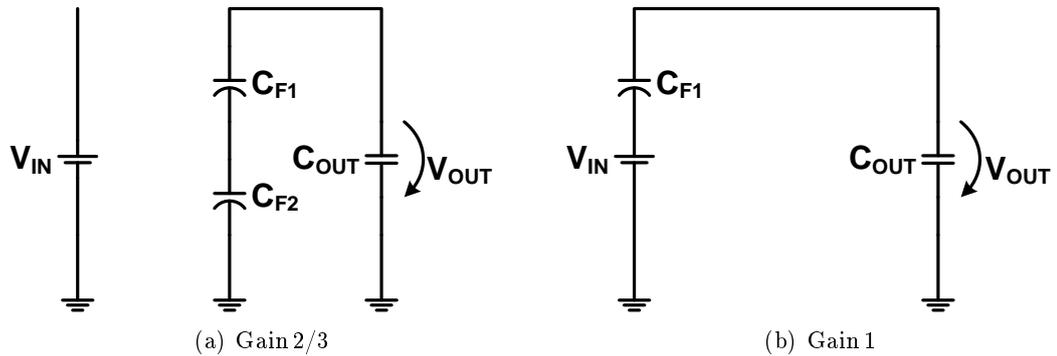


Figure 2.2: Applied Gain Modes in this Converter

Gain 2/3

The flying capacitors are connected in series to the output capacitor as shown in figure 2.2(a). The flying capacitors were charged to $V_{IN} - V_{OUT}$ and deliver now the charge to the output capacitor as long a voltage difference is given. As the output voltage is equal to the voltage of the two flying capacitors in series, no more charge is transported. When pumping with gain 2/3, the output voltage will converge to 2/3 of the input voltage.

Starting with gain 2/3, V_{OUT} is given by:

$$V_{OUT}(n) = \frac{Q_{OUT} + Q_F}{C_{OUT} + \frac{C_F}{2}} .$$

When switching from gain 2/3 to common mode, according to the superposition principle, $V_{OUT}(n + \frac{1}{2})$ is the sum of $V_{OUT}(n)$ and the result of the voltage divider:

$$V_{OUT}\left(n + \frac{1}{2}\right) = V_{OUT}(n) + \frac{2 \cdot C_F}{2 \cdot C_F + C_{OUT}} \left(V_{IN} - \underbrace{\left(V_{OUT}(n) + \frac{V_{OUT}(n)}{2} \right)}_{=\frac{3}{2} \cdot V_{OUT}} \right) . \quad (2.9)$$

At the end of phase gain 2/3, the charge stored in the capacitors is given by:

$$Q_{OUT}\left(n + \frac{1}{2}\right) = C_{OUT} \cdot V_{OUT}\left(n + \frac{1}{2}\right)$$

$$Q_{F1}\left(n + \frac{1}{2}\right) = Q_{F2}\left(n + \frac{1}{2}\right) = C_F \cdot \left(V_{IN} - V_{OUT}\left(n + \frac{1}{2}\right) \right) .$$

When switching from common mode to gain 2/3, according to the charge conservation theory, $V_{OUT}(n+1)$ is:

$$V_{OUT}(n+1) = \frac{C_{OUT} \cdot V_{OUT}\left(n + \frac{1}{2}\right) + C_F \cdot \left(V_{IN} - V_{OUT}\left(n + \frac{1}{2}\right) \right)}{C_{OUT} + \frac{C_F}{2}} . \quad (2.10)$$

Substituting $V_{OUT}(n + \frac{1}{2})$ in equation 2.9 with equation 2.10 gives:

$$V_{OUT}(n+1) \cdot \left(C_{OUT} + \frac{C_F}{2} \right) = V_{OUT}(n) \left(C_{OUT} - C_F - \right.$$

$$\left. (C_{OUT} - C_F) \cdot \frac{2 \cdot C_F}{2 \cdot C_F + C_{OUT}} \cdot \frac{3}{2} \right) +$$

$$V_{IN} \left(C_F + (C_{OUT} - C_F) \cdot \frac{2 \cdot C_F}{2 \cdot C_F + C_{OUT}} \right) .$$

Now, the Z -transformation can be applied:

$$V_{OUT}(z) = \frac{z}{z-1} \cdot V_{IN} \cdot \quad (2.11)$$

$$\frac{C_F + (C_{OUT} - C_F) \cdot \frac{2 \cdot C_F}{2 \cdot C_F + C_{OUT}}}{z \left(C_{OUT} + \frac{C_F}{2} \right) + \left(-C_{OUT} + C_F + (C_{OUT} - C_F) \cdot \frac{2 \cdot C_F}{2 \cdot C_F + C_{OUT}} \cdot \frac{3}{2} \right)} .$$

According to the finite value theorem, equation 2.11 is multiplied with $(1 - z^{-1})$ and $z \rightarrow 1$ results:

$$\begin{aligned} \lim_{n \rightarrow \infty} V_{OUT}(n) &= \lim_{z \rightarrow 1} (1 - z^{-1}) \cdot \frac{z}{z-1} \cdot V_{IN} \cdot \frac{C_F + (C_{OUT} - C_F) \cdot \frac{2 \cdot C_F}{2 \cdot C_F + C_{OUT}}}{\frac{3}{2} \cdot C_F + (C_{OUT} - C_F) \cdot \frac{2 \cdot C_F}{2 \cdot C_F + C_{OUT}} \cdot \frac{3}{2}} \\ \lim_{n \rightarrow \infty} V_{OUT}(n) &= \frac{2}{3} \cdot V_{IN} \quad . \end{aligned} \quad (2.12)$$

Gain 1

In gain 1, the flying capacitor C_{F1} is connected as shown in figure 2.2(b). The main principle is the same as above. When pumping with gain 1, the voltage of the output capacitor will converge to the input voltage. The flying capacitor C_{F2} is not needed.

At the end of phase gain 1, V_{OUT} is according to the superposition principle given by:

$$V_{OUT}\left(n + \frac{1}{2}\right) = V_{OUT}(n) + \frac{C_F}{C_F + C_{OUT}} (V_{IN} + V_F(n) - V_{OUT}(n)) \quad . \quad (2.13)$$

At the end of phase common mode, V_{OUT} is given by:

$$V_{OUT}(n+1) = V_{OUT}\left(n + \frac{1}{2}\right) + \frac{C_F}{C_F + C_{OUT}} \left(V_{IN} - V_F\left(n + \frac{1}{2}\right) - V_{OUT}\left(n + \frac{1}{2}\right) \right) \quad . \quad (2.14)$$

Inserting in this equation 2.13 gives:

$$\begin{aligned} V_{OUT}(n+1) &= V_{OUT}(n) + \frac{C_F}{C_F + C_{OUT}} (V_{IN} + V_F(n) - V_{OUT}(n)) + \\ &\quad \frac{C_F}{C_F + C_{OUT}} (V_{IN} - V_F\left(n + \frac{1}{2}\right) - V_{OUT}(n) + \\ &\quad \frac{C_F}{C_F + C_{OUT}} (V_{IN} + V_F(n) - V_{OUT}(n))) \\ V_{OUT}(n+1) &= V_{OUT}(n) \cdot \left(1 - 2 \frac{C_F}{C_F + C_{OUT}} - 2 \left(\frac{C_F}{C_F + C_{OUT}} \right)^2 \right) + \\ &\quad V_{IN} \cdot \left(2 \frac{C_F}{C_F + C_{OUT}} + 2 \left(\frac{C_F}{C_F + C_{OUT}} \right)^2 \right) \quad . \end{aligned}$$

Applying the Z -Transformation gives:

$$\begin{aligned} z^1 \cdot V_{OUT}(z) &= z^0 \cdot V_{OUT}(z) \cdot (\dots) + \frac{z}{z-1} \cdot V_{IN} \cdot (\dots) \\ V_{OUT}(z) &= \frac{z}{z-1} \cdot V_{IN} \cdot \frac{2 \frac{C_F}{C_F + C_{OUT}} + 2 \left(\frac{C_F}{C_F + C_{OUT}} \right)^2}{z-1 + 2 \frac{C_F}{C_F + C_{OUT}} + 2 \left(\frac{C_F}{C_F + C_{OUT}} \right)^2} \quad . \end{aligned}$$

The finite value theorem yields:

$$\lim_{n \rightarrow \infty} V_{OUT}(n) = \lim_{z \rightarrow 1} (1 - z^{-1}) \cdot V_{OUT}(z) = V_{IN} \quad . \quad (2.15)$$

Equation 2.12 and 2.15 show that the output voltage converges to $2/3 V_{IN}$ and V_{IN} respectively.

2.4 Switch Network

Figure 2.3 depicts the switch-capacitor network, which results from figure 2.1, 2.2(a) and 2.2(b). Table 2.1 gives the according switch configurations for common mode, gain $2/3$ and gain 1, whereby “1” denotes a conducting and “0” a non conducting switch.

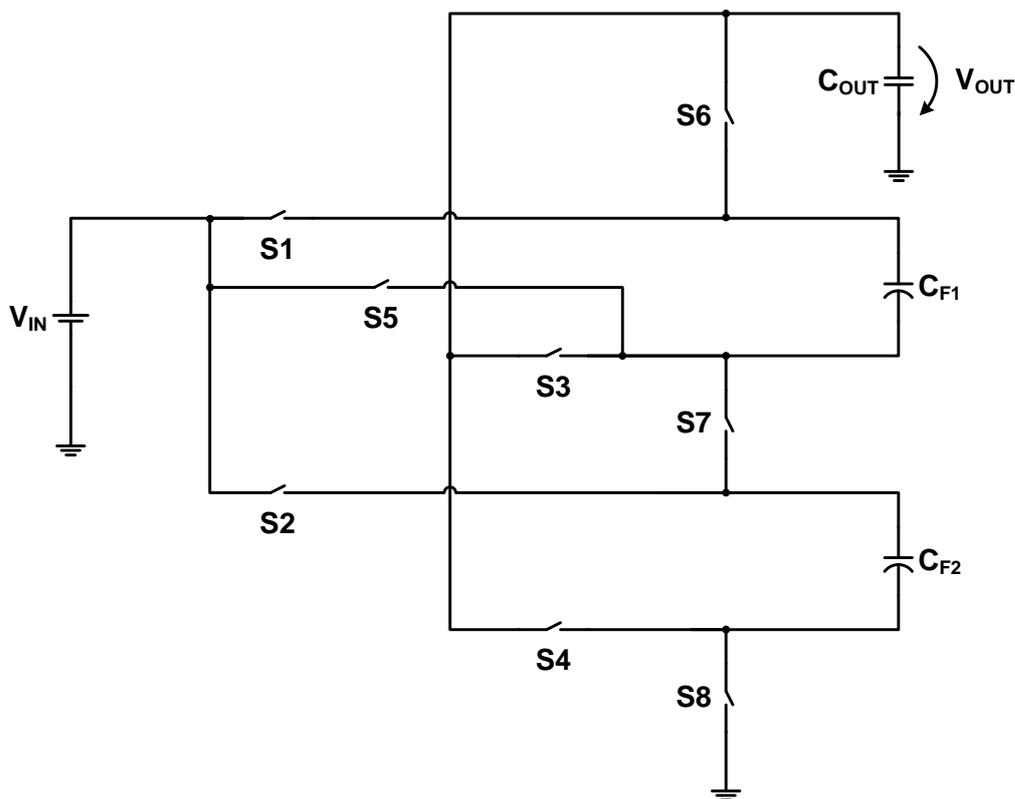


Figure 2.3: Simplified Switch Network to Transport Charge in Two Phases with Flying Capacitors from the Input Supply to the Output Capacitor

Table 2.1: Switch Configuration for Common Mode, Gain2/3 and Gain 1

	S1	S2	S3	S4	S5	S6	S7	S8
Common Mode	1	1	1	1	0	0	0	0
Gain2/3	0	0	0	0	0	1	1	1
Gain 1	0	0	0	0	1	1	0	0

2.5 Non Overlapping Phases

The switch network operates in two phases. It is important to have a non overlapping phases, because by turning the switches on and off simultaneously, there is a short time where a critical path exists. This is a low ohmic path from the input to the output, from the input to ground or from the output to ground. In this time a so-called shoot through current flows. This current is given by the sum of the R_{ON} in the critical path and the according voltage drop. This has a major impact on the efficiency. Figure 2.4 depicts an appropriate timing of the two phases. The non overlapping time must be long enough so that first all transistors in the critical paths can turn off before the other transistors turn on. This delay between the two phases is essential to avoid shoot through current.

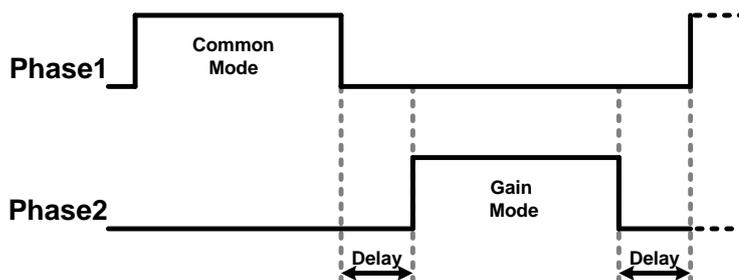


Figure 2.4: Non Overlapping Phases to Avoid Shoot Through Current

2.6 Control Strategies

There are different strategies to control the output voltage. Thereby, different parameters like the applied gain or the switching frequency can be varied. Another strategy is to pump or not to pump, just as required.

- PFM: The Pulse Frequency Modulation varies the pumps which deliver charge to the output capacitor. If the output voltage is high enough, no more pumps are performed and so no more charge is delivered to the output capacitor. If the output voltage of the output capacitor falls under a certain level, the circuit continues to pump and delivers charge to the output.

- **Gain Switching:** The circuit can switch between different gain modes to support different output currents. The circuit described in this work applies gain 2/3 and gain 1, as described in section 2.3. Gain 2/3 can deliver charge to the output highly efficient due to the specified ratio of output voltage to input voltage. But if the output current increases, the output voltage drops and gain 2/3 is not able to keep the output voltage in specification. Then, the circuit switches to gain 1, which can deliver more charge to the output but with lower efficiency. The circuit tries to work as long as possible with gain 2/3 and switches only if really necessary to gain 1. If the output voltage is higher than 1.2 V, then the circuit performs no pumps.
- **VCO:** A Voltage Controlled Oscillator can be use to control the output voltage. As the output voltage falls, the pumping frequency is increased in order to deliver more charge to the output capacitor. The frequency can vary only in a certain range. If the frequency gets to high, the switching losses begin to dominate. This strategy is not implemented in this work.

2.7 Switches

The flying capacitors and the output capacitor are connected by switches, which are realized by CMOS transistors. The drain current I_D of a transistor in the ohmic region defined by the square law model is given by following equation [2]:

$$I_D = K' \frac{W}{L} \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right] . \quad (2.16)$$

The square law model is not accurate for the applied technology, but is used to describe basically the properties of a transistor. In terms of load capability, the resistance of the switches should be as low as possible. To keep R_{ON} low, the transistor has to be made wide and short. The R_{ON} can be calculated from equation 2.16:

$$R_{ON} = \left(\frac{\delta I_D}{\delta V_{DS}} \right)^{-1} = \frac{1}{K' \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})} . \quad (2.17)$$

As the area of the gate is increased to reduce R_{ON} , the capacitance of the gate is increased. The transistor is in the ohmic region. The gate-source, the gate-drain and the gate-bulk capacitances have to be considered, whereby C_{OX} denotes the oxide capacitance and C_{GBO} denotes the gate-bulk-overlap capacitance [3]:

$$C_{gs} = C_{gd} = \frac{W \cdot L \cdot C_{OX}}{2} , \quad C_{gb} = C_{GBO} \cdot L .$$

These capacitances need to be charged or discharged each time the transistor is turned on or off. The drivers that charge and discharge the gates of the switches have also wide

gates, since they need to turn on and off the switches quickly. Also those capacitances need to be charged and discharged and this costs power. At a certain point, increasing the width does not help to increase the efficiency since the power dissipation in the gate overbalance the lower conduction losses of R_{ON} . Finally, a trade off between area and R_{ON} is done, since increasing the area gains only little and costs a lot of money.

Chapter 3

Implementation

This chapter presents the implementation of the switched capacitor DC-DC converter. The chapter starts with the block diagram. It gives an overview over the single components like the external capacitors, the switch network, the drivers, the controller, the voltage comparator and the resistive voltage divider. The implementation issues of the components are discussed.

3.1 Block Diagram

Figure 3.1 depicts the block diagram of the implemented switched capacitor DC-DC converter. The converter consists mainly of a switch network, drivers, a digital controller, a resistive voltage divider and three voltage comparators. Furthermore, a start up circuit and a clock manipulation circuit are implemented.

The switch network connects the two flying capacitor as described in section 2.3, so that they can deliver charge in two phases from the input supply to the output capacitor. The switch network operates with non overlapping phases, as described in section 2.5. Therefore, asymmetrical drivers are used which delay the turning on signal and propagate fast the turning off signal. The drivers are controlled by a digital controller. The controller operates with two different gain modes, depending on the output of the voltage comparators as described later in section 3.7. The controller can be enabled and disabled using the enable signal. The IDDQ signal is used to perform an IDDQ test. The test signal is used to select which internal signals are monitored at the three test outputs. Either the output of the three flip flops, which define the internal state of the finite state machine or the output of the three comparators can be monitored. The controller is clocked by a clock manipulation circuit. This circuit can manipulate the clock to react faster, if the comparators for the upper or lower limit trigger. The controller enables and disables the start up circuit. The start up circuit uses a current source to precharge the output capacitor during the start up phase.

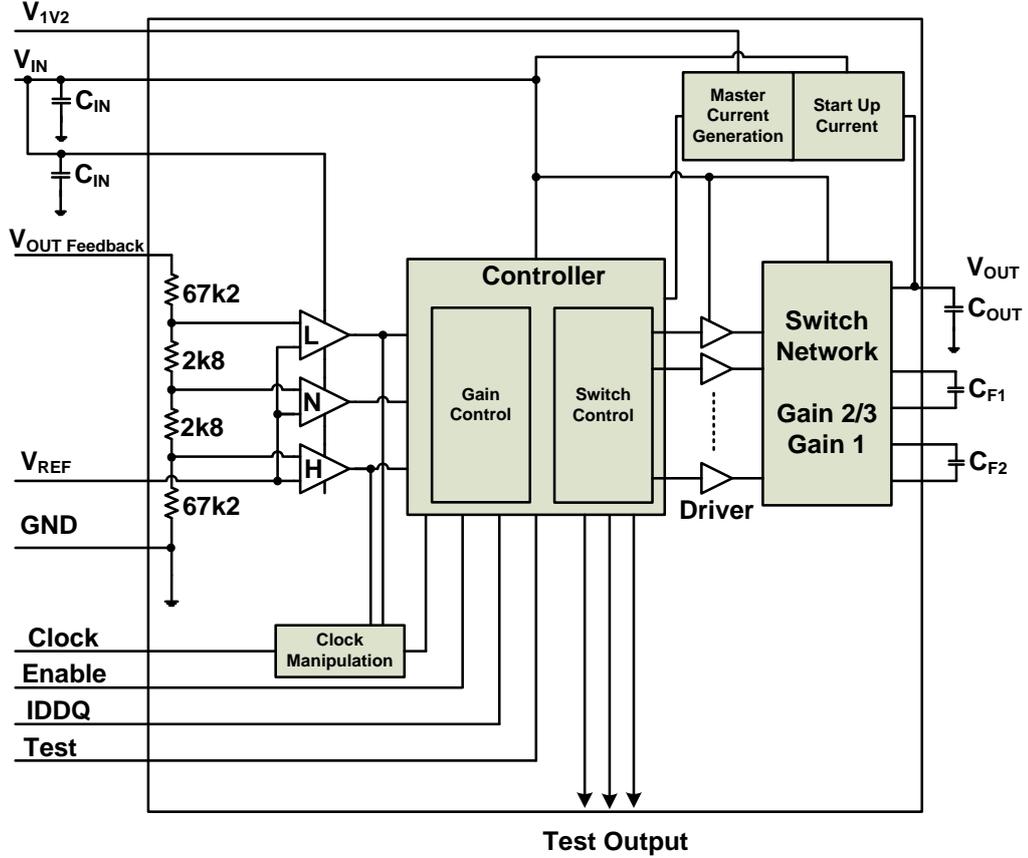


Figure 3.1: Block Diagram of the Switched Capacitor DC-DC Converter

$V_{OUT\text{ Feedback}}$ is supposed to be connected externally to the output capacitor to sense V_{OUT} and is divided by a resistive voltage divider. The comparators compare the external applied reference voltage V_{REF} of 0.6 V with the divided voltage $V_{OUT\text{ Feedback}}$. Comparator *H* (*High*) detects the upper level, which is 5 mV under the upper specified output voltage limit. Comparator *N* (*Nominal*) detects the nominal level of 1.2 V and comparator *L* (*Low*) detects the lower level, which is 9 mV above the lower specified output voltage limit.

The subcircuit, which generates the master current for the start up circuit, has an extra external power supply of 1.2 V. This power supply is only needed during start up and has no impact on the efficiency.

The input supply is buffered by input capacitors C_{IN} in order filter high current peaks caused by switching. The power supply for the analog and the digital part is separately, because the digital controller, the drivers and the switches produce noise on the power supply. This can influence the performance of the comparators in an undesired manner.

3.2 Capacitors

Switched capacitor DC-DC converters transfer the energy using capacitors. Therefore, the right selection of the capacitors is important. MLCCs are adequate for external capacitors. They have a small footprint and require only little area on the PCB. MLCCs have a low ESR and a low ESL (= Equivalent Series Inductance). The capacitance of X7R or X5R capacitors varies about 10%. The variation over temperature is about 15% from -55°C to $+125^{\circ}\text{C}$.

Input and output capacitors are ceramic capacitors with a low ESR. A higher ESR increases the ripple of the output voltage. To reduce ESR, two capacitors can be placed in parallel. This is beneficial for the ripple, if the capacitors have a different load response. The ripple caused by switching can be reduced by increasing the capacitance of the input and output capacitors. The input capacitor provides charge for the flying capacitors, as they are connected to the input, whereby charge is transferred quickly. Polarized capacitors must not be used as flying capacitors, since they can be reversed biased, if gain 1 is applied. The size of the flying capacitors impacts the load capability and the ripple of the input and output voltage.

As explained above, a big output capacitor is beneficial for the ripple of the output voltage. $C_{OUT\max}$ can be calculated, based on t_{start} and I_{start} , given in table 1.1 and $V_{OUT\min}$, calculated in equation 3.3. The output voltage increases, as the slave transistor of the current mirror charges the output capacitor. Thereby, V_{DS} of this transistor is reduced. This reduces the average provided start current. The provided current can change with different technology parameters. Therefore, the maximal available start current to load C_{OUT} (30 mA output current) is assumed to be 50 mA. The output voltage must trigger comparator L in order that the circuit starts to pump. This level is theoretically 1.154 V.

$$C_{OUT\max} = \frac{I'_{Start\max}}{V'_{OUT\min} \cdot t_{Start}} = \frac{50mA}{1.154V \cdot 1ms} = 43.3\mu F \quad (3.1)$$

$C_{OUT\text{nom}}$ is chosen to be 22 μF . The input capacitor is equal to the output capacitor. The flying capacitors are 1 μF . All external components are listed in table 3.1:

Table 3.1: External Components

Parameter	Symbol	Values			Unit	Note Test Condition
		min.	typ.	max.		
Output Capacitor	C_{OUT}	-35%	22	+35%	μF	External
C_{OUT} ESR	$\text{ESR}(C_{OUT})$			50	$\text{m}\Omega$	1MHz...10MHz
Input Capacitor	C_{IN}	-35%	22	+35%	μF	External
C_{IN} ESR	$\text{ESR}(C_{IN})$			50	$\text{m}\Omega$	1MHz...10MHz
Flying Capacitor	C_F	-35%	1	+35%	μF	External
C_F ESR	$\text{ESR}(C_F)$			25	$\text{m}\Omega$	1MHz...10MHz

3.3 Resistive Voltage Divider

The output voltage is divided using a resistive voltage divider. It consists of unit resistors to provide a good matching. The value of the resistor is mainly defined by the length, the width and the sheet resistance. The length has to dominate the width, so that the value of the resistor is mainly defined by the length and not by the inaccurately matching contacts to metal. To size the unit resistor, a compromise is necessary: The voltage divider should consume only little current. Therefore, the value of the unit resistor has to be big. On the other hand, the resistor and the gate capacitance of the following voltage comparator build an RC-delay. This delay has to be small in order to detect fast transitions of the output voltage. Thereby, the maximum steepness of $V_{OUT\ Feedback}$ is given by $C_{OUT\ min}$ and $I_{OUT\ max}$:

$$\frac{\Delta V_{OUT\ max}}{\Delta t} = \frac{I_{OUT\ max} \cdot \Delta t}{C_{OUT\ min}} = \frac{-0.2A \cdot 1\mu s}{14.3\mu F} = -14mV/\mu s \quad . \quad (3.2)$$

Figure 3.2 depicts the implemented resistive voltage divider. The resolution of the resistive voltage divider is defined by the unit resistors. The desired levels, resulting from the resistive voltage divider, have to fit in this resolution. Finally, the size of the unit resistor is $5.6\text{ k}\Omega$. A ladder with 50 resistors with a size of $2.8\text{ k}\Omega$ is implemented, whereby two unit resistors are placed in parallel. Additionally, a NMOS transistor is used to avoid current flowing through the resistive voltage divider during an IDDQ test. The R_{ON} of the NMOS transistor is low, so that the impact to the trigger levels for the comparators is negligible.

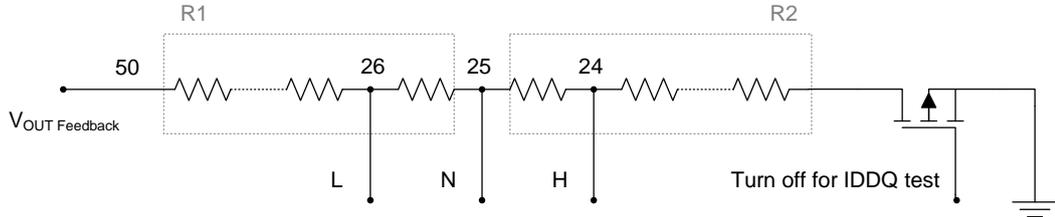


Figure 3.2: Resistive Voltage Divider consisting of 50 Resistors, each $2.8\text{ k}\Omega$

The taps for the input voltage of the comparators are at position 24, 25 and 26 and give following trigger levels of V_{OUT} :

$$V_{OUT\ L} = V_{REF} \cdot \frac{R_{total}}{R_L} = 0.6V \cdot \frac{50 \cdot 2.8k\Omega}{26 \cdot 2.8k\Omega} = 1.154V \quad (3.3)$$

$$V_{OUT\ N} = V_{REF} \cdot \frac{R_{total}}{R_N} = 0.6V \cdot \frac{50 \cdot 2.8k\Omega}{25 \cdot 2.8k\Omega} = 1.2V \quad (3.4)$$

$$V_{OUT\ H} = V_{REF} \cdot \frac{R_{total}}{R_H} = 0.6V \cdot \frac{50 \cdot 2.8k\Omega}{24 \cdot 2.8k\Omega} = 1.25V \quad . \quad (3.5)$$

For the design, the impact of the mismatch on the trigger levels has to be considered. The standard deviation of a resistor for 1σ is given in equation 3.6. The matching of the resistors is inversely proportional to the area of the resistor. The matching parameter for the resistor is $A_{\Delta R/\langle R \rangle}$ [% μm]. The units for W and L are μm .

$$\sigma_{\Delta R/\langle R \rangle} = \frac{A_{\Delta R/\langle R \rangle}}{\sqrt{W \cdot L}} \quad . \quad (3.6)$$

3σ equates to 99.7% and is therefore sufficient for a test chip. The impact of the matching for a 3σ design on tap 25 is calculated in the following:

$$\begin{aligned} 3 \cdot \sigma_{\Delta R/\langle R \rangle} &= \frac{3 \cdot A_{\Delta R/\langle R \rangle}}{\sqrt{W \cdot L}} \\ &= 0.18\% \quad . \end{aligned} \quad (3.7)$$

The voltage at tap 25 depends on R_1 and R_2 (see figure 3.2) as follows:

$$V_{25} = V_{\text{OUT Feedback}} \cdot \frac{R_1}{R_1 + R_2} \quad .$$

The impact of the matching of R_1 and R_2 is given by:

$$\begin{aligned} \Delta V_{25} &= \frac{\partial V_{25}}{\partial R_1} \Delta R_1 + \frac{\partial V_{25}}{\partial R_2} \Delta R_2 \\ &= \left| V_{\text{OUT Feedback}} \cdot \frac{(R_1 + R_2) - R_1}{(R_1 + R_2)^2} \Delta R_1 \right| + \left| V_{\text{OUT Feedback}} \cdot \frac{-R_1}{(R_1 + R_2)^2} \Delta R_2 \right| \\ &= V_{\text{OUT Feedback}} \cdot \frac{R_2}{(R_1 + R_2)^2} \Delta R_1 + V_{\text{OUT Feedback}} \cdot \frac{R_1}{(R_1 + R_2)^2} \Delta R_2 \quad . \end{aligned} \quad (3.8)$$

At tap 25, R_1 is equal R_2 . The error e_{RVD} of the resistive voltage divider, caused by mismatch is according to equation 3.7 and 3.8 given by:

$$\begin{aligned} e_{RVD} = \Delta V_{25} &= V_{\text{OUT Feedback}} \cdot \frac{(2R)}{(2R)^2} \Delta R \\ &= \frac{1.2V}{2} \cdot 0.0018 \\ e_{RVD} &= 1.08mV \quad . \end{aligned} \quad (3.9)$$

According to equation 3.9 is the error caused by mismatch at tap 25 for a 3σ design 1mV.

3.4 Voltage Comparator

The voltage comparator compares the resulting voltages coming from the resistive voltage divider with a reference voltage of 0.6 V. Figure 3.3 depicts the voltage comparator, which consists of a preamplification circuit, a decision circuit, a postamplification circuit ([4], p. 910) and a bias circuit.

The preamplification circuit consists of three fully differential pairs with diode load. They are symmetrically and have therefore no inherent offset. The offset caused by mismatch of the transistors is mainly coming from the first differential pair of the preamplification circuit. The influence of the mismatch to the offset caused by the following stages is reduced by the gains of the previous stages. The gain of one fully differential pair with diode load is low (6 dB to 10 dB). Therefore, three stages are used to amplify the difference of the input signals and to reduce kickback by the product of the gains of each stage. Kickback occurs due to capacitive coupling back to the input, caused by the fast switching decision circuit. The decision circuit is a simple CMOS OTA, which does the differential to single conversion. The simple CMOS OTA is not symmetrical and has therefore an inherent offset. The preamplification circuit amplifies the signal, so that the offset of the OTA has a negligible impact. The postamplification circuit consists of a Schmitt trigger ([4], p. 524) and an inverter. This circuit is used to convert the analog output signal of the OTA into the digital signal. The biasing, and so the voltage comparator, can be turned on and off by the enable signal. The postamplification circuit and the bias circuit are reused from an existing project.

The comparator has a low offset voltage, low current consumption and is fast. It is important to have a low offset voltage in order to compare accurately the resulting voltages of the resistive voltage divider. This is especially important for comparator L which triggers, if the output voltage is near to the lower specified limit. The offset voltage defines also the minimum resolution. Offset is mainly introduced by the mismatch of the differential pair of the first stage. The offset voltage of one stage is the voltage which needs to be applied to the input of a differential pair, so that the resulting output voltages are equal. If the loads (diode loads) match perfectly, then the offset voltage is the needed differential voltage so that the currents I_D in both transistors are the same. The transistors are typically in saturation and I_D is therefore given by:

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \quad \text{with} \quad \beta = K' \frac{W}{L} \quad .$$

Thereby, mismatch is introduced by K' , W , L and V_T . The offset voltage V_{OS} for a differential pair with resistive load is given by [2]:

$$V_{OS} = \Delta V_T + \frac{V_{GS} - V_T}{2} \left(-\frac{\Delta\beta}{\beta} - \frac{\Delta R}{R} \right) \quad \text{with} \quad \frac{g_m}{I_D} = \frac{2}{V_{GS} - V_T} \quad .$$

Based on the findings above, the differential pairs are designed with a high g_m over I_D , which is equal to a low $V_{GS} - V_T$. This affects positively the offset voltage, current

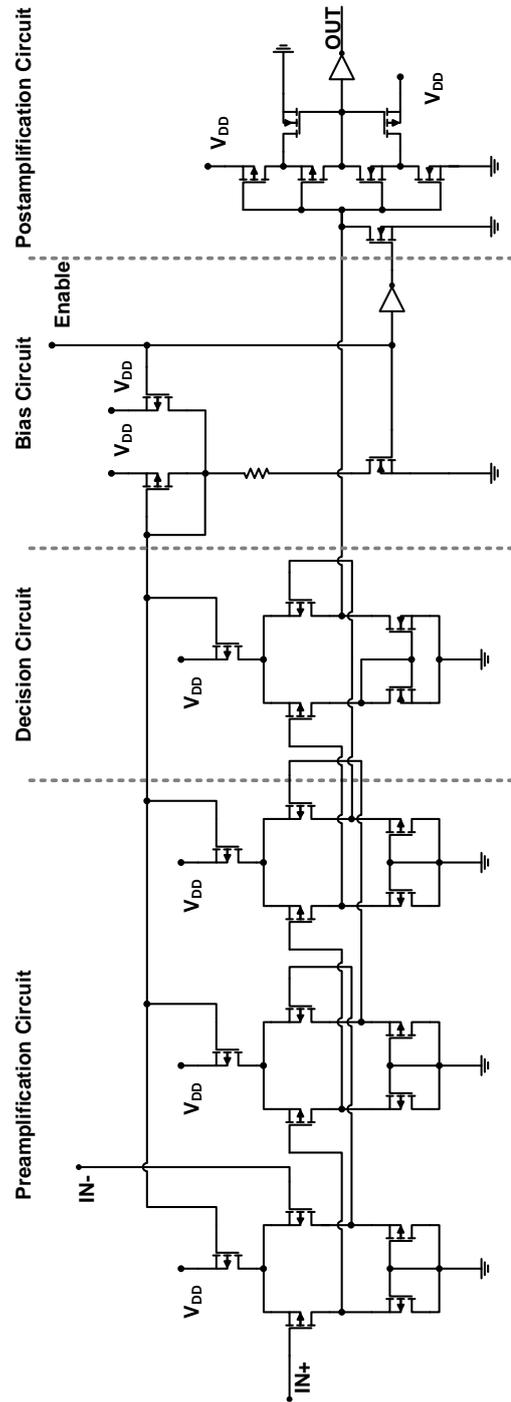


Figure 3.3: Voltage Comparator with Preamplification Circuit (3 Fully Differential Pairs), Decision Circuit (1 Simple CMOS OTA), Postamplification Circuit (Schmitt trigger and Inverter) and Biasing Circuit

consumption and gain. The offset voltage is mainly caused by the mismatch of the threshold voltages. Therefore, the offset voltage can be estimated by calculating the standard deviation of the threshold voltage. Equation 3.10 describes the variation of the threshold voltage of a transistor with the size W [μm] times L [μm] for 1σ :

$$\sigma_{\Delta VT} = \frac{A_{\Delta VT}}{\sqrt{W \cdot L}} \quad , \quad (3.10)$$

$A_{\Delta VT}$ [$\text{mV } \mu\text{m}$] denotes the matching parameter of the threshold voltage for 1σ . The offset voltage is approximately inversely proportional to the square root of the area of the transistor. The outcome of this is that the transistors for the differential pair and the diodes are big. The area for the second stage can be reduced by the square of the gain of the first stage A_1 , in order that the impact of each transistor to the offset voltage is approximately the same. The area of the third stage can be reduced by $(A_1 \cdot A_2)^2$. The offset voltage for a 3σ design can be estimated as follows, whereby A_n denotes the gain of stage n :

$$\begin{aligned} V_{OS}(3\sigma) &\approx \sqrt{\left(\frac{3 \cdot A_{\Delta VT}}{\sqrt{W_1 \cdot L_1}}\right)^2 + \left(\frac{3 \cdot A_{\Delta VT}}{\sqrt{W_2 \cdot L_2} \cdot A_1}\right)^2 + \left(\frac{3 \cdot A_{\Delta VT}}{\sqrt{W_3 \cdot L_3} \cdot A_1 \cdot A_2}\right)^2 + \left(\frac{3 \cdot A_{\Delta VT}}{\sqrt{W_{OTA} \cdot L_{OTA}} \cdot A_1 \cdot A_2 \cdot A_3}\right)^2} \\ V_{OS}(3\sigma) &\approx 1.16 \text{ mV} \quad . \end{aligned} \quad (3.11)$$

The inaccuracies introduced by the voltage comparator and the resistive voltage divider are similar. This means that, concerning mismatch, the resistive voltage divider is not over- or undersized regarding the voltage comparator. The inaccuracies caused by the resistive voltage divider and the voltage comparator can be calculated from equation 3.9 and 3.11 as follows:

$$\begin{aligned} e &= \sqrt{e_{RVD}^2 + V_{OS}^2} \\ e &= 1.58 \text{ mV} \quad . \end{aligned} \quad (3.12)$$

This result of equation 3.12 is similar to the simulation results in section 4.3.

3.5 Clock Manipulation Block

In worst case, the output voltage drops $14 \text{ mV}/\mu\text{s}$, as seen from equation 3.2. In order to avoid undershoot a circuit which manipulates the clock is implemented. The result is an asynchronous design. This allows the converter to react faster on a trigger event, caused by comparator H or comparator L . The output signal of this circuit is used for the synchronization of the comparators with the controller and as clock for it. The synchronization is done with two flip flops in series. The first flip flop is clocked with the output signal. The signal is delayed with a buffer and clocks then the second flip

presented in section 4.1. The controller is sensitive to the rising edge of the clock and reacts after a short delay. After this, the circuit continues to work with the external clock.

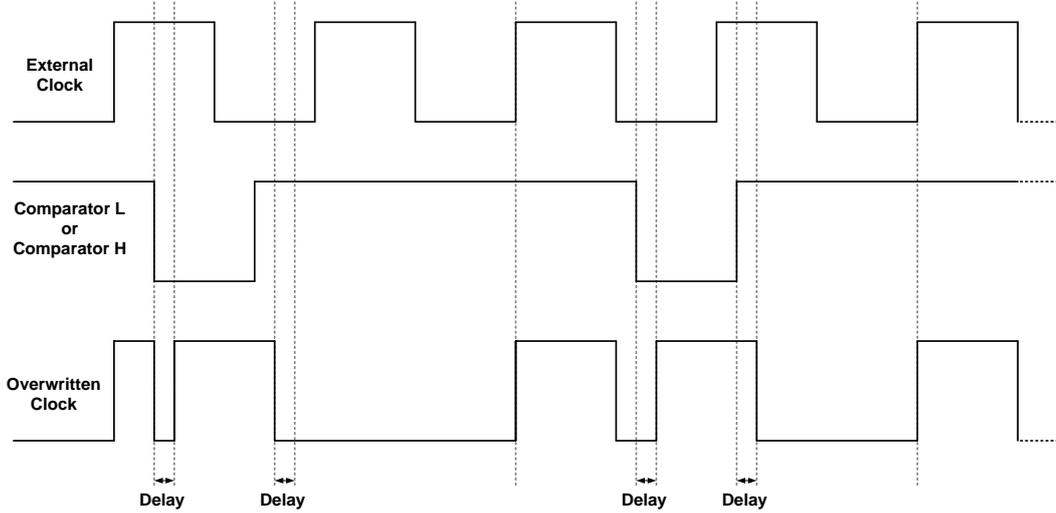


Figure 3.5: Timing Behavior of the Clock Manipulation Block

3.6 Start Up Block

During start up, the output capacitor is charge via a current source. Figure 3.6 depicts the schematic for the generation of the start up current. The start up block consists mainly of a PMOS current mirror which provides the start up current and a NMOS current mirror.

I_{REF} is generated by a circuit which is biased with 1.2V and which is reused in this project. This current is almost constant over temperature to get a better defined start up behavior of the circuit. For the start up, the enable signal is set to '1'. Transistor N3 is turned on and forms together with N1 the master for the NMOS current mirror. N2 is the slave. N4 is turned off. The current through N2 flows through P1, since P3 is turned off too. P1 is the master and P2 is the slave of the PMOS current mirror. $I_{Start Up}$, provided by P2, is:

$$I_{Start Up} = 10 \cdot 180 \cdot I_{REF} \quad . \quad (3.13)$$

If the enable signal is '0', the N3 is turned off and N4 pulls the gate of N1 and N2 with ground. No current is mirrored. P3 is turned on and pulls the gates of P1 and P2 to V_{IN} . $I_{Start Up}$ is zero.

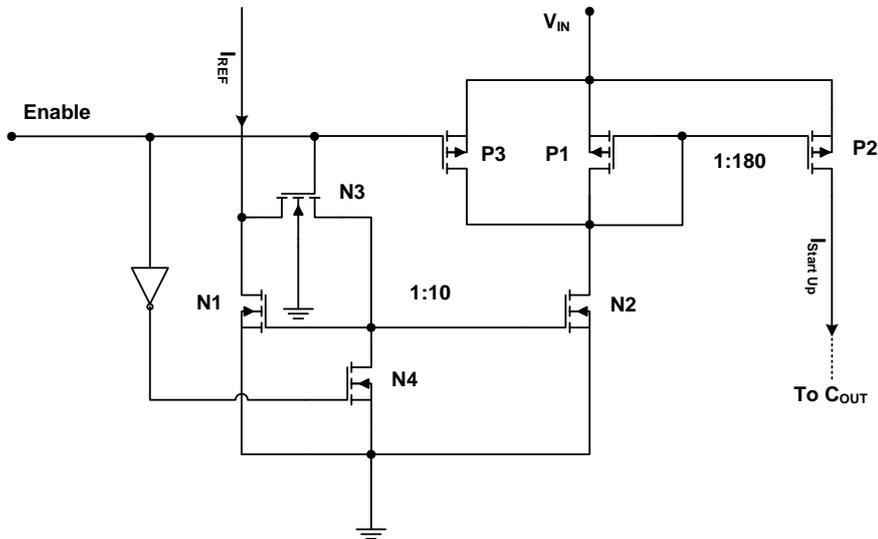


Figure 3.6: Schematic of the Start Up Current Generation Block

3.7 Controller

The controller, implemented in this converter, uses PFM and gain switching to regulate the output voltage, as described in section 2.6. Figure 3.7 depicts the output voltage and the used gains¹ for different output currents. “H” and “L” mark the upper and lower level, at which the comparators trigger. “N” marks the level for the nominal output voltage.

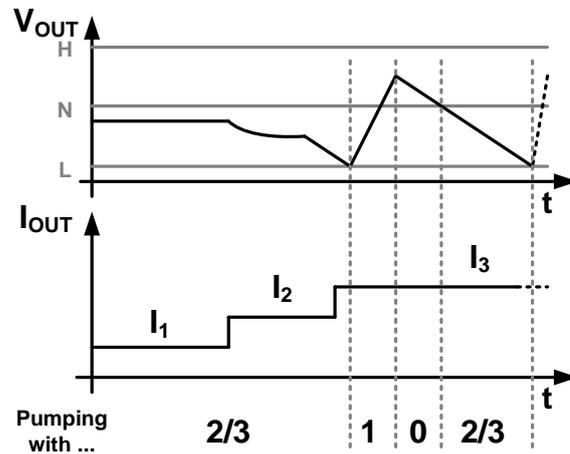


Figure 3.7: Applied Control Strategy, using PFM and Gain Switching

¹0... do nothing 2/3... gain 2/3 1... gain 1

For a certain output current I_1 , the converter is pumping with gain $2/3$ and keeps the output voltage in specification. As the output current increases to I_2 , the converter is still pumping with gain $2/3$. The average output voltage drops but is still higher than level L . The output current increases further to I_3 and the converter applies as long as possible gain $2/3$. But the output voltage drops and reaches level L . The converter performs one pump with gain 1, which transports more charge to the output capacitor but with a lower efficiency. The output voltage increases and is higher than level N . The converter waits, until the output voltage gets lower than level N . Then, the converter starts pumping with gain $2/3$ as long as possible, until the output voltage reaches level L . Basically, the implemented converter pumps as long as possible with gain $2/3$, stops pumping if the output voltage is higher than level N and performed one pump with gain 1, if the output voltage reaches level L .

Figure 3.8 shows the implemented finite state machine. The source code is given in the appendix. The states control the signals for the drivers, the start bit for the clock manipulation circuit and the enable signal for the start-up circuit and for the voltage comparators. Not all comparators are needed in each state. Therefore, unused comparators are disabled to save energy. The controller has following states:

- Power Down: The state machine changes in this state, if the enable signal is '0' or the IDDQ signal is '1'.
- Start Up: The enable signal for the start up circuit as described in section 3.6 is set to '1'. The output capacitor is charged via a current source until comparator L triggers.
- Common Mode: As long as the output signal of comparator N is '1', the state machine stays in common mode. As the output voltage drops and the output signal of comparator N becomes '0', the state machine switches to state gain $2/3$. If comparator L is '0', the state machine goes to state gain 1.
- Gain $2/3$: The state machine goes in the common mode state, if the output signal of comparator L is '1', else in state gain 1.
- Gain 1: The state machine goes in the off state, whereby all switches are turned off.
- Off State: The state machine waits until the output voltage falls below 1.2 V. If the output signal of comparator N is '0', then the state machine goes to the common mode state.

If the IDDQ signal is set to '1', the state changes to power down state. The IDDQ signal can overwrite all other signals like the enable signal and the signal for the power down switch S9. So, an IDDQ test can be performed by applying a voltage between input and output, between input and ground or between output and ground. Thereby, the current consumption is measured.

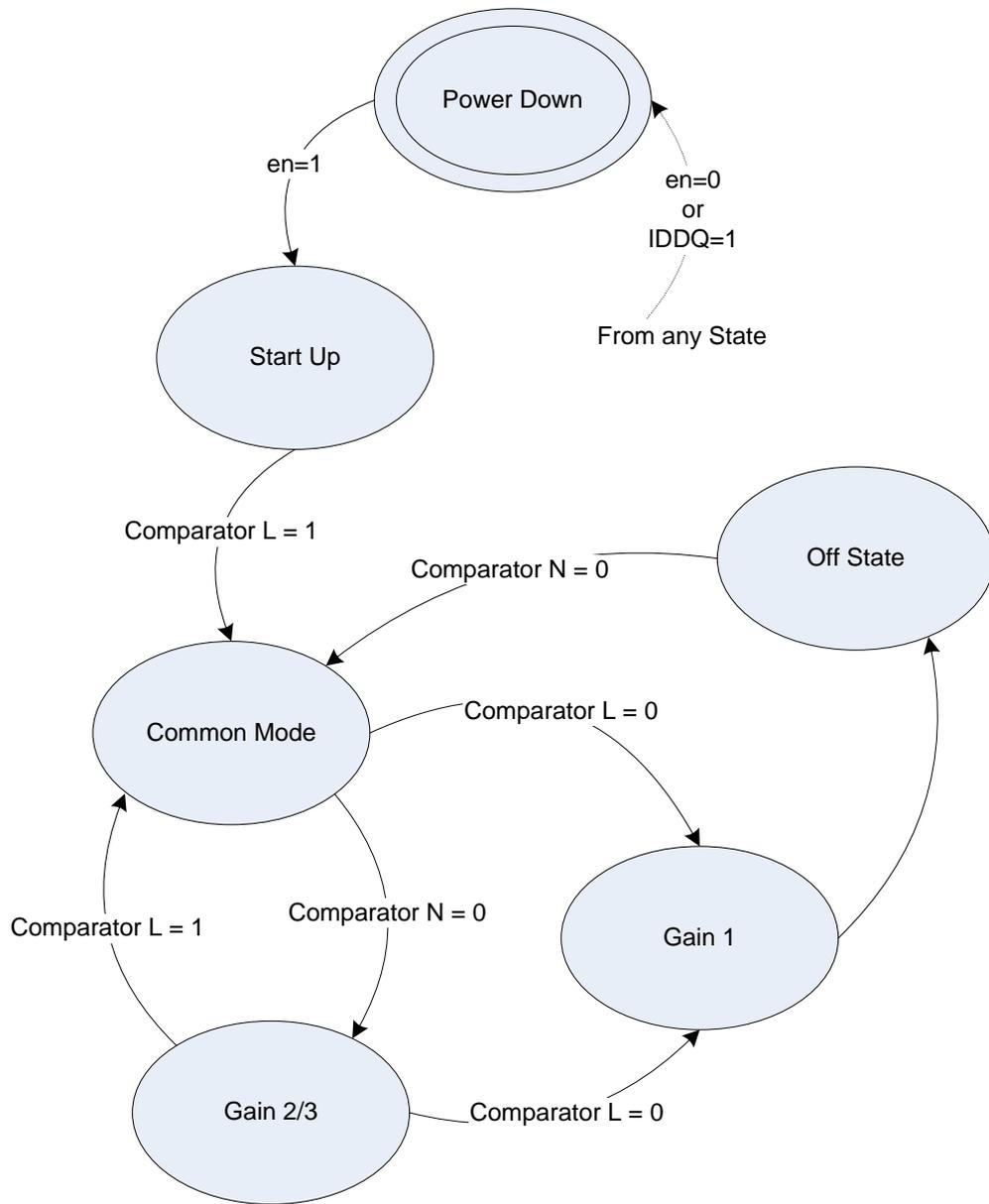


Figure 3.8: Finite State Machine of this Switched Capacitor DC-DC Converter

3.8 Non Overlapping Phases

To achieve non overlapping turning on signals for the switch network as described in section 2.5, a non overlapping clock with two phases can be used. But non overlapping phases for the switch network can be accomplished easier. The desired behavior to delay only the turning on signal and not the turning off signal for the switches can be achieved either with buffer and gates or with asymmetrical drivers. Both possibilities are described in the following, whereby the latter possibility is implemented in this converter.

3.8.1 Non Overlapping Phases with Buffer and Gates

Non overlapping signals for the switches can be realized combining gates and buffers, whereby the buffer introduces a delay into the signal path, as depicted in figure 3.9.

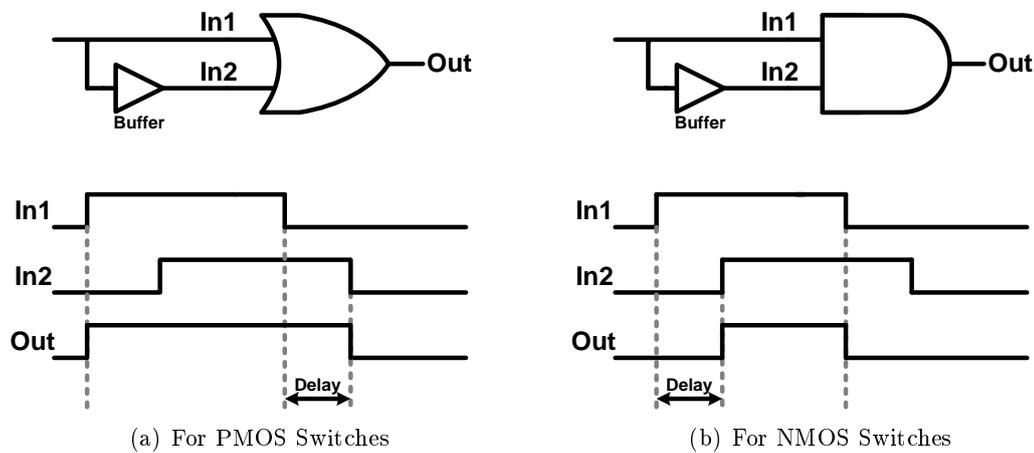


Figure 3.9: Non Overlapping Phases with Buffer and Gates

To drive a PMOS switches, a buffer and an OR gate can be applied. If the output of the OR gate is '1', then the PMOS transistor is off. As shown in figure 3.9(a), the transition from '1' \rightarrow '0' is affected by the delay and turning on the PMOS switch is delayed. The transition from '0' \rightarrow '1' is not affected by the delay and turning off the PMOS switch happens immediately.

The same considerations can be done for the NMOS switches. Figure 3.9(b) depicts a buffer and an AND gate, which can be applied to drive a NMOS switch.

3.8.2 Asymmetrical Driver

In this work, asymmetrical drivers are used to generate non overlapping phases. The drivers are supposed to have a short rise and fall time in order to be able to make a

short non overlapping time, since in this time no charge is transported. Furthermore, the turning on signal has to be delayed in contrast to the turning off signal, which has to propagate fast through the driver. This behavior generates non overlapping signals for the switches. This avoids shoot through current and is therefore important for the efficiency.

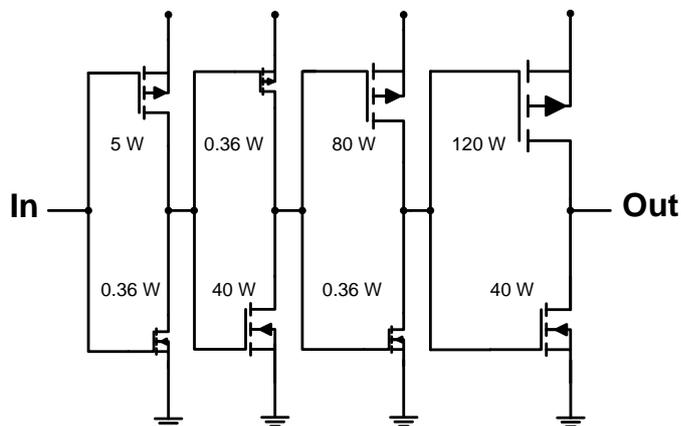


Figure 3.10: Asymmetrical Driver for NMOS Switch to generate Non Overlapping Phases

Figure 3.10 depicts the driver for a NMOS switch. The driver consists of four inverter stages. The first inverter of the driver has a strong PMOS and a weak NMOS transistor. The second inverter has a weak PMOS and a strong NMOS transistor. Thereby, the desired behavior is achieved, namely, to propagate fast '0' and to delay '1'. The third inverter has a strong PMOS and a weak NMOS transistor. The last inverter, which drives the gate of the switch, should have a strong NMOS transistor and a strong PMOS transistor in order to keep the rise and fall time of the output short. The output of the fourth stage is connected to the switch.

Similar considerations can be done for the asymmetrical driver for the PMOS switch. This driver has the property to delay '0' and propagate fast '1'.

The simulation results for the asymmetrical drivers are given in section 4.4.

3.9 Switch Network

The switch network is the core of the switched capacitor DC-DC converter. Based on the findings in section 2.4, a switch network is designed. The schematic of the switch network is depicted in figure 3.11. Switch S1 to S6 are designed with PMOS transistors and switch S7 to S9 are NMOS transistors. Switch S9 is an additionally power down transistor to discharge the output capacitor. Switch S7 is not a transmission gate consisting of a NMOS and a PMOS transistor, but just a NMOS transistor. Simulation results have shown that an additional parallel PMOS transistor has almost no benefit for R_{ON} .

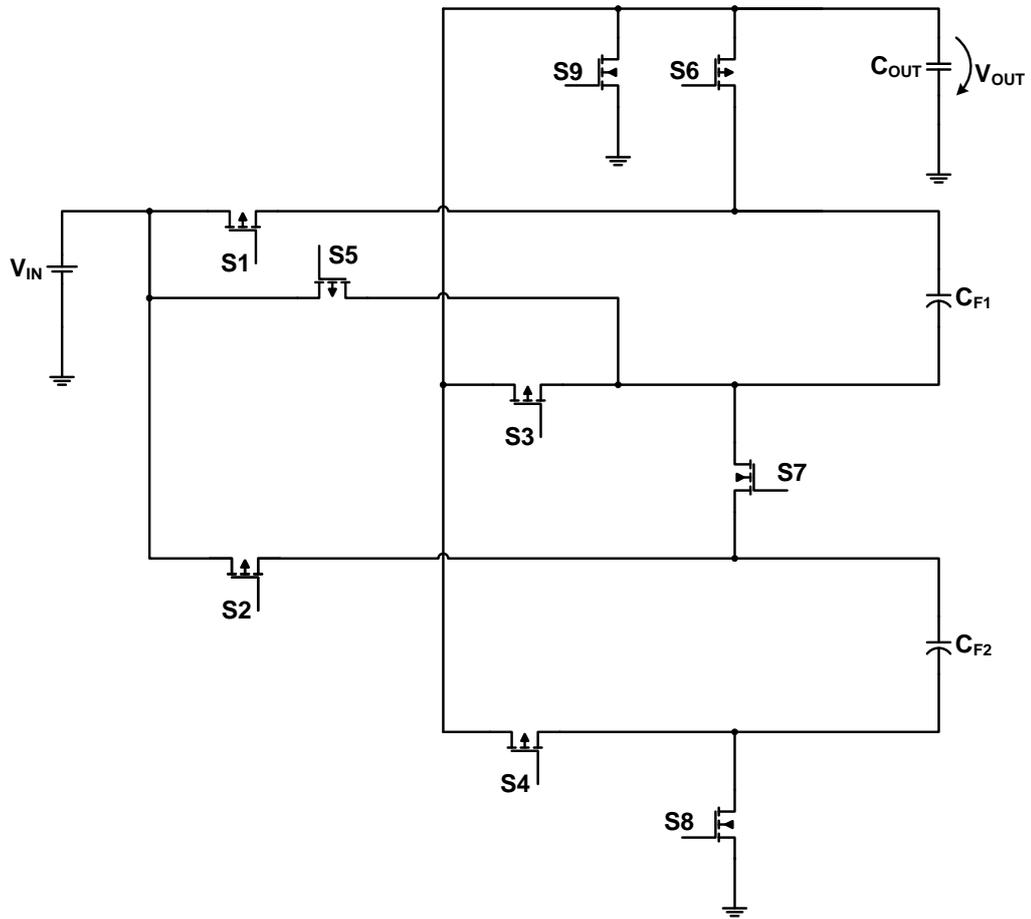


Figure 3.11: Schematic of the Switch Network to Transport Charge in Two Phases with Flying Capacitors from the Input Supply to the Output Capacitor

Figure 3.12: Bits of the Switch Configurations for Different States

State	Switch								
	S1	S2	S3	S4	S5	S6	S7	S8	S9
Power Down	1	1	1	1	1	1	0	0	1
Start Up	1	1	1	1	1	1	0	0	0
Common Mode	0	0	0	0	1	1	0	0	0
Gain 2/3	1	1	1	1	1	0	1	1	0
Gain 1	1	1	1	1	0	0	0	0	0
Off State	1	1	1	1	1	1	0	0	0

As given in equation 2.17,

$$R_{ON} \propto \frac{1}{K'} \quad \text{with} \quad K' = \mu_0 \cdot C_{OX} \quad .$$

Since $K'_{NMOS} \approx 3 \cdot K'_{PMOS}$, $R_{ON\ NMOS}$ is three times smaller than $R_{ON\ PMOS}$ for the same dimensions [1]. Table 3.12 gives the states and the according bits for the switches, whereby '1' means that $V_{GS} = V_{DD}$ and '0' means $V_{GS} = 0V$.

3.10 Frequency

A rough estimation for the switching frequency is given by R_{ON} and $C_{F1,2}$. The switching losses are proportional to the switching frequency. To minimize the switching losses, each pump should deliver as much charge as possible. After five τ , the capacitor is loaded to 99.3% and almost no current is flowing. Almost as much charge as possible is delivered. The outcome of this is that the external frequency can be estimated as follows:

$$f_{\text{external}} = \frac{1}{5 \cdot R_{ON} \cdot C_F} \quad . \quad (3.14)$$

Because the circuit works in two phases and is sensitive to the rising edge of the clock, the switching frequency is half of the external frequency:

$$f_{\text{switching}} = \frac{1}{2} \cdot f_{\text{external}} \quad . \quad (3.15)$$

Chapter 4

Simulation Results

This chapter presents the simulation results of the designed switched capacitor DC-DC converter. All simulations are performed on transistor level to get accurate simulation results. The simulation results include corner simulations for single components like the buffer and the drivers. Corner simulations include variations of technology parameters¹, temperature and supply voltage. To simulate the offset introduced by mismatch of the resistive voltage divider and the voltage comparator, a Monte Carlo simulation is performed. The drivers and the switches are connected together to design the switch network, since the drivers have a major impact on the efficiency as described in section 2.5. Finally, the full converter is simulated on transistor level as well. Corner simulations of the behavior of the converter during ramp up of the power supply and start up are performed. The efficiency is simulated for different temperatures, output currents and switching frequencies. The transient behavior of the converter is simulated under nominal conditions and the impact of the clock manipulation is explained.

The simulation results show that the switched capacitor DC-DC converter fulfills the requirements. The converter can deliver a nominal output current of 30 mA with an efficiency of 96%.

4.1 Buffer

Figure 4.1 depicts the results of the corner simulation including input signal and output signal of the buffer. Table 4.1 presents the according timing of the buffer. The delay is measured from 50% of the input signal to 50% of the output signal. The rise and fall time of the output signal is measured from 10% to 90% respectively. The longest path of the controller is less than 1 ns. The simulation results show that the shortest delay produced by the buffer is 1.1 ns. Therefore, the controller has enough time to change its

¹No comments regarding the technology variations, since it is intellectual property of Infineon Technologies Austria AG

internal signals which define the next state, before the next clock edge arrives. Different variations have different impacts on the behavior of the circuit. The shortest delays are achieved with the highest power supply and the lowest temperature. The longest delays are achieved with minimum power supply and highest temperature. The variation of the temperature is dominating.

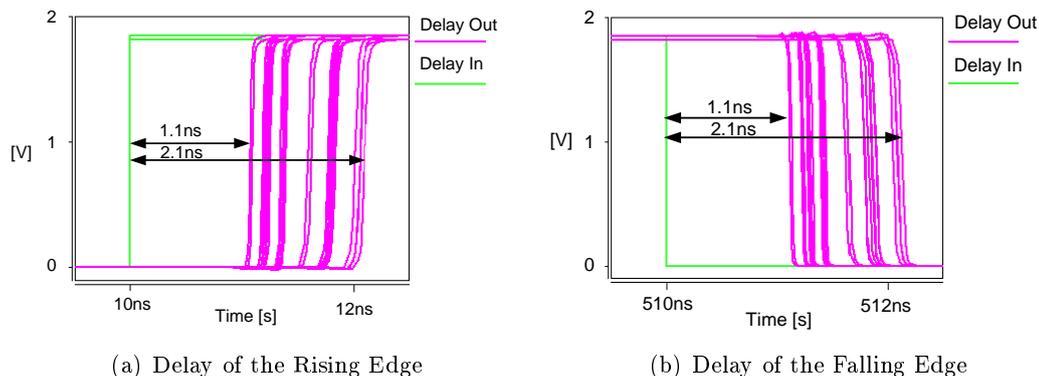


Figure 4.1: Simulation Results for the Buffer which delays the Clock for the Controller

Table 4.1: Simulation Results for the Buffer

	min.	nom.	max.
Delay of the rising edge	1.07 ns	1.67 ns	2.1 ns
Delay of the falling edge	1.11 ns	1.7 ns	2.12 2ns
Rise time	36 ps	60 ps	78 ps
Fall time	33 ps	59 ps	74 ps

4.2 Resistive Voltage Divider

As described in section 3.3, the matching of the unit resistors is important, because it influences the voltage levels for the voltage comparators. Therefore, the resistive voltage divider is simulated with a Monte Carlo simulation with 1000 runs. Figure 4.2 depicts the output voltage, at which the comparators trigger. The resulting voltages from the resistive voltage divider are compared with 0.6 V. The introduced uncertainty of the trigger level for the voltage comparator is ± 1 mV. The simulation results fit to the result in equation 3.9.

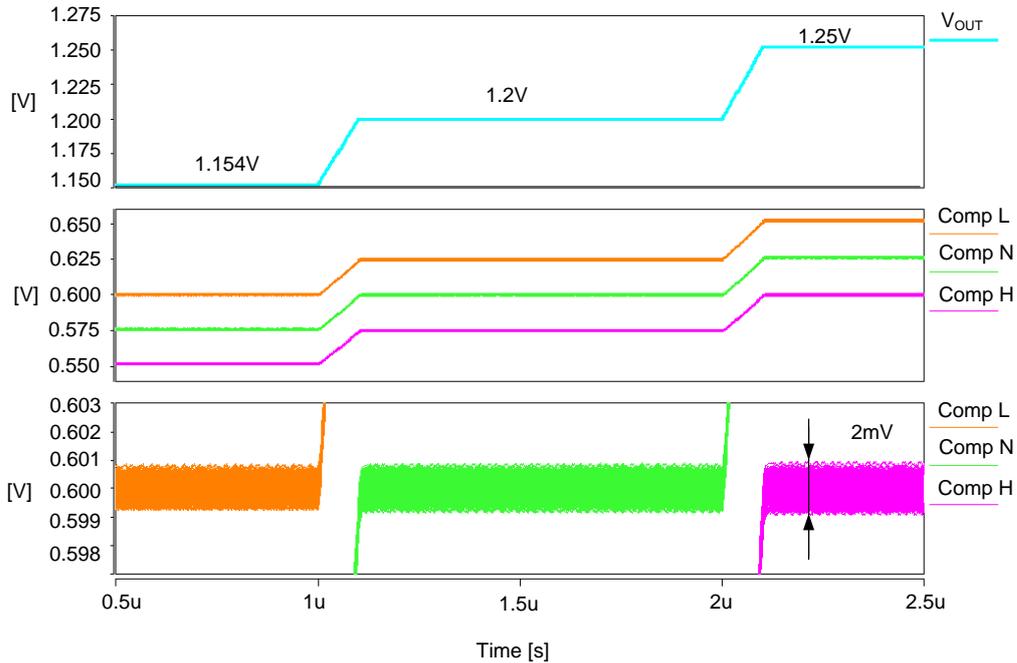


Figure 4.2: Variation of the Output Voltage and Resulting Voltages for the Inputs of the Voltage Comparator with Introduced Uncertainty caused by Mismatch of the Resistive Voltage Divider

4.3 Voltage Comparator

The offset voltage of the voltage comparator is simulated with a Monte Carlo simulation with 1000 runs. The standard deviation of the offset voltage is 0.47 mV. The offset voltage for a 3σ design is 1.41 mV. This is similar to the results of equation 3.11. The maximum measured offset voltage is 1.65 mV. The main contribution to the offset voltage comes from the first stage of the preamplification circuit as described in section 3.4.

Resistive Voltage Divider and Voltage Comparator

The maximum steepness of the falling output voltage caused by an output current of 200 mA is according to equation 3.2 $-14\text{ mV}/\mu\text{s}$. This, the influence of the resistive voltage divider and the timing behavior of the voltage comparator are included in a Monte Carlo simulation with 1000 runs at -20°C and $+125^\circ\text{C}$.

Figure 4.3 depicts the waveforms of the input voltages resulting from the resistive voltage divider and the resulting output signals of the voltage comparator.

The time, until the voltage comparator triggers is measured. This simulation shows that comparator *L* triggers in worst case at an output voltage of 1.147 V. As the output

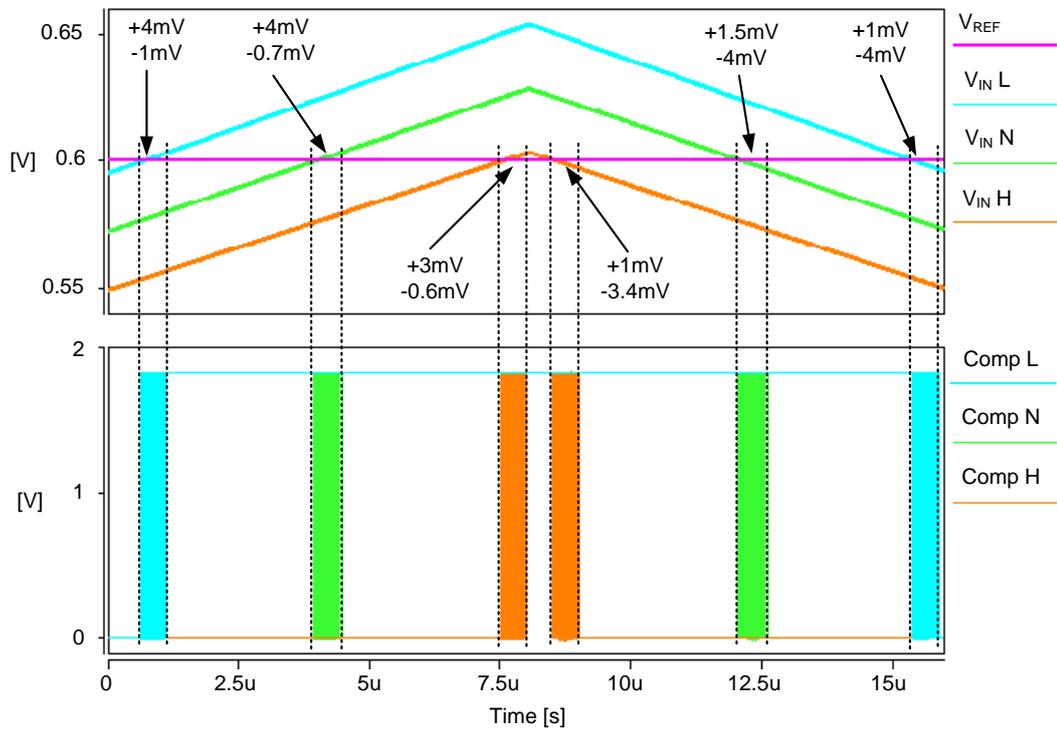


Figure 4.3: Input Voltage and Reference Voltage with the resulting Output Signals of the Voltage Comparators

voltage continues to fall caused by an output current of 200 mA and a minimum sized output capacitor, the circuit has enough time (114 ns) to react until the output voltage would fall out of specification.

The standard deviation of the uncertainty introduced by the resistive voltage divider and the voltage comparator is 0.45 mV. The uncertainty for a 3σ design is 1.35 mV. This is similar to the results of equation 3.12.

4.4 Asymmetrical Drivers

The asymmetrical drivers are responsible for the generation of the non overlapping phases of the switch network. Each switch has a certain capacitance at the gate. To get accurate simulation results, this capacitance is included in the simulation. MOS capacitors with the size of a switch are connected to the output of the drivers. To simulate a PMOS switch, the gate of the PMOS is connected to the output of the driver. Drain and source are connected to the positive power supply. To simulate a NMOS switch, the gate of the

NMOS transistor is connected to the output of the NMOS driver and drain and source are connected to ground.

Figure 4.4 depicts the results of the corner simulation of the asymmetrical drivers. The timing of the drivers is given in table 4.2. The non overlapping time is measured from 90 % off to 10 % on. The delay of the rising and falling edge is measured between 50 % from the input signal to 50 % of the output signal. The simulation shows that the drivers generate non overlapping phases for the switch network.

The dominating effect on the delay of the drivers is the variation of the temperature.

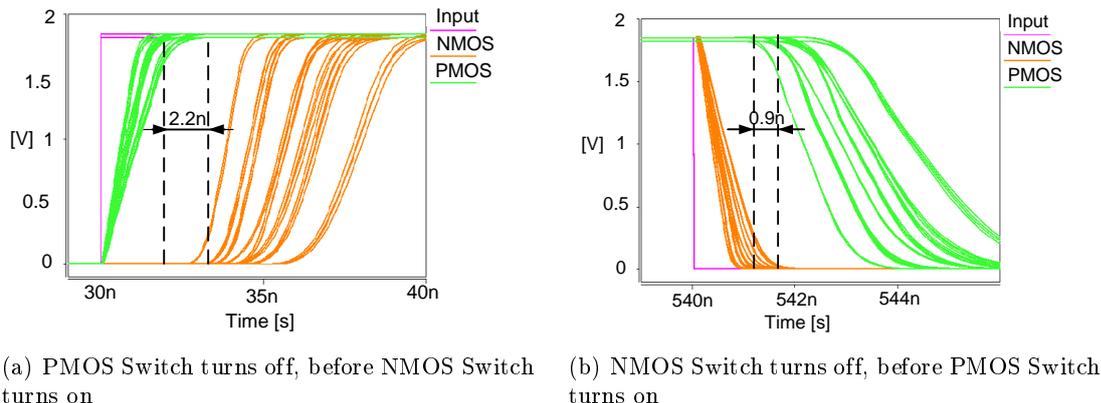


Figure 4.4: Simulation Results for the Asymmetrical Drivers

Table 4.2: Timing of the Asymmetrical Drivers

	min.	nom.	max.
NMOS off, PMOS on	0.89 ns	1.43 ns	2 ns
PMOS off, NMOS on	2.2 ns	3.42 ns	4.7 ns
PMOS - Delay of rising edge	0.57 ns	0.84 ns	1.07 ns
PMOS - Delay of falling edge	2.2 ns	3.38 ns	4.5 ns
NMOS - Delay of rising edge	3.8 ns	5.93 ns	7.9 ns
NMOS - Delay of falling edge	0.38 ns	0.53 ns	0.7 ns

4.5 Switches

As described in section 2.7, R_{ON} should be low in terms of load capability and efficiency. To size the switches, following simulations are performed: The drivers are connected to the switches. The simulation is started under nominal conditions. The current, pulled from the output capacitor is once 30 mA and then 60 mA. The efficiency is measured in steady state. The width of the each switch is increased separately. To model the switch network more accurately, the resistance of the wiring is introduced. The resistance of the

bonding wires is assumed to be $100\text{ m}\Omega$ and the wiring between the switches is assumed to be $25\text{ m}\Omega$.

Figure 4.5 depicts efficiency vs. width of switch S7. As the width is increased, the efficiency increases too. At a certain point, the efficiency begins to decrease, even if the width is increased, because the switching losses dominate the gain of the lower R_{ON} . At highest efficiency, the curve is flat. Because of this, the resulting values for the switches are a compromise between area and efficiency. Table 4.3 gives the width of the switches, which are applied in this converter. The switches have a minimum length of 180 nm .

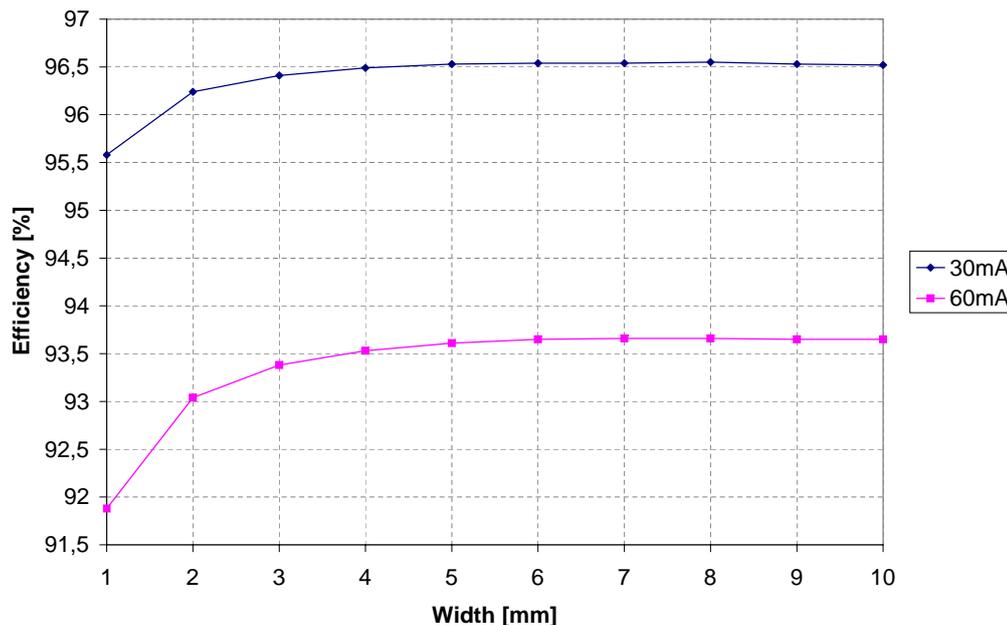


Figure 4.5: Efficiency vs. Width for Switch S7

Table 4.3: Width of the Switches

S1	12 mm	S4	16 mm	S7	6 mm
S2	12 mm	S5	10 mm	S8	6 mm
S3	16 mm	S6	24 mm	S9	40 μm

4.6 Frequency

At the begin of the gain phase, more charge is transported to the output capacitor than in the end. Therefore, increasing the frequency means avoiding this time in which less current is flowing. This results in a higher average output voltage, because more charge is

transported to the output capacitor. This is beneficial for the efficiency, because higher output currents can be supported without switching from gain 2/3 to gain 1.

Assuming $R_{ON}=0.2\Omega$ and $C_F=1\mu\text{F}$, according to equation 3.14 the external frequency is 2 MHz and the switching frequency is 1 MHz. Figure 4.6 shows the waveforms of the output voltage of a simulation with nominal values for power supply, technology parameters, capacitors and temperature. Thereby, the output current is 30 mA and 60 mA. The external frequency is varied from 1 MHz to 3 MHz in steps of 500 kHz. There are two interesting observations regarding the average output voltage, since the converter is pumping only with gain 2/3. First of all, the upper waveforms correspond to the simulation results with 30 mA output current and the lower waveforms correspond to the simulation results with 60 mA output current. Second, a higher frequency results in a higher average output voltage.

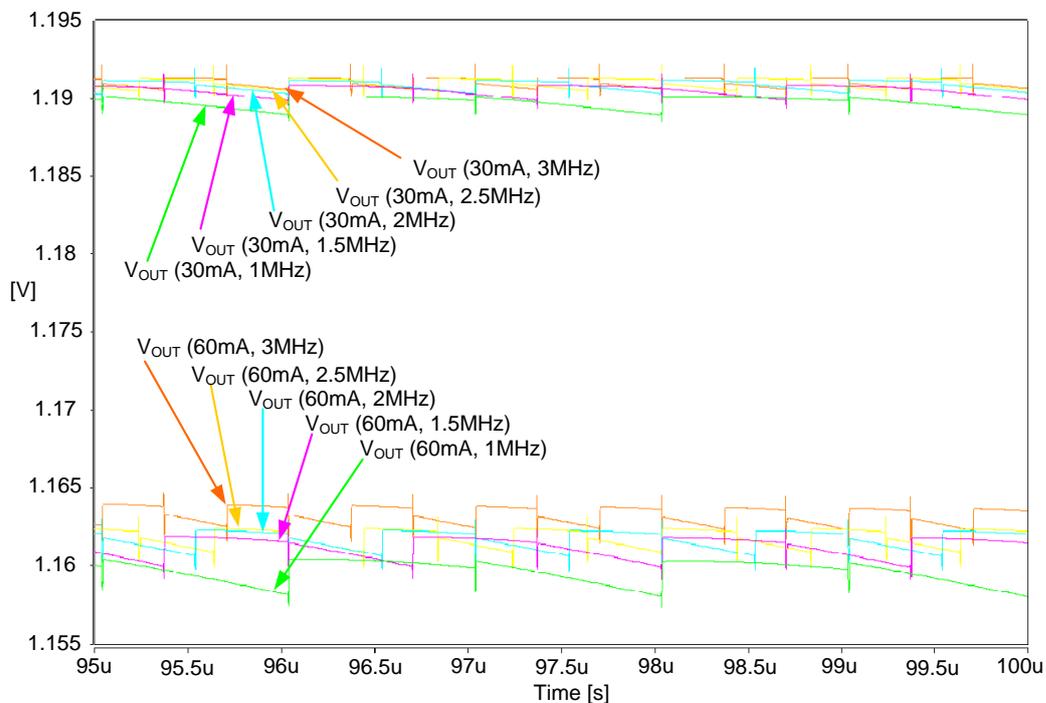


Figure 4.6: Variation of the Frequency with 30 mA and 60 mA Output Current, whereby the Converter Operates only with Gain 2/3; Higher Output Current results in a Lower Average Output Voltage; A Higher Switching Frequency results in a Higher Average Output Voltage

4.7 Switched Capacitor DC-DC Converter

In this section the simulation results of the switched capacitor DC-DC converter are presented. Output current, switching frequency, temperature and technology parameter are changed to show the impact of different variations to the circuit.

4.7.1 Ramp Up of the Power Supply

The simulation of the ramp up of the power supply is necessary to check if during the ramp up no unwanted currents are flowing. The ramp up time for the power supply is assumed to be 100 μs .

Figure 4.7 shows the simulation results of a corner simulation varying technology parameters and temperature. It depicts the waveforms of the supply voltage, the output voltage and the consumed current. No output current is pulled from the output capacitor. After the ramp up of the power supply, the enable signal is set to '1', the IDDQ signal is '0' and the clock is running. The circuit is in the start up state.

A simple visual check to the current consumption gives that no extraordinary currents flow during the ramp up of the power supply. During start up, the output voltage rises.

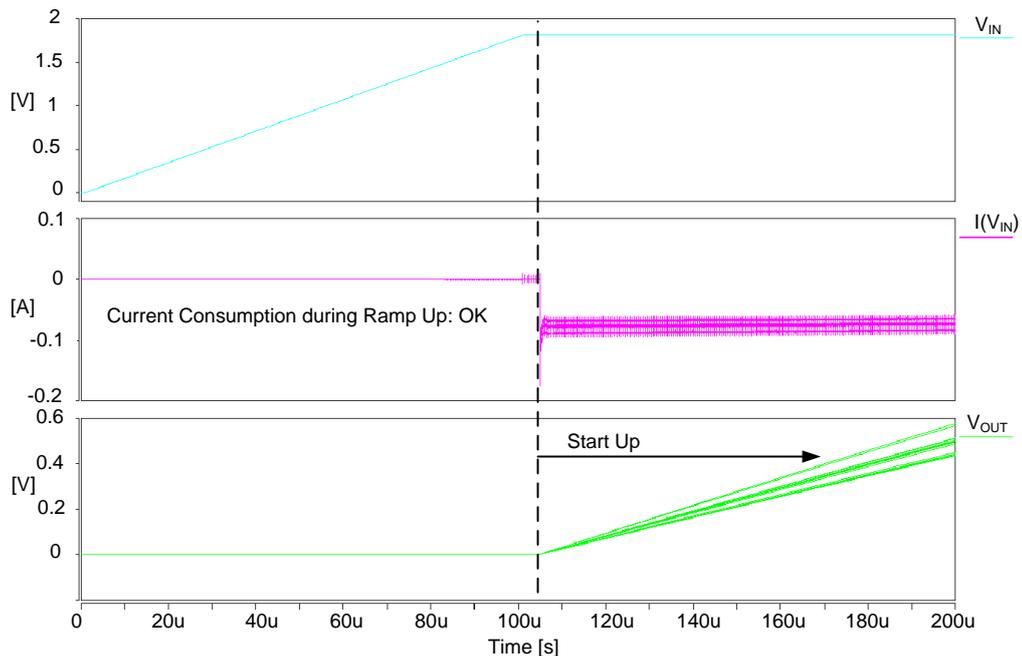


Figure 4.7: Ramp Up of the Power Supply, Current Consumption of the Converter and Output Voltage, including Begin of Start Up Phase

4.7.2 Start Up

The setup for the simulation looks like follows: At the beginning, $V_{OUT} = 0V$. The enable signal is set to '1'. At the same time, an output current of 30 mA is pulled from the output capacitor, which has maximum size. The maximum start up time is 1 ms. The start up time is the time that the output voltage takes from 0 V to 1.145 V. Figure 4.8 depicts the waveforms of the output voltage of a corner simulation. The simulation results of the start up time are given in table 4.4. As given in equation 3.1, the size of the output capacitor has a big impact on the start up time. Also the variation of the technology parameters has a big impact as well.

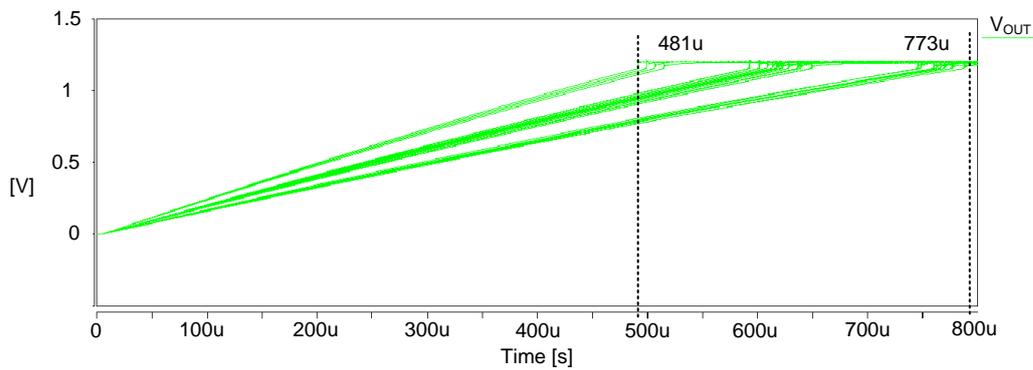


Figure 4.8: Waveform of the Output Voltage during Start Up Phase

Table 4.4: Start Up Time of the Converter

	min.	nom.	max.
Start Up Time	481 μ s	622 μ s	773 μ s

4.7.3 Efficiency

After a successful ramp up of the power supply and start up, the main functionality is simulated. The simulation results for the efficiency for different output currents, switching frequencies and temperatures are presented. The simulation results end with the transient behavior of the converter.

Efficiency for Different Switching Frequencies

Figure 4.9 depict the efficiency vs. frequency for an output current of 30 mA and 60 mA. The simulation is started under nominal conditions. The simulation results show that

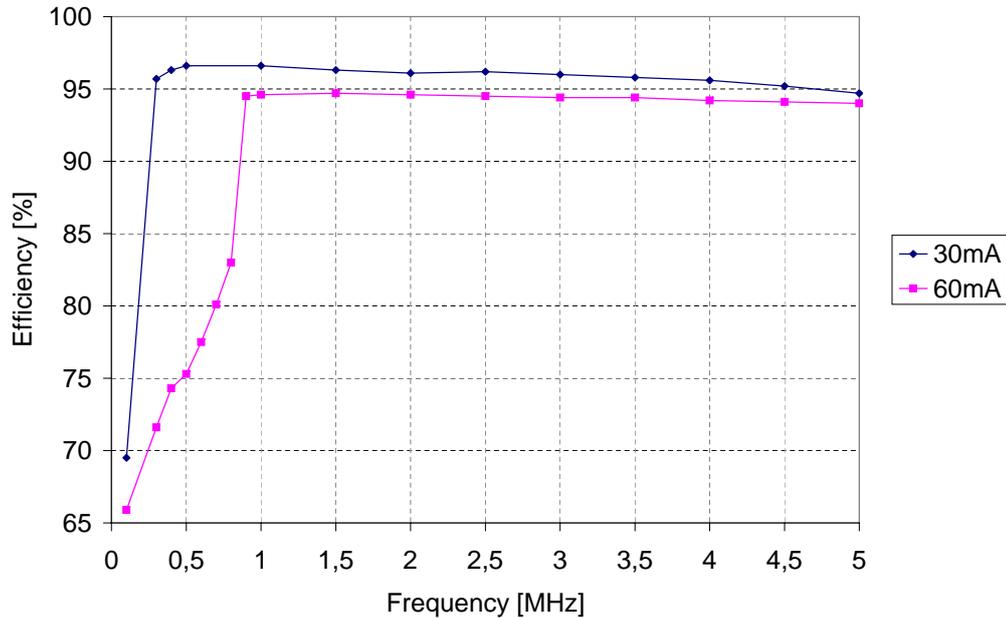


Figure 4.9: Efficiency vs. Frequency for 30 mA and 60 mA Output Current

the converter pumps for low frequencies (100 kHz) with gain 1 and gain 2/3. Since gain 1 is needed, the efficiency is low. As the frequency increases, more charge is transported to the output capacitor. Gain 1 is used less often and the efficiency increases. The frequency is increased further, the average output voltage is increased as described in section 4.6 and gain 1 is avoided. For different output currents, this happens at different frequencies, as depicted in figure 4.9. The converter operates only with gain 2/3. The efficiency is very high. If the switching frequency increases higher than necessary, the efficiency decreases due to higher switching losses.

There are two impacts on the efficiency: On the one hand, the switching losses are proportional to the switching frequency. Therefore, a low frequency is beneficial for a high efficiency. On the other hand, the average output voltage increases with higher switching frequency. The frequency should be high enough to transport sufficient charge to the output capacitor. This is beneficial for a high efficiency.

The peak efficiency for different output currents is at different switching frequencies. Therefore, the frequency could be modified with a VCO, but this is beyond the scope of this master's thesis.

Efficiency for Different Output Currents

Figure 4.10 depicts the efficiency vs. output current for different external frequency. The efficiency for low output currents like 30 mA drops with higher frequencies, because

the switching losses are proportional to the switching frequency, as explained above. The efficiency increases for output currents between 50 mA and 70 mA with higher frequency, because with higher frequency more charge is transported to the output capacitor and gain 1 is not needed and so shifted to higher output currents. As gain 1 is needed, the circuit can perform many pumps with gain 2/3 before one pump with gain 1 is needed, which improves the efficiency as well.

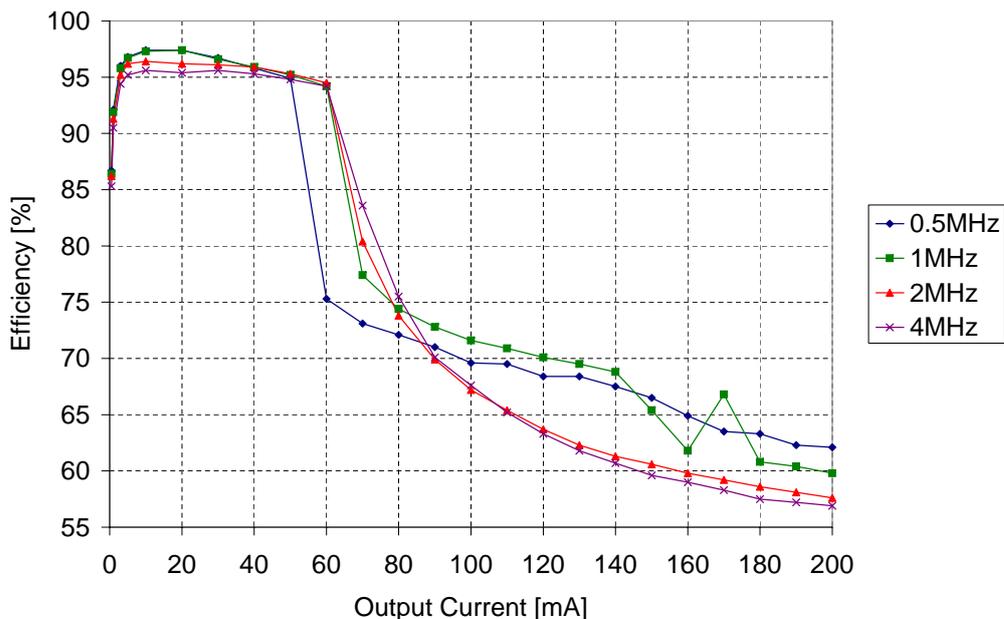


Figure 4.10: Efficiency vs. Output Current for Different External Frequencies

The simulation shows that the efficiency is very high, as long as the circuit can keep the output voltage in specification with only gain 2/3. In this simulation, this holds until 60 mA. As soon as gain 1 is used, a lot of charge is transported with a low efficiency. As a consequence of this the efficiency sinks. The efficiency for the desired ratio of output voltage to input voltage is according to equation 1.2 given by:

$$\eta \approx \frac{V_{OUT}}{V_{IN} \cdot \text{gain}} = \frac{1.2V}{1.83V \cdot 1} = 0.656 = 65.6\% \quad .$$

The circuit pumps as long as possible with gain 2/3 and only if comparator L triggers, once with gain 1. Many pumps can be performed with gain 2/3 and so with high efficiency. From time to time one pump with gain 1 with low efficiency is performed. As the output current increases, the circuit can perform fewer pumps with gain 2/3. This decreases further the efficiency.

For very low output currents the efficiency decreases too. The power consumption of

the drivers, the switches, the voltage comparators, the resistive voltage divider and the controller preponderate.

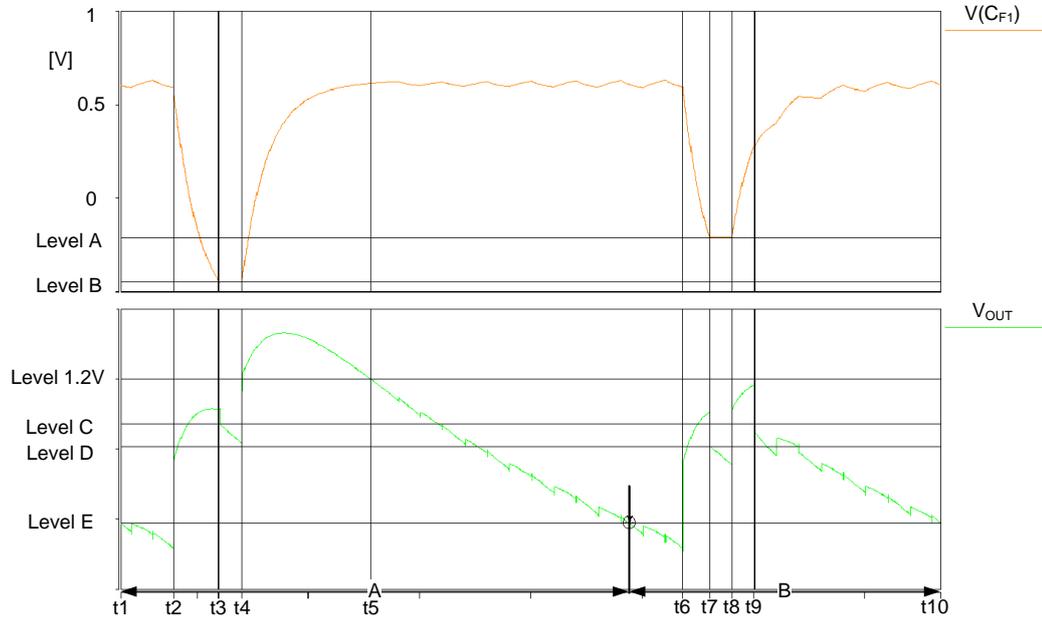


Figure 4.11: Waveforms of the Output Voltage and the Voltage of the Flying Capacitor C_{F1} with 120 mA Output Current and 1 MHz External Frequency

The efficiency increases with lower frequencies for output currents above approximately 70 mA. Consider the waveforms of the output voltage depicted in figure 4.11. For high output currents the efficiency depends on the output voltage as follows:

- $t1$ to $t2$: The circuit uses gain $2/3$ to transport charge to the output capacitor.
- $t2$ to $t3$: The flying capacitor C_{F1} delivers charge to the output capacitor during gain 1 and the output voltage increases to level C. Thereby, C_{F1} is discharged and even reversed biased. The voltage of the flying capacitor falls to level B.
- $t3$ to $t4$: The next state is the off state before the circuit switches to common mode. The voltage of C_{F1} does not change and the output capacitor is discharged by the output current.
- $t4$ to $t5$: The flying capacitors are connected in common mode parallel together and in series to the output capacitor. Thereby, also the output capacitor is charged by the input voltage and the output voltage increases. If enough time is given so that the output voltage is higher than 1.2 V, then the circuit remains in common mode until the output current decreases the output voltage so that comparator N triggers.

- t5 to t6: The circuit continues to pump with gain $2/3$, as the output voltage falls below level 1.2 V.
- t6 to t7: The circuit pumps once with gain 1. The output voltage is raised to level D and the voltage of C_{F1} falls to level A. The output voltage is not increased as much as during t4 to t4+1 period of the clock, because the voltage of C_{F1} decreased during t6 to t7 not that much as during t2 to t3.
- t7 to t8: The circuit is in off state.
- t8 to t9: The converter is in common mode, but the output voltage does not reach level 1.2 V.
- t9 to t10: The circuit continues to pump with gain $2/3$.

The time t2 to t3 or t6 to t7 depends on the external frequency and on the trigger time of comparator L . If this comparator triggers early in the period, then it is more likely that enough time is given and the output voltage is increased higher than 1.2 V as explained above. If the frequency is lower, then it is more likely that enough time is given and the efficiency increases as depicted in figure 4.10.

The simulation results given in table 4.5 show that it is a benefit for the efficiency if the output voltage is increased more than 1.2 V.

Table 4.5: Efficiency for the Waveforms depicted in Figure 4.11

Output Current	Efficiency for A	Efficiency for B
120 mA	70.4%	65.9%

4.7.4 Transient Behavior

The following transient simulation includes a load jump from 30 mA to 60 mA, and from 60 mA to 200 mA and shows the behavior of the output voltage regarding voltage ripple, average output voltage and load response. The simulation is started with nominal conditions. The external applied frequency is 1 MHz.

Figure 4.12 depicts the resulting waveform of the output voltage. The average output voltage for 30 mA output current is 1.189 V and the ripple of the output voltage is 2.4 mV. The load jump to 60 mA reduces the average output voltage to 1.158 V and the ripple increases to 3.1 mV. The load jump to 200 mA increases the average output voltage and increases the ripple of the output voltage to 37 mV, because gain 1 is applied. Furthermore, figure 4.12 depicts also the impact of the manipulation of the clock.

This simulation shows that the converter can keep the output voltage in specification, but the converter can not regulate the output voltage to the nominal voltage of 1.2 V for moderate output currents like 30 mA or 60 mA.

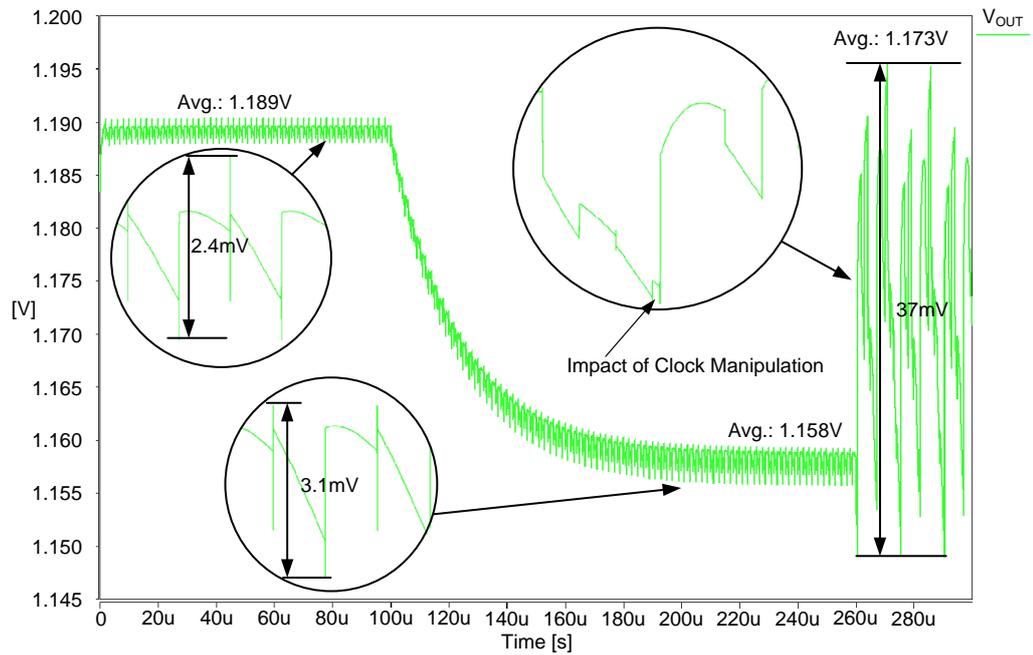


Figure 4.12: Waveforms of the Output Voltage for 30 mA, 60 mA and 200 mA Output Current

Efficiency for Different Temperatures

Table 4.6 shows the simulation results for the efficiency, varying temperature and output current. The variation of the temperature has only a small impact on the efficiency. The efficiency drops with higher temperatures.

Table 4.6: Efficiency for Different Output Currents and Different Temperatures

Output Current	Efficiency			
	@ -20°C	@ 27°C	@ 85°C	@ 125°C
30 mA	96.8%	96.6%	96.5%	96.3%
60 mA	95.3%	95.0%	94.6%	94.2%
100 mA	70.7%	68.9%	67.1%	66.4%
200 mA	59.0%	58.2%	57.6%	57.6%

4.7.5 Current Consumption

Table 4.7 gives the simulation results for the current consumption with different temperatures and zero output current. The circuit is in common mode and performs no pumps,

since comparator N is '1'. Comparator L and comparator N are turned on. They are mainly responsible for the power consumption.

The simulation is started with nominal values for power supply and technology parameters.

Table 4.7: Current Consumption for Different Temperatures

Temperature	-20°C	27°C	85°C	125°C
Current Consumption	18.97 μ A	20.69 μ A	28.85 μ A	52.88 μ A

4.8 Conclusion of the Simulation Results

The simulation results show that the presented switched capacitor DC-DC converter can reach for low output currents (3 mA to 50 mA) a high efficiency of approximately 96%. A such high efficiency can be performed because the ratio of output voltage to input voltage is constant and an appropriate gain can be realized with two flying capacitors. The ripple of the output voltage for such output currents is about 3 mV. Furthermore, the simulation results show that a low switching frequency is beneficial for the efficiency of low output currents, as long as the converter pumps only with gain 2/3. This is because the switching losses are proportional to the switching frequency.

For output currents of 50 mA to 70 mA, a higher switching frequency is beneficial since more charge is transported to the output and gain 1 can be avoided or is not used that often. For this range of output currents, the efficiency is mainly depending on the switching frequency. But increasing the switching frequency is not cure-all solution, because only a limited amount of charge can be transported.

For an output current of 100 mA the efficiency is about 71.6% and for 200 mA about 59.8%. For such high output currents, the ripple of the output voltage is approximately 37 mV.

Chapter 5

Layout and Test Chip

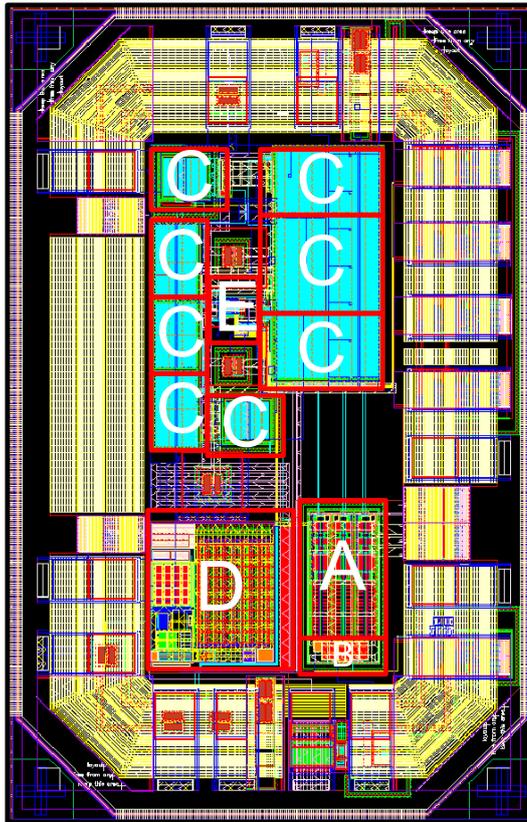
This chapter presents the layout of the implemented switched capacitor DC-DC converter. The layout is depicted in figure 5.1(a) and is described in table 5.1. Figure 5.1(b) depicts the produced chip. The core area is $322.045 \mu\text{m} \times 719.91 \mu\text{m}$. The total area is $700 \mu\text{m} \times 1100 \mu\text{m}$. The chip has this shape because it was produced on a multiple project wafer and there were constraints regarding the shape.

Figure 5.1(c) depicts the bond diagram for a QFP44 package. The pin for the output voltage and the pin to sense the output voltage are placed next to each other. Therefore, one bond wire crosses the chip. Figure 5.1(d) depicts the produced test chip and the package.

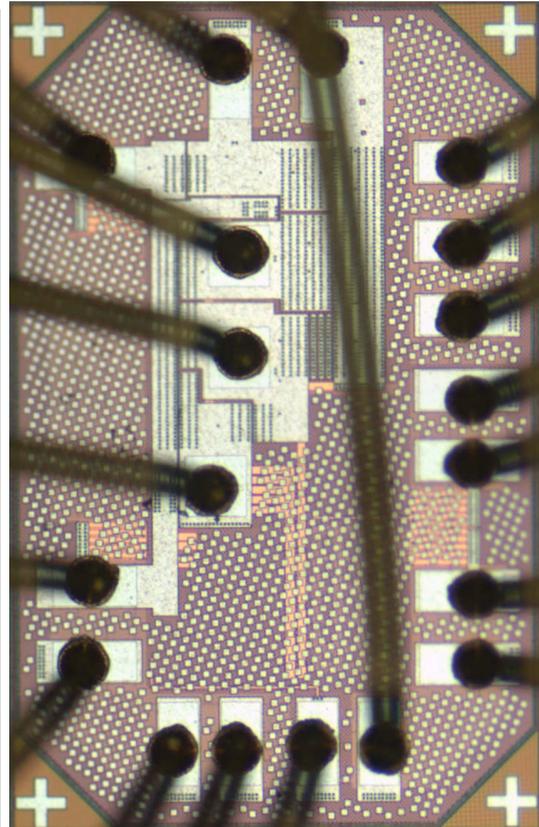
I did the layout of this test chip. A common centroid layout is applied for the voltage comparator and the current mirrors to achieve a good matching. For the layout of the controller, a place & route tool was applied. The switches are connect as low ohmic as possible among each other and to the power supply. The layout of the switches is non-conform to the ESD guidelines. The switches are not ESD proof, because it would require a lot of area which cost money. Therefore, the test chip is only a lab product.

Table 5.1: Switched Capacitor DC-DC Converter in 65 nm Low Power CMOS Technology

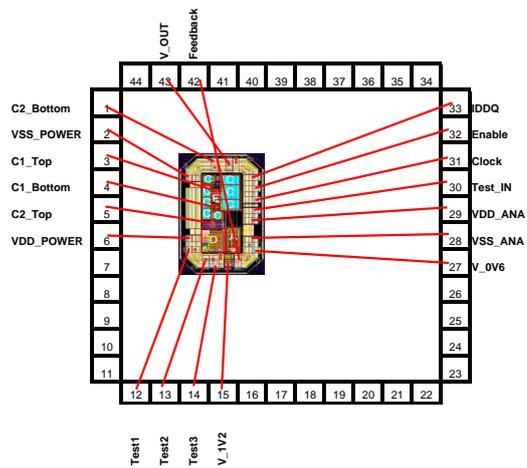
	Block	Area [mm²]
A	3 voltage comparator	0.022
B	resistive voltage divider	0.005
C	switches and driver	0.09
D	current generation for start up	0.032
E	controller	0.001
	core area	0.232
	total area	0.77



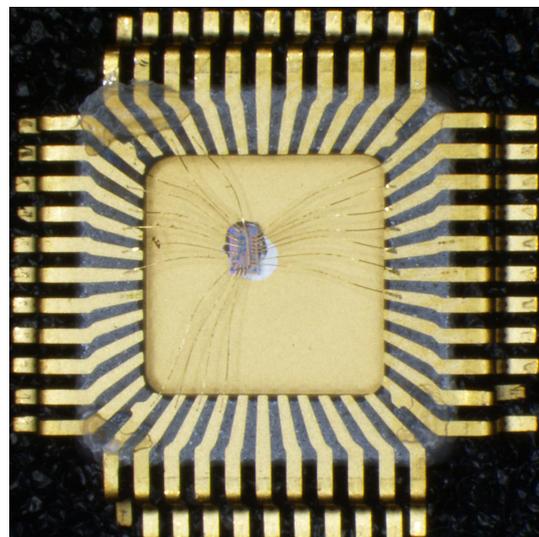
(a) Layout of the Switched Capacitor DC-DC Converter



(b) Photo of the Chip



(c) Bond Diagram for a QFP44 Package



(d) Photo of the Chip with Package

Figure 5.1: Layout, Bond Diagram and Photos of the Chip

Chapter 6

Measurements

This chapter presents the test board and the measurement results of the implemented switched capacitor DC-DC converter.

6.1 Test Board

The test board is designed with EAGLE 5.7.0 Light. The schematic of the test board is given in figure 6.1. Table 6.1 lists the used elements of the eagle library. Figure 6.2(a), 6.2(b) and 6.2(c) depict top and bottom of the test board and the assembly diagram.

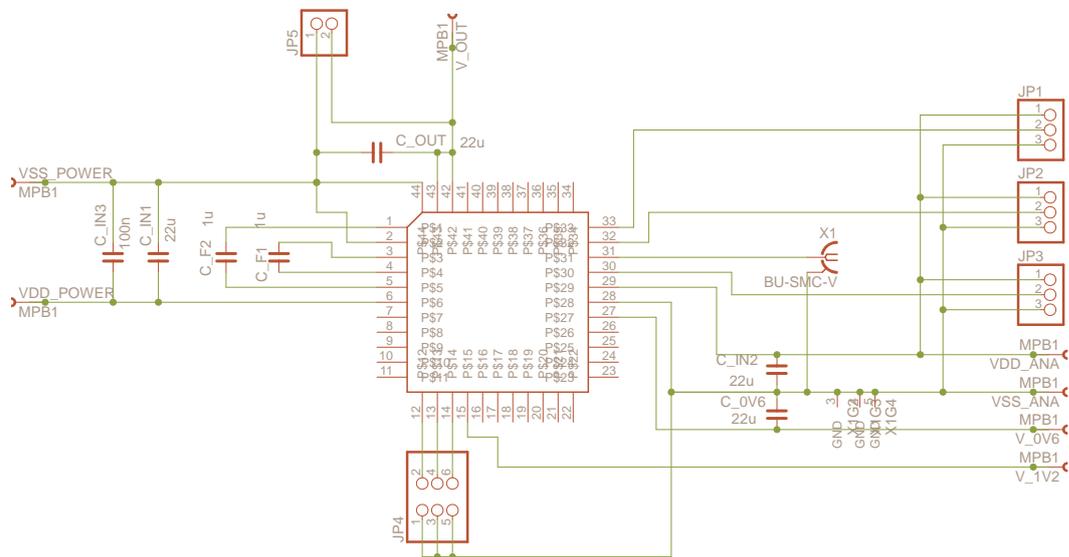


Figure 6.1: Schematic of the Test Board, used to Characterize the Test Chip

Table 6.1: Components of the Test Board

Name	Comment	Library	Device	Package
JP1,2,3		pinhead	PINHD-1X3	1X03
JP4		pinhead	PINHD-2X3	2X03
JP5		pinhead	PINHD-1X2	1X02
MPB1		con-hirschmann	MPB1	MPB1
BU-SMC-V		con-coax	BU-SMC-V	BU-SMC-V
C _{F1,2}	1 μ F, MLCCs	rc-master	C_0402(C_)	C0402
C _{IN1,2, OUT, 0V6}	22 μ F, MLCCs	rc-master	C_3216(C_)	C3216
C _{IN3}	100 nF, MLCCs	rc-master	C_2012(C_)	C2012
QFP44	device taken from:	exar	XR-2443Q	QFP-44

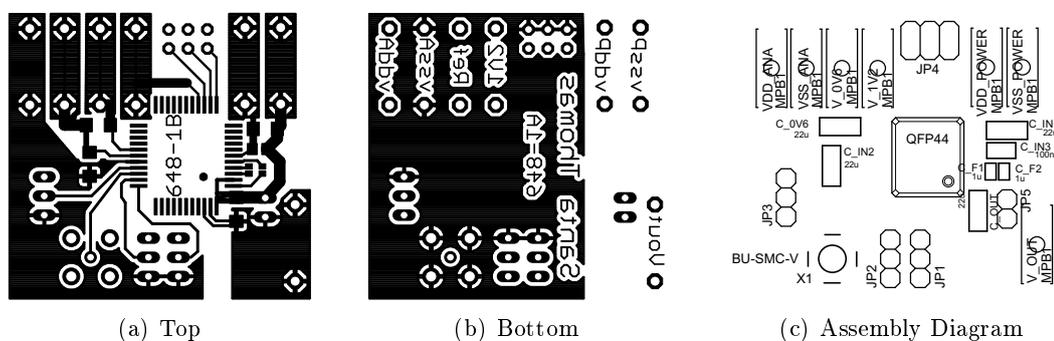


Figure 6.2: Masks for the Test Board and Assembly Diagram

The capacitors are placed as close as possible to the test chip in order to keep the parasitics as low as possible.

6.2 Measurement Results

The first measurement results with the test board show that the switched capacitor DC-DC converter works. The converter uses gain 1 earlier than expected. This is because the resistance of the switches, the parasitic resistance of the board and the package are bigger than the resistance in the simulation setup. This higher resistance has an impact on the load capability. Therefore, the converter has to apply gain 1 earlier to keep the output voltage in specification.

6.2.1 Efficiency for Different External Frequencies

Figure 6.3 shows the measured efficiency depending on the external frequency for different output currents. For low output currents up to 35 mA, the measurement results fit very well with the simulation results in figure 4.9. The efficiency of the converter decreases for an output current of 35 mA and higher frequencies. The measured peak efficiency for an external frequency of 0.5 MHz at an output current of 10 mA is 97%.

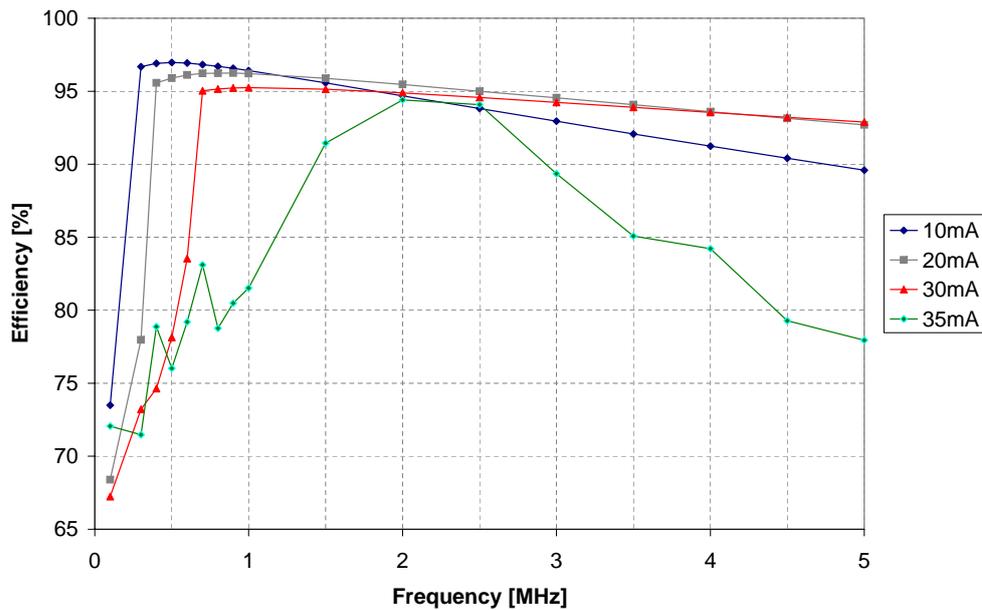


Figure 6.3: Efficiency vs. External Frequency for Different Output Currents

6.2.2 Efficiency for Different Output Currents

Figure 6.4 gives the measurement results for the efficiency varying the output currents for different external frequencies. The measurement results are similar to the simulation results in figure 4.10. The measured peak efficiency for 30 mA output current at an external frequency of 2 MHz is 95%.

Figure 6.5 gives the measurement results for the efficiency over the full load range. Thereby, the external frequency is 3 MHz. At an output current of 30 mA, the measured efficiency is 94%.

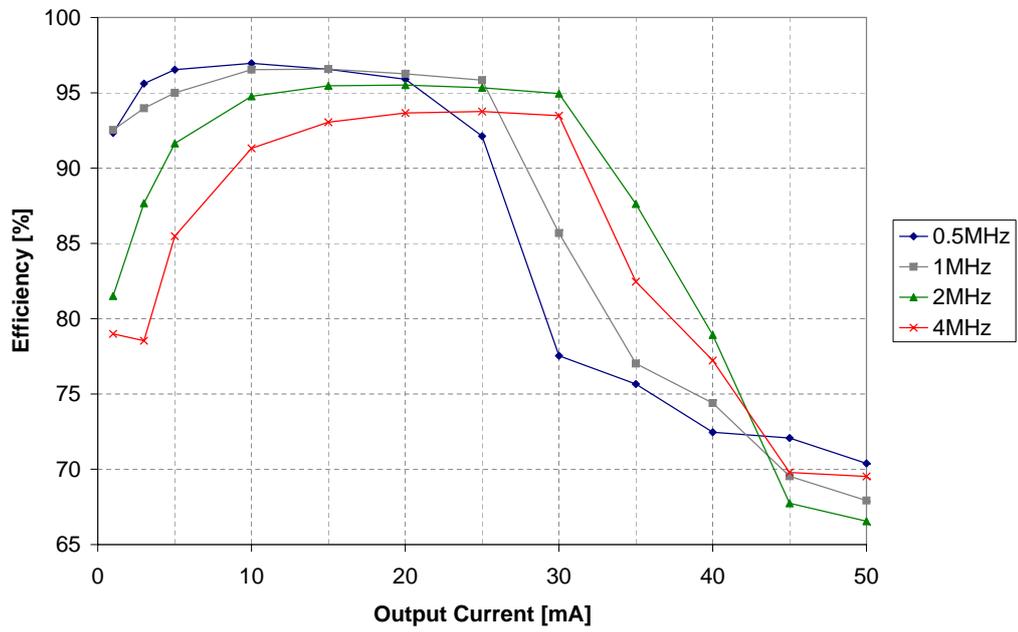


Figure 6.4: Efficiency vs. Output Current for Different External Frequencies

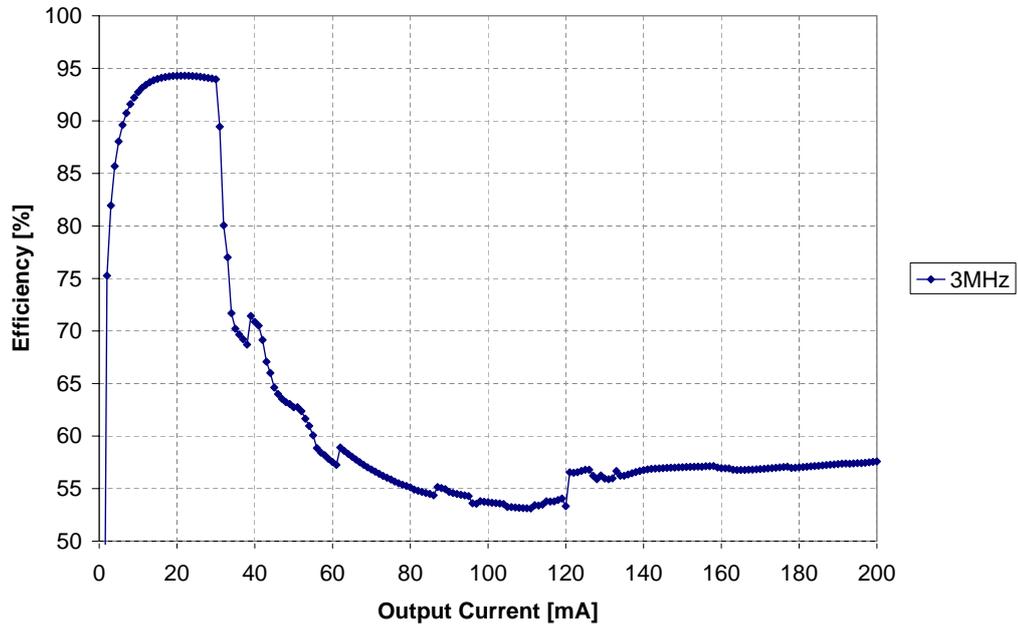


Figure 6.5: Efficiency vs. Output Current

6.2.3 Transient Behavior

In the following transient measurement, the circuit operates with an external frequency of 1 MHz. Figure 6.6 depicts the waveform of the output voltage for a load jump of the output current from 20 mA to 30 mA. The average output voltage drops from 1.19 V to 1.17 V. The ripple of the output voltage increases from 10 mV to 12 mV. The circuit operates only with gain 2/3.

Figure 6.7 depicts the waveform of the output voltage for a load jump of the output current from 30 mA to 40 mA. The average output voltage increases. Also the ripple of the output voltage increases as gain 1 is used.

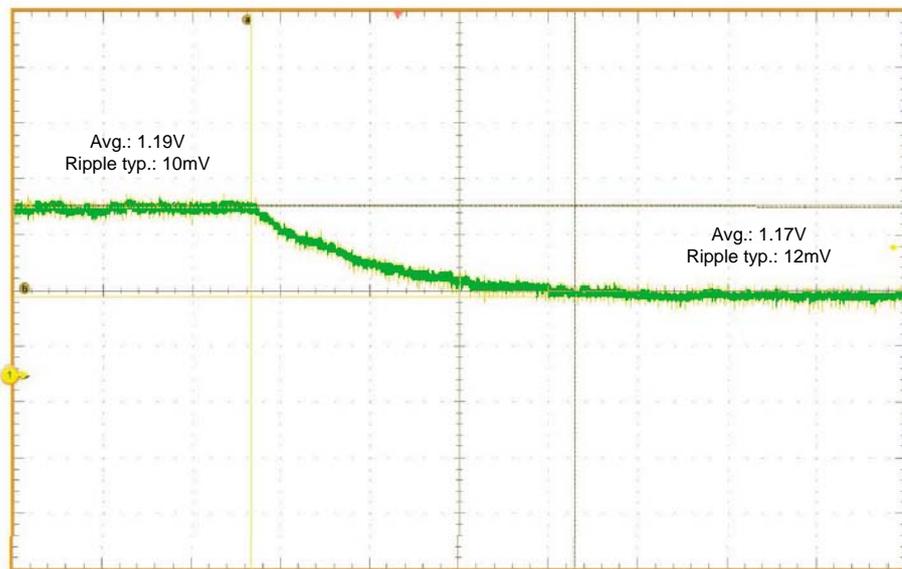


Figure 6.6: Waveform of the Output Voltage for a Load Jump of the Output Current from 20 mA to 30 mA

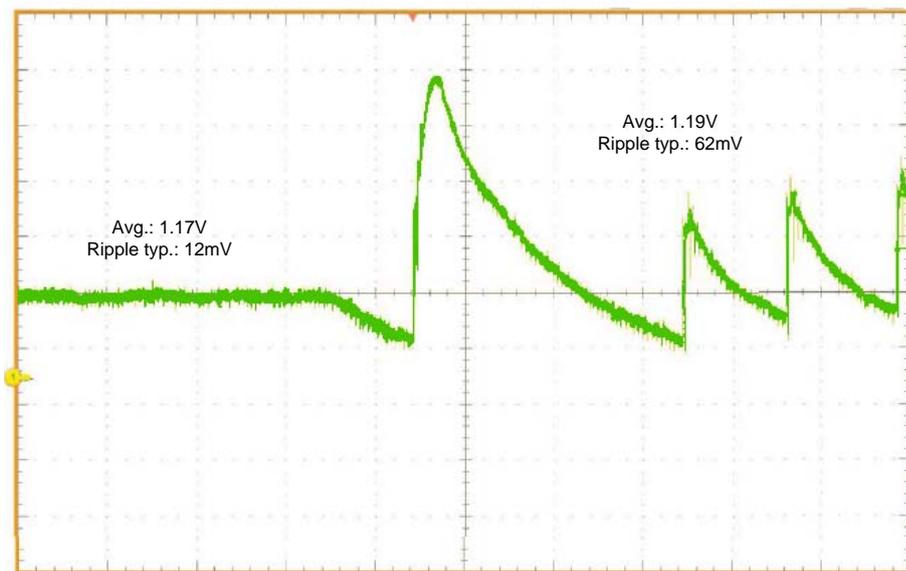


Figure 6.7: Waveform of the Output Voltage for a Load Jump of the Output Current from 30 mA to 40 mA

Chapter 7

Conclusion

The aim of this master's thesis was to design a highly efficient switched capacitor DC-DC converter in a 65 nm low power CMOS process. The converter operates with two additional external capacitors. A test chip was produced and evaluated in the lab. The measurement results show that the presented switched capacitor DC-DC converter converts an input voltage of 1.83 V into an output voltage of 1.2 V and delivers a nominal output current of 30 mA with an efficiency of 95%. At an output current of 10 mA, the peak efficiency is 97%.

The switched capacitor solution fits very well, if the ratio of output voltage to input voltage is similar to a realizable gain with the switch-capacitor network and if the output current remains low.

Chapter 8

Outlook

An important observation is that a higher output current decreases the average output voltage. With three flying capacitors it is possible to realize gain $3/4$ as described in [8]. With gain $3/4$ the output voltage is $V_{OUT} = V_{IN} \cdot \frac{3}{4} = 1.83V = 1.37V$. For a certain range of high output currents, the output voltage is decreased so that it is in specification. The efficiency is according to equation 1.2 given by:

$$\eta \approx \frac{V_{OUT}}{V_{IN} \cdot \text{gain}} = \frac{1.2V}{1.83V \cdot \frac{3}{4}} = 87.4\% \quad .$$

The efficiency for a certain range of output currents could be improved by the cost of an additional external flying capacitor and additional switches on the chip.

A further improvement is to design the switched capacitor DC-DC converter for a variable input voltage, since the voltage, coming from a battery, drops over time.

The start up time can be reduced with an additional voltage comparator. This voltage comparator can be slow and does not need a low offset voltage. The trigger level for the voltage comparator is lower than the trigger level for comparator L but it must be high enough so that the resulting voltages at the switches do not destroy them.

Voltage comparator N can be made smaller since the offset voltage does not have to be very low. This trigger level does not have to be as accurate as the trigger level for the lower limit.

Gain 1 can be made more efficient by extending the switch network with two additional switches. These additional switches can be used to connect also the second flying capacitor to the output capacitor. To increase the efficiency, also the size of the output capacitor and the size of the flying capacitor have to be considered.

Chapter 9

Appendix

```
1 library ieee , analog_hw;
2 use ieee.std_logic_1164.all;
3 use ieee.std_logic_arith.all;
4 use analog_hw.analog_pack.all;
5
6 — controller
7 entity CONTROLLER is
8 port( comp_hh      : IN std_logic;  — upper level
9       comp_h      : IN std_logic;  — nominal level
10      comp_l      : IN std_logic;  — lower level
11      en          : IN std_logic;  — enable
12      clk        : IN std_logic;
13      s_s1_2_3_4 : OUT std_logic;
14      s_s5       : OUT std_logic;
15      s_s6       : OUT std_logic;
16      s_s7_8     : OUT std_logic;
17      s_s9       : OUT std_logic;
18      en_out     : OUT std_logic;  — enable start up circuit
19      start_bit  : OUT std_logic;  — for clock manipulation
20      en_comp_h  : OUT std_logic;
21      en_comp_hh : OUT std_logic;
22      en_comp_l  : OUT std_logic;
23
24      test_in    : IN std_logic;
25      test_in1   : IN std_logic;
26      test_in2   : IN std_logic;
27      test_in3   : IN std_logic;
28      test_out1  : OUT std_logic;
```

```

29     test_out2      : OUT std_logic;
30     test_out3      : OUT std_logic;
31     );
32 end CONTROLLER;
33
34 architecture beh of CONTROLLER is
35     — switch config for different states: "s_s1_2_3_4_2_3_4, s5,
36     s6, s_s7_8, s9"
37     constant pd      : std_logic_vector(4 downto 0) := "11101"; —
38     power down
39     constant start    : std_logic_vector(4 downto 0) := "11100"; —
40     en, all off
41     constant cm      : std_logic_vector(4 downto 0) := "01100"; —
42     common mode
43     constant g1      : std_logic_vector(4 downto 0) := "10000"; —
44     gain 1
45     constant g2      : std_logic_vector(4 downto 0) := "11010"; —
46     gain 2/3
47
48     type state is (pd_state, en_state, cm_state, g2_state,
49     g1_state, off_state);
50     signal current_state, next_state : state;
51
52     begin
53
54     — Sequential part
55
56     seq: process(en, clk)
57     begin
58         if(en = '0') then current_state <= pd_state;
59         elsif(clk 'event and clk = '1') then current_state <=
60             next_state;
61         end if;
62     end process;
63
64     — Comb. part
65
66     comb: process(current_state, comp_h, comp_l, en)
67     begin
68         case current_state is
69             when pd_state => — power down
70                 if(en = '1') then next_state <= en_state;

```

```

64                                     else next_state <= pd_state;
65     end if;
66     s_s1_2_3_4 <= pd(4);
67     s_s5 <= pd(3);
68     s_s6 <= pd(2);
69     s_s7_8 <= pd(1);
70     s_s9 <= pd(0);
71     en_out <= '0' and en;
72     start_bit <= '1';
73     en_comp_hh <= '0' and en;
74     en_comp_h <= '0' and en;
75     en_comp_l <= '0' and en;
76 when en_state =>                    — start up with current source
77     if(comp_l = '1') then next_state <= cm_state;
78         else next_state <= en_state;
79     end if;
80     s_s1_2_3_4 <= start(4);
81     s_s5 <= start(3);
82     s_s6 <= start(2);
83     s_s7_8 <= start(1);
84     s_s9 <= start(0);
85     en_out <= '1' and en;
86     start_bit <= '1';
87     en_comp_hh <= '0' and en;
88     en_comp_h <= '0' and en;
89     en_comp_l <= '1' and en;
90 when cm_state =>                    — common mode
91     if(comp_l = '0') then next_state <= g1_state;
92     elsif(comp_h = '0') then next_state <= g2_state;
93         else next_state <= cm_state;
94     end if;
95     s_s1_2_3_4 <= cm(4);
96     s_s5 <= cm(3);
97     s_s6 <= cm(2);
98     s_s7_8 <= cm(1);
99     s_s9 <= cm(0);
100    en_out <= '0' and en;
101    start_bit <= '0';
102    en_comp_hh <= '0' and en;
103    en_comp_h <= '1' and en;
104    en_comp_l <= '1' and en;
105 when g2_state =>                    — gain 2/3
106     if(comp_l = '0') then next_state <= g1_state;

```

```

107                                     else next_state <= cm_state;
108     end if;
109     s_s1_2_3_4 <= g2(4);
110     s_s5 <= g2(3);
111     s_s6 <= g2(2);
112     s_s7_8 <= g2(1);
113     s_s9 <= g2(0);
114     en_out <= '0' and en;
115     start_bit <= '0';
116     en_comp_hh <= '0' and en;
117     en_comp_h <= '0' and en;
118     en_comp_l <= '1' and en;
119     when g1_state =>                                     — gain 1
120         next_state <= off_state;
121         s_s1_2_3_4 <= g1(4);
122         s_s5 <= g1(3);
123         s_s6 <= g1(2);
124         s_s7_8 <= g1(1);
125         s_s9 <= g1(0);
126         en_out <= '0' and en;
127         start_bit <= '0';
128         en_comp_hh <= '1' and en;
129         en_comp_h <= '1' and en;
130         en_comp_l <= '1' and en;
131     when off_state =>                                     — off state
132         if(comp_h = '0') then next_state <= cm_state;
133             else next_state <= off_state;
134         end if;
135         s_s1_2_3_4 <= start(4);
136         s_s5 <= start(3);
137         s_s6 <= start(2);
138         s_s7_8 <= start(1);
139         s_s9 <= start(0);
140         en_out <= '0' and en;
141         start_bit <= '0';
142         en_comp_hh <= '0' and en;
143         en_comp_h <= '1' and en;
144         en_comp_l <= '1' and en;
145     when others =>                                       — all switches off
146         next_state <= pd_state;
147         s_s1_2_3_4 <= '1';
148         s_s5 <= '1';
149         s_s6 <= '1';

```

```

150         s_s7_8 <= '0';
151         s_s9 <= '0';
152         en_out <= '0' and en;
153         start_bit <= '1';
154         en_comp_hh <= '1' and en;
155         en_comp_h <= '1' and en;
156         en_comp_l <= '1' and en;
157     end case;
158 end process;
159
160 -----
161 — Monitor internal signals
162 -----
163 test: process(test_in, comp_h, comp_l, comp_hh, test_in1,
164               test_in2, test_in3)
165 begin
166     case test_in is
167     when '0' =>
168         test_out1 <= comp_l;
169         test_out2 <= comp_h;
170         test_out3 <= comp_hh;
171     when '1' =>
172         test_out1 <= test_in1; — test_in* are connected in the
173         test_out2 <= test_in2; — schematic to the output of the
174         test_out3 <= test_in3; — FF of the current state
175     end case;
176 end process;
177 end beh;

```


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