Master Thesis

Design and Implementation of Low Power Circuits for a Sensor Interface for Biological Applications

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Abstract

In order to connect an RFID tag with a sensor for biological applications, a sensor interface has to be implemented. The goal of the system is to be able to measure the physiologic condition, proliferation and concentration of microbiological cell structures using their impedance without having to rely on the usage of batteries. This application can primarily be used in biological laboratories as well as hospitals to detect infections such as sepsis.

Since the system is powered with an RF field, the tag, along with the sensor interface, has to have a low power consumption. The goal of this master thesis is to implement different low power circuits, which are to be used in the sensor interface. Specifically, a comparison between adaptively biased operational transconductance amplifiers (OTAs) has to be made as well as a peak detector implemented.

Given an input differential voltage, adaptively biased OTAs have the ability to increase their output current in order to follow an input signal step quickly. As soon as the difference of the input signals decreases, the output current is reduced, along with the power consumption. In order to accomplish this, a variety of approaches are analyzed. In addition, the advantages and disadvantages of a new rail-to-rail OTA are considered. The different topologies are then compared with each other using different figures of merit.

The second part of this thesis includes the implementation of three different approaches for detecting the amplitude of a sinusoidal signal. All of the topologies meet the given criteria, however, due to a smaller area as well as lower power consumption, the low leakage peak detector has been layouted to be included in the interface. To obtain the simulation results, as well as a layout, a 120 nm CMOS process has been used.

Kurzfassung

Eine Sensorschnittstelle soll konstruiert werden, um einen RFID Tag mit Sensoren für biologische Applikationen zu verbinden. Ziel dieses Systems ist es, die Ausbreitung, Konzentration, sowie den physiologischen Zustand von Zellkulturen mittels einer Impedanzmessung zu erkennen, ohne auf die Verwendung von Batterien zurückgreifen zu müssen. Diese Applikation findet vor allem in biologischen Laboratorien Anwendung, kann aber auch in Krankenhäusern zur Detektierung von Infektionen wie Sepsis herangezogen werden.

Da das System über ein RF-Feld versorgt wird, muss der Tag und die Sensorschnittstelle energiesparend aufgebaut sein. Ziel dieser Diplomarbeit ist es, verschiedene stromarme Schaltungen zu implementieren, die in der Sensorschnittstelle zum Einsatz kommen sollen. Speziell handelt es sich hier um einen Vergleich zwischen 'adaptively biased' Transkonduktanzverstärkern (OTA) und einem Amplitudendetektor.

'Adaptively biased' OTAs besitzen die Eigenschaft ihren Ausgangsstrom bei anliegender Differenzeingangsspannung zu erhöhen, um einen Eingangssprung schneller folgen zu können. Sobald die Differenz der Eingangssignale wieder verringert wird, passt sich der Strom an um Energie zu sparen. Um dies zu erreichen werden verschiedene Lösungsansätze untersucht, sowie die Vor- und Nachteile eines neuen Rail-to-Rail Verstärkers erläutert. Die unterschiedlichen Topologien werden anhand von 'Figures of Merit' verglichen.

Für die Implementierung eines Amplitudendetektors werden drei verschiedene Lösungsansätze präsentiert. Alle Topologien erfüllen die Anforderungen, jedoch auf Grund des geringsten Platzbedarfs und Stromverbrauchs wurde schlussendlich der 'Low Leakage Peak Detector' im Layout umgesetzt. Für die Simulationen sowie das Layout wurde ein 120 nm CMOS Prozess verwendet.

Ich versichere hiermit, diese Arbeit selbständig verfasst, andere als die angegebenen Quellen und Hilfsmittel nicht benutzt und mich auch sonst keiner unerlaubten Hilfsmittel bedient zu haben.

I hereby certify that the work presented in this thesis is my own and that work performed by others is appropriately cited.

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Michael Stadler

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Contents

List of Figures

List of Abbreviations

A_v	Open Loop Gain
C_{Load}	Load Capacitor
g_m	Transconductance
V_{DD}	Supply Potential
V_{DSAT}	Saturation Voltage
V_{DS}	Drain-Source Potential
V_{GS}	Gate-Source Potential
v_{id}	Differential Input Voltage
V_{TH}	Transistor Threshold Voltage
AC	Alternating Current
ADC	Analog to Digital Converter
BJT	Bipolar Junction Transistor
BW	Bandwidth
FOM	Figure of Merit
FVF	Flipped Voltage Follower
FVFDP	Flipped Voltage Follower Differential Pair
GBW	Gain Bandwidth Product
Gnd	Signal Ground
HF	High Frequency
HSC	High Swing Cascode
ICMR	Input Common Mode Range
KCL	Kirchhoff's Current Law
LLPD	Low Leakage Peak Detector
NMOS	N-Channel Metal Oxide Semiconductor
OPA	Operational Amplifier
OTA	Operational Transconductance Amplifier
PM	Phase Margin
PMOS	P-Channel Metal Oxide Semiconductor
RF	Radio Frequency
RFID	Radio Frequency Identification
SD	Source Degeneration
SR	Slew Rate
UGF	Unity Gain Frequency
UHF	Ultra High Frequency

Chapter 1

Motivation

A passive Radio Frequency Identification (RFID) tag shall be used to make impedance measurements of microbiological cell structures. As power consumption is an issue, different topologies of adaptively biased operational amplifiers need to be analyzed to be implemented effectively to increase the performance of the analog to digital converter (ADC). Furthermore, different approaches to detect a signal amplitude are analyzed. The peak detector is used to find the maximum of the measurand from an impedance measurement, which is then converted by the ADC.

In order to observe proliferation, concentration and the physiologic condition of microbiological cells, impedance measurements are often used. Depending on the application, sometimes the growth environment may not be disturbed from the outside, making measurements impossible without the use of batteries. However, due to the harshness of the environment, either product lifetime may be reduced or the space consumption due to the battery may have to be increased. Using RFID, one is able to achieve the needed measurements while still only having to include a single tag within the growth environment. A buffer capacitor stores the energy generated by the harvester from a Radio Frequency (RF) field. Once the field is deactivated an accurate impedance measurement can be accomplished and the result sent back to the reader unit [10, 13].

A CellMonitor system from [13] is shown in Fig. 1.1. The micro-titer plate, which encases the sensors along with their tags, sits on top of the reader unit.

Figure 1.1: CellMonitor System

A block diagram of the functionality of the chip is shown in Fig. 1.2. The High Frequency (HF) and Ultra High Frequency (UHF) energy harvester converts the RF field and stores the gathered energy in the capacitor. The power management unit then supplies the different sections of the chip only as needed in order to reduce consumption. The reader activates a measurement and then turns off the field for a set amount of time. Therefore, the influence through the RF field upon the measurement is reduced. Once the measurement has finished, the collected data is stored via the data management unit. The reader unit requests the data which is then backscattered by the tag.

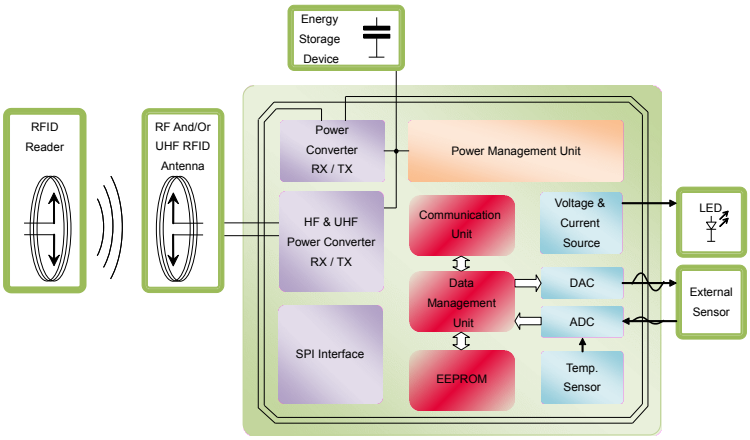


Figure 1.2: Block Diagram of the RFID Tag

Fig. 1.3 shows a more detailed representation of the sensor interface. The sections which are to include the work of this thesis are highlighted.

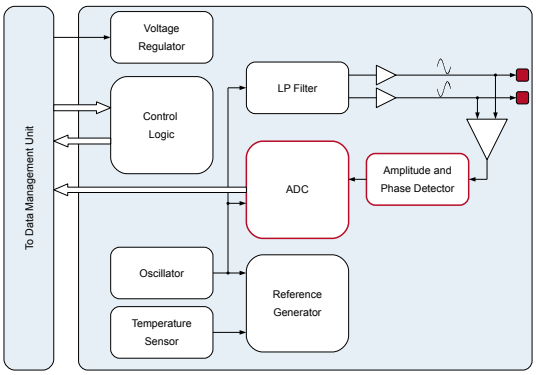


Figure 1.3: Block Diagram of the Sensor Interface

The application range for the tag including the sensor system is fairly wide spread. Besides the usage in laboratories to gather information about the growth of cell cultures, the system may be used in a medical environment to quickly detect diseases such as sepsis. Sepsis leads to blood abnormalities which can be detected using an impedance measurement [1].

Chapter 2

Class AB Operational Transconductance Amplifiers

The Operational Transconductance Amplifier (OTA) is a commonly used building block in electronic circuits. In analog chip design specifically it serves as subcomponent in more complex circuits such as ADCs, Bandgap References, Peak Detectors and many more.

Class A OTAs are defined as having a constant output current, independent of the input signal. This is a major disadvantage with regard to power consumption. Class B circuits have an output current depending on the input signal. When a large differential input signal (v_{id}) is applied, this is advantageous because the output is capable of adapting much quicker. However, if v_{id} is too small, the quiescent current becomes too small and the signal is distorted [9]. The class AB OTA tries to combine the advantages of class A and class B OTAs by having a large output current dependent on v_{id} and a quiescent current that is small to limit power consumption, but not too small in order to avoid distortion. The characteristics of the output current of a Class AB OTA can be seen in Fig. 2.1.

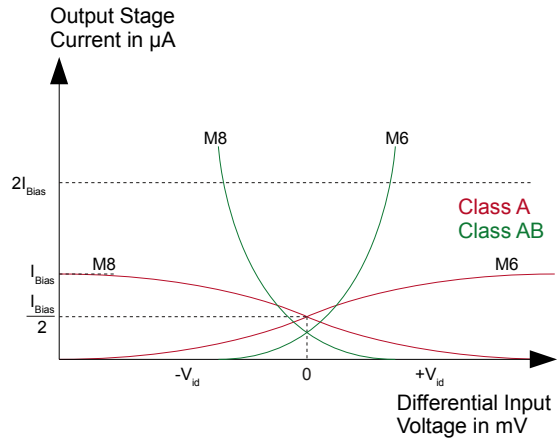


Figure 2.1: Output Current Adaptively Biased OTA

Transistors $M\,6, 8$ represent the output stage of an OTA as shown in Figs. 2.3 and 2.6.

2.1 Objective

The task at hand is to find an OTA to be used as a buffer which is capable of following an input step in 1 μs using as little energy as possible. The signal has to settle to less than 1 mV difference from the final value within the given time limit. In order to guarantee this, a monte carlo analysis has been made. It includes process and mismatch variations, where the standard deviation of the final value was chosen to be less than 1 mV. For the input step, a rise of 0.5 V was chosen due to the limitations of the 1.2 V technology. The input step along with the desired step response is shown in Fig. 2.2. The load capacitor to be used is 5 pF. Tab. 2.1 summarizes these requirements.

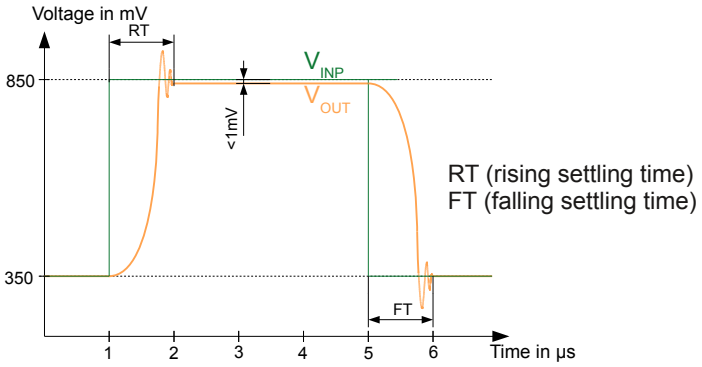


Figure 2.2: Input Step Response

Parameter	Value	Unit
Settling Time	1	μs
Offset	$\pm$1	mV
Input Step	350-850	mV
C_{Load}	5	pF

Table 2.1: Requirements

Usually, small signal parameters as well as the slew rate (SR) defined in Sec. 2.2.1, are used to compare the performance of different topologies as well as for defining the dimensions of the components of the circuit. The small signal parameters are obtained by linearizing the circuit for a certain operating point (AC Analysis [3]). This analysis is no longer valid when using Class AB, because the operating point changes depending on the applied input signal. Due to this restriction, the OTA's performance will be measured and compared by their static power consumption, as well as the energy needed to follow an input step.

2.2 Current Mirror OTA

The class A Current Mirror OTA in Fig. 2.3, even though it is single ended, has a very symmetrical shape due to its current mirrors M_3 and M_5 as well as M_4 and M_6. It is therefore much better suited to modifications than other OTA structures because the positive as well as the negative signal path have to be modified in the same way to increase the current given certain circumstances but limit it given others. The modification has to be equal on both sides in order to not decrease the overall performance of the OTA. Another advantage of this structure is the output stage. Given a technology with a maximum voltage of 1.2V, an output stage consisting of 4 transistors would significantly reduce the output swing, even though the gain would benefit due to the larger output resistance. If needed, cascode transistors can be included in this structure to increase the overall gain of the OTA.

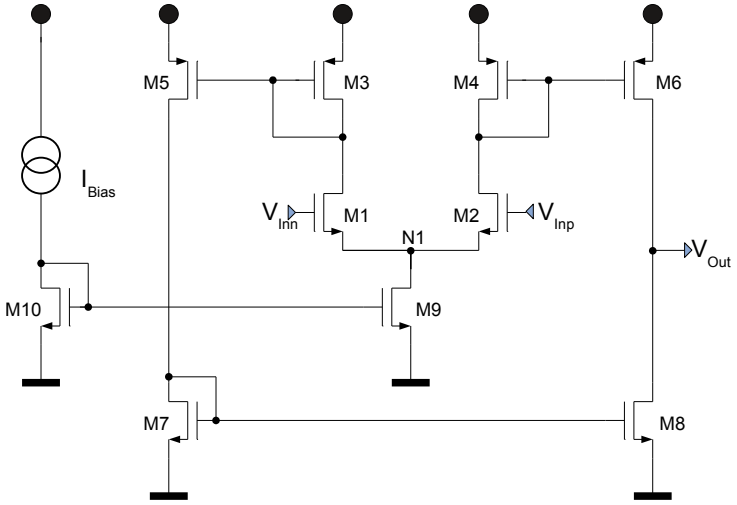


Figure 2.3: Class A Current Mirror OTA

2.2.1 Basics

The major performance characteristics of an OTA are the small signal characteristics, which can be found in the bode plot. Fig. 2.4 shows the open loop gain (A_v), bandwidth (BW), phase margin (PM) and unity gain frequency (UGF). The transconductance (g_m), needed to calculate A_v and the UGF, is usually determined by the input differential transistor pair. However, in this configuration it can be improved by the scaling factor of the PMOS current mirror (Eq. 2.2.1).

$$G_m = g_{m1}\,\frac{g_{m5}}{g_{m3}} = g_{m2}\,\frac{g_{m6}}{g_{m4}} \tag{2.2.1}$$

Even though the increase in g_m is a significant improvement of the performance of the OTA, it comes at the cost of power consumption, even in steady state.

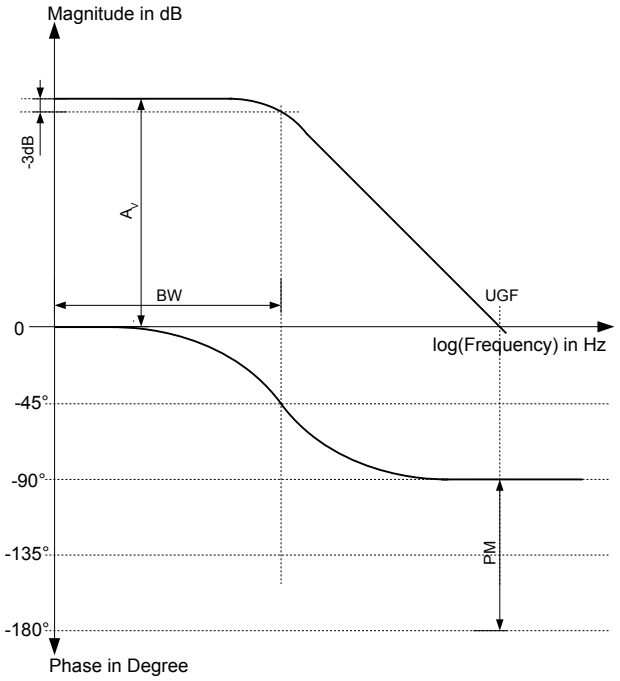


Figure 2.4: Bode Plot

A_v of the OTA is given by the product of the transconductance and the output resistance (2.2.2).

$$A_v = G_m \ (r_{ds6} \parallel r_{ds8}) \tag{2.2.2}$$

Assuming the OTA is stable it therefore has a PM of reasonable value. A PM of 60° is suggested by [12] as the step responce shows a good trade-off between settling time and ringing. Having this kind of PM means that the non-dominant pole is at a much higher frequency than the UGF. The non-dominant pole is at the nodes of the gates of M_3 and M_4 due to symmetry. Given the assumption, the gain bandwidth (GBW) product is estimated to be equal to the UGF. The GBW product is dependent on the transconductance as well as the total capacitance at the output node (2.2.3). This capacitance is approximately the size of the load capacitor (C_{Load}).

$$\text{GBW} = \frac{G_m}{2\pi C_{Load}} \tag{2.2.3}$$

Furthermore the output swing has previously been mentioned. Its maximum can be calculated by subtracting the saturation voltage of M_6 and M_9 from V_{DD} (2.2.4).

$$V_{OutSwing} = V_{DD} \text{ - } V_{DSAT-M6} \text{ - } V_{DSAT-M8} \tag{2.2.4}$$

The topology in Fig. 2.3 shows an NMOS input stage, which enables the OTA to accept higher input voltages compared to a PMOS input stage. The input common mode range (ICMR) can be calculated by finding the upper and lower voltage limits in order for all of the OTA's transistors to stay in saturation. The former is found by subtracting all voltage drops from V_{DD} to the input gate (2.2.5). To find the latter all voltage drops from the input gate to ground (Gnd) are added together (2.2.6). Eq. 2.2.8 shows the result for the input common mode range. Similarly, the input range for an OTA with a PMOS input stage can be found in Eq. 2.2.8.

$$V_{InMax} = V_{DD} \text{ - } V_{DSAT-M3} \text{ - } V_{TH-M3} + V_{TH-M1} \tag{2.2.5}$$

$$V_{InMin} = V_{DSAT-M11} + V_{DSAT-M1} + V_{TH-M1} \tag{2.2.6}$$

$$\begin{aligned} V_{ICMR-N} = V_{DD} \text{ - } V_{DSAT-M3} \text{ - } V_{TH-M3} + V_{TH-M1} \\ -(V_{DSAT-M11} + V_{DSAT-M1} + V_{TH-M1}) \end{aligned} \tag{2.2.7}$$

$$V_{ICMR-N} = V_{DD} \text{ - } 3 \cdot V_{DSAT} \text{- } V_{TH} \tag{2.2.8}$$

Another parameter to measure the performance of an OTA is the SR. It is a large signal measurement and uses an input step to see just how fast the OTA can respond when connected as follower. The theoretical maximum SR can be calculated as shown in Eq. 2.2.9. The SR of an OTA usually does not reach the maximum value for longer periods of time because this assumes that all of I_{Out}, which would be equivalent to I_{Bias}, is charging or discharging C_{Load}. This is only the case if there is a large differential voltage at the input. If the differential voltage decreases, I_{Bias} starts to split more evenly across the differential pair according to the voltage applied.

$$\text{SR} = \frac{I_{Bias} \ \frac{g_{m5}}{g_{m3}}}{C_{Load}} \tag{2.2.9}$$

Note: The equations are obtained from [4].

Given the equations above, it can be be seen that, if available in the technology, using an input transistor with a lower V_{TH} and larger g_m is advantageous as the ICMR as well as the GBW and A_v are increased.

2.2.2 Implementation

Given the specifications in Sec. 2.1 as well as the functionality of the current mirror OTA in Sec. 2.2.1, the circuit shown in Fig. 2.3 was implemented. Instead of using the GBW to find g_m of the input stage and then the biasing current, by applying Eq. 2.2.10 the SR can be used to approximate the current needed to charge C_{Load} by 0.5 V. However, this is only an estimation, because the output current only equals I_{Bias} at a large V_{id}. Once the output approaches the input signal, the differential pair will start to divide the current, decreasing the output current. Therefore more biasing current will eventually be needed to achieve the desired input step response.

$$0 < \frac{g_m}{I_D} < 30 \text{ [9]} \tag{2.2.10}$$

The above equation can be used to quickly estimate the operating region of a transistor. In most cases the transistor will be used in saturation. While a $\frac{g_m}{I_D}$ <5 is commonly used for current mirrors, a $\frac{g_m}{I_D}$ between 10 and 15 is a good value for an input stage. Knowing the $\frac{g_m}{I_D}$ at a given current, the transistor size can be found by implementing a circuit with an ideal current source and a transistor configured as diode. Using this circuit, simulations can be done to find the width and length according to the desired givens.

Having estimated the size of the input stage, the transconductance can further be improved by increasing the width of the transistor which will eventually result in forcing it into weak inversion. This results in the MOSFET becoming similar to a BJT[9]. The advantage of this is that it enables one is to obtain the highest g_m possible. This in turn increases the gain as well as the gain bandwidth product of the amplifier. The length of the input stage transistors should not be kept at the minimum length of the process to decrease the offset. Roughly quintupling the length, compared to its minimum results in a larger area which will decrease mismatch and therefore keep the offset lower.

The remaining transistors of the OTA in Fig. 2.3 are current mirrors. As mentioned above, a low $\frac{g_m}{I_D}$ is generally desired. This will result in a small $\frac{\mathrm{W}}{\mathrm{L}}$ which causes the diode connected transistor of the current mirror to set a higher gate-source voltage (V_{GS}). Increasing the length of a transistor stabilizes its threshold voltage (V_{TH}) over process variations. It furthermore maximizes V_{GS} which in turn also reduces the effects of a varying V_{TH} allowing for the current to be mirrored more accurately. Given a process with different transistors, one implemented with a small g_m is to be used to further increase its V_{GS}.

As seen in Eq. 2.2.9, the output current can be further increased by scaling the PMOS current mirrors. This is a trade-off, however, as the SR will be increased proportionally but the static power consumption will be as well. For this comparison, these current mirrors were implemented with a ratio of 1:3.

The same approach was used to design an OTA with a PMOS input stage. However, it was a goal to roughly keep the layout area of the block similar for the two OTAs. This

was achieved as seen in Tab. 2.2.

Input Stage	**Area in μm^2**
NMOS	512
PMOS	578

Table 2.2: OTA Size

2.2.3 Results

The top plot in Fig. 2.5 shows the sum of the rise and fall times of the current mirror OTA with an NMOS input stage (CM N-OTA, Fig. 2.3) as well as a PMOS input stage (CM P-OTA, Fig. A.1) over temperature. On the bottom of the plot, the total energy used during the respective settling times is shown. Since an NMOS input stage is compared to a PMOS, the energy during a positive as well as a negative input step has to be observed due to the differences in topology. Given a positive input step, the NMOS input stage causes I_{Bias} to flow through M_2 and M_4 (Fig. 2.3). Therefore, M_6 will either have the same or a scaled current yielding a total of 2 branches with current flow. The PMOS input step, given the same input signal, draws the current through $M_{1,3,5,7}$ and M_8 where M_5 and M_8 are used as current mirrors (Fig. A.1). This in total yields three branches and will eventually result in a higher energy consumption. So in order to equally record the current consumption, both input steps are measured and their respective energies recorded. Note that the PMOS topology does in fact need one more branch to mirror the current from M_{12} to, eventually, M_9. This however is included, because the bias current usually is supplied to an NMOS transistor and not copied through a PMOS transistor.

Given a similar area for the two OTAs the one with the NMOS input stage is expected to perform better. At the same size the NMOS transistor will have a higher transconductance due to the higher mobility of electrons compared to holes, as can be found in [9],[5],[12] and [2]. As seen in Eq. 2.2.1, the g_m of the input stage determines the transconductance for the overall OTA. An OTA with a higher g_m, given the same output resistance, will have a higher gain and a higher GBW. Eq. 2.2.11, obtained from [11], shows the dependence of the amplifier error E, which is the difference between the ideal and actual output voltage of the amplifier, on the open loop gain.

$$E = \frac{V_{In}}{1 + \mathrm{A}\beta} \tag{2.2.11}$$

While the applied differential voltage is much greater than the error, the OTA will distribute all of I_{Bias} accordingly to V_{id}, therefore achieving its maximum SR. As the output approaches the input voltage I_{Bias} will be divided up again until the voltages are equal. From this it is apparent that at a higher gain, the maximum SR will be achieved

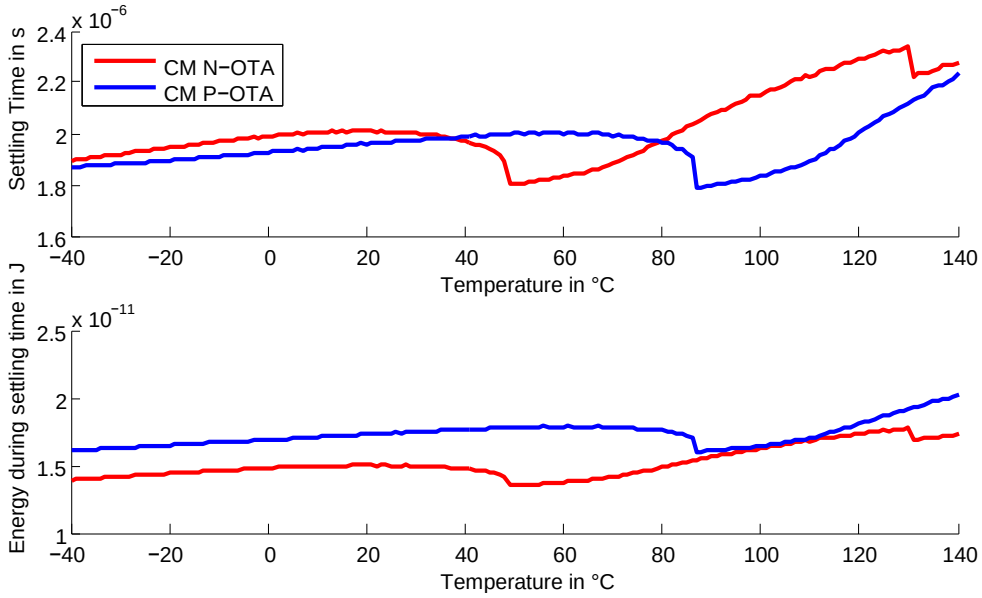


Figure 2.5: Settling Time and Energy over Temperature NMOS vs. PMOS

for a longer period of time, therefore decreasing the overall settling time of the OTA. Since, as established above, the OTA with the NMOS input stage has a higher gain, it is expected to need less time to accomplish the input step responses.

Overall, looking at the curves, it can be seen that the settling time increases with temperature. At low temperatures V_{TH} is higher, causing a lower voltage at node N1 in Fig. 2.3 affecting the current through M_9. As temperature increases, the threshold voltage of a transistor decreases, yielding an increase in potential at node N1. This results in an increase in I_{Bias} over temperature. The transistors of the input stage operate in weak inversion at room temperature. An increase in their currents results in a decrease in $\frac{g_m}{I_D}$ eventually driving the transistor into the saturation region. In consequence, the transconductance of the OTA decreases, affecting small signal parameters such as the gain, unity gain frequency and phase margin as well. As mentioned above, less gain will increase the settling time.

The sudden decreases in the curves occur due to the aforementioned changes in small signal parameters. A different phase margin represents changes in the settling behavior. Specifically, the overshoot is inversely proportional to the phase margin. Given the increase in current, no change in the pole locations in the bode plot results in an increase in phase margin. If the overshoot decreases to less than the 1 mV specified to be the maximum allowed offset, the final input step response time decreases significantly. This case happens to the NMOS input stage OTA if the temperature is increased from 48°C to 49°C and from 130°C to 131°C. While the former occurs given a positive input step,

the latter is a result of a negative input step response. The PMOS input stage OTA shows the same reaction given a positive input step and a temperature increase from 86°C to 87°C. At the cost of a smaller GBW, the phase margin could be increased to avoid those drop offs if a more linear application over temperature is needed.

The standard deviation of the output variation over process and mismatch was determined to be 0.97 mV for the NMOS input stage OTA. The PMOS input stage topology has a standard deviation of the final output value of 0.96 mV.

Tab. 2.3 shows the quiescent and active current consumption of the OTA as well as the maximum and minimum output current at room temperature. The quiescent current $I_{V_{DD}}$ is measured at input voltages of 350 and 850 mV.

Input Stage	$I_{Out-Min}$ in μA	$I_{Out-Max}$ in μA	I_{Vdd} in μA
NMOS	2.24	4.66	6.01-6.32
PMOS	2.14	4.05	7.35-7.76

Table 2.3: Quiescent Current Consumption regular current mirror OTAs

From the quiescent current it can be seen that the PMOS input stage uses more energy. In this comparison I_{Bias} is not scaled, therefore the extra branch makes a big difference. However even if a scaled version was implemented, the area consumption would increase.

Since no noise requirements are given, the NMOS input stage OTA will be used throughout this thesis because, as shown, it consumes less energy given a similar area to achieve the desired input step response.

2.3 Class AB Current Mirror OTA: Source Degeneration

Generally class AB OTAs can be split into two categories, one type modifies the current through the input, the other the output stage to achieve class AB. The modification of the input stage is done by using a Flipped Voltage Follower and will be discussed in Sec. 2.5.

The first example of a modified output stage is shown in Fig. 2.6 taken from [8]. Transistors M_{11} and M_{12} have been added to the regular current mirror OTA from Fig. 2.3 similarly as if they were used as source degeneration. Even though the modification is done in the branch of the input stage, the current change occurs only in the output stages of the OTA, therefore not influencing the current through the input transistors M_1 and M_2.

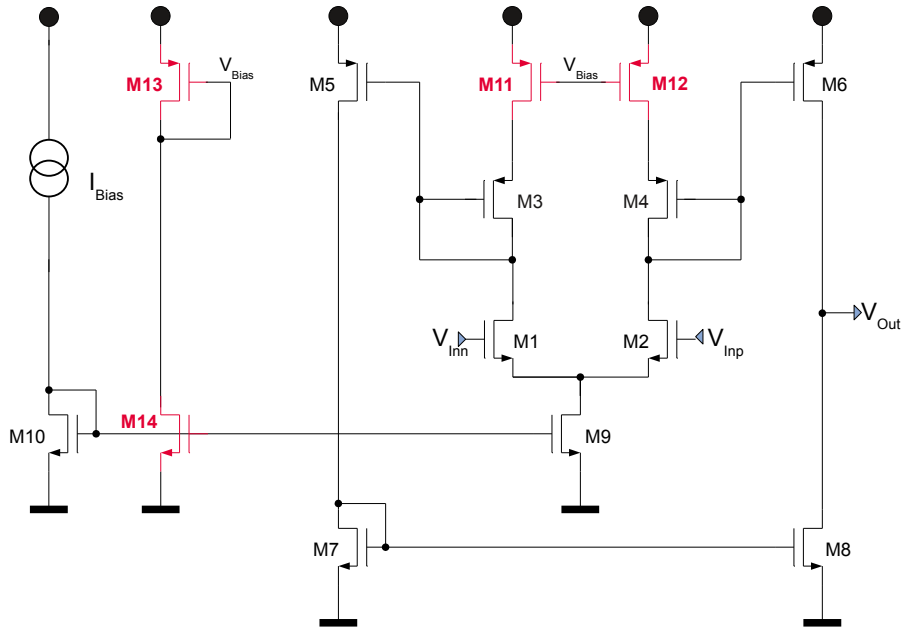


Figure 2.6: Class AB Current Mirror OTA Source Degeneration

2.3.1 Basics

Usually source degeneration with a resistor is used to increase the output resistance [12]. In this case the degeneration transistor is used to generate a voltage drop depending on the current through its branch. At v_{id} approximately zero, the transistor is biased in the linear region and therefore has a low V_{DS}. If v_{id} increases, the current through one branch increases and V_{DS} of the 'degeneration' transistor along with it. The current mirroring transistors M_5 and M_6 see the sum of $V_{GS-M3,4}$ and $V_{DS-M11,12}$ as their V_{GS}. This causes an increase in output current beyond the quiescent current, classifying it as class AB.

Achieving a higher output current using this structure comes at the price of having a higher quiescent current. Close examination of transistors M_{11} and M_{12} shows that they are capable of switching from the linear to saturation region, therefore increasing their V_{DS} just as planned. However, the minimum value for V_{DS}, if zero v_{id} is applied, is not equal to zero. Therefore the current flow of the overall circuit will be increased. Furthermore, the input common mode range should be considered when v_{id} is large because V_{DS} reaches its maximum at this point. The maximum for the ICMR of the circuit in Fig. 2.6 can be seen in Eq. 2.3.1.

$$V_{InMax} = V_{DD} - V_{DS-M12} - V_{TH-M4} - V_{DSAT-M4} + V_{TH-M2} \tag{2.3.1}$$

The maximum of $V_{DS-M11,12}$ can be limited by increasing the ratio of $\frac{W}{L}$ which then in turn decreases the maximum output current. Last but not least, an extra branch to generate V_{Bias} will always be needed and therefore cost energy even if a ratio to I_{Bias} is chosen.

2.3.2 Implementation

The dimensions of the input pair transistors along with the current mirrors were implemented as described in Sec. 2.2.2. A factor of three has been used to permanently increase the output current, just as has been done with the regular current mirror OTA. In order to generate V_{Bias} for M_{11} and M_{12}, an extra branch with a diode connected transistor has to be used. M_{13} is used to generate a voltage which allows M_{11} and M_{12} to change their operating region if v_{id} is applied. The different operating regions are shown in Fig. 2.7. In order to determine how to chose the dimensions of M_{13}, the power consumption shall be temporarily neglected. In this case, the current mirrored by M_{14} is I_{Bias}. Eq. 2.4.2 states the condition for a transistor to be in saturation. Since the transition from linear to saturation region is given by Eq. 2.3.3, obtained from [9], the diode connected transistor will be comfortably in saturation. M_{13} sets V_{Bias} for M_{11} and M_{12}. If v_{id} is zero, I_{Bias} will be split equally and M_{11} and M_{12} each get $\frac{I_{Bias}}{2}$. As seen in Fig. 2.7, this puts M_{11} and M_{12} in the linear region, each therefore having a small V_{DS}. If a large v_{id} is applied, I_{Bias} will be steered according through either M_{11} or M_{12}. This transistor will then move into the saturation region, equaling the diode connected transistor M_{13} and generating a larger V_{DS}. As a result V_{GS-M5} consists of the sum of V_{GS-M3} and V_{DS-M11} and V_{GS-M6} consists of the sum of V_{GS-M4} and V_{DS-M12}. This yields the desired effect of an increased output current given a nonzero v_{id}.

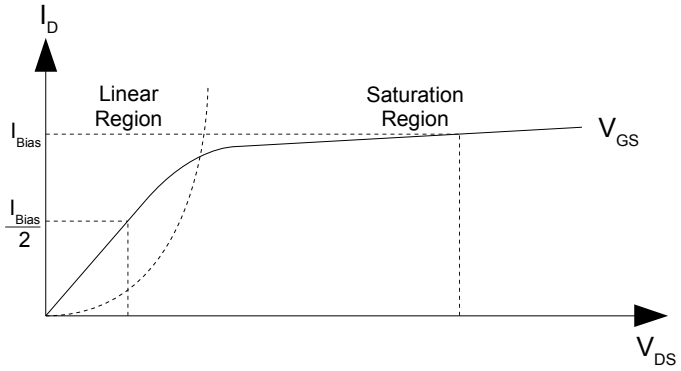


Figure 2.7: Drain Current vs. Drain-Source Voltage

$$V_{DS} \geq V_{GS} - V_{TH} \tag{2.3.2}$$

$$V_{DS} = V_{GS} - V_{TH} \tag{2.3.3}$$

Finally, in order to reduce the power consumption, especially of the branch generating V_{Bias}, a scaling factor can be used. However the aforementioned factor should be maintained for the circuit to work as described.

2.3.3 Results

The result time and energy consumption if an input step is applied to the current mirror OTA with source degeneration (A-Bias SD1) is plotted against the regular current mirror OTA (CM N-OTA) in Fig. 2.8. At low temperatures the settling time of both OTAs, shown on top, is almost equivalent. A good comparison can be made, and it can be seen in the bottom half that the OTA with adaptive biasing needs slightly less energy to complete the input step response. However, a clear-cut advantage cannot be seen. Note that here only the positive input step settling time and energy are compared. This is possible because the input stage is NMOS in both cases, so the general functionality is the same, and there is no need to include the negative rise time as well, as it will show similar results. Having analyzed the rise time and energy of the regular current mirror OTA in 2.2.3, this current mirror OTA with adaptive biasing shows a very similar behavior over temperature. The settling time increases with temperature, as does the energy, due to the aforementioned events. The significant change in phase margin and overshoot occurs when increasing the temperature from 2°C to 3°C. Overall the source degeneration delivers a higher SR but the overall energy of the OTA increases, making the impact of adaptive biasing very minor. The standard deviation of the final output value over process and mismatch was simulated with 1 mV.

A third curve is shown in Fig. 2.8 labeled with A-Bias SD2. This is an improved version of the current mirror OTA with source degeneration with regards to settling time and energy used at the cost of an increasing offset. Reducing the length of the input stage transistors decreases the gate-source capacitance and therefore increases the transit frequency of the transistor itself. On the other hand, the threshold voltage fluctuates more due to mismatch. This substantially increases the offset of the circuit, as the input stage is still operated in weak inversion using the same ratio of $\frac{W}{L}$ as A-Bias SD1. This is included to show that an improvement with this topology is possible. The final standard deviation of the offset was found to be 1.6 mV.

Table 2.4 shows the quiescent and active current consumption of the OTA architectures at room temperature.

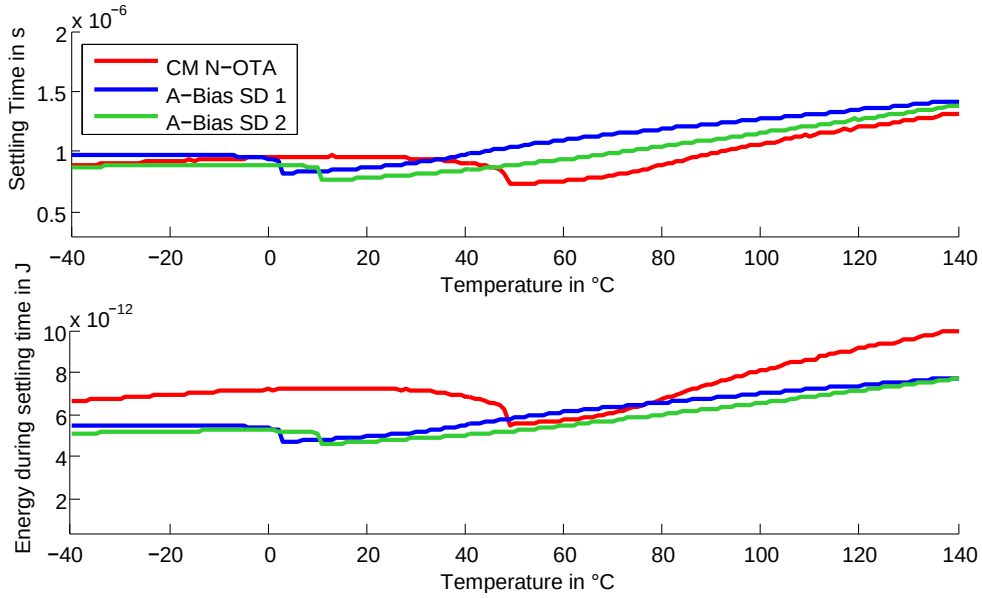


Figure 2.8: Current Mirror OTA vs. Adaptively Biased OTA SD

Input Stage	$I_{Out-Min}$ in μA	$I_{Out-Max}$ in μA	$I_{Vdd-Min}$ in μA	$I_{Vdd-Max}$ in μA
A-Bias SD1	1.5	4.15	3.86	5
A-Bias SD2	1.22	4.14	3.14	4.87
CM N-OTA	2.24	4.66	6.01	6.32

Table 2.4: Quiescent Current Consumption A-Bias SD1 & CM N-OTA

Even though the energy consumed during the input step is not reduced, the theory of adaptive biasing is clearly shown here. While the maximum output currents between the three types are very similar, the source degeneration implementations only needs about one half of the current of the regular OTA to maintain the output.

2.4 Class AB Current Mirror OTA: High Swing Cascode

Another approach to increase the current of the output stage is to switch the degeneration transistor with the diode connected transistor. The result can be seen in Fig. 2.9.

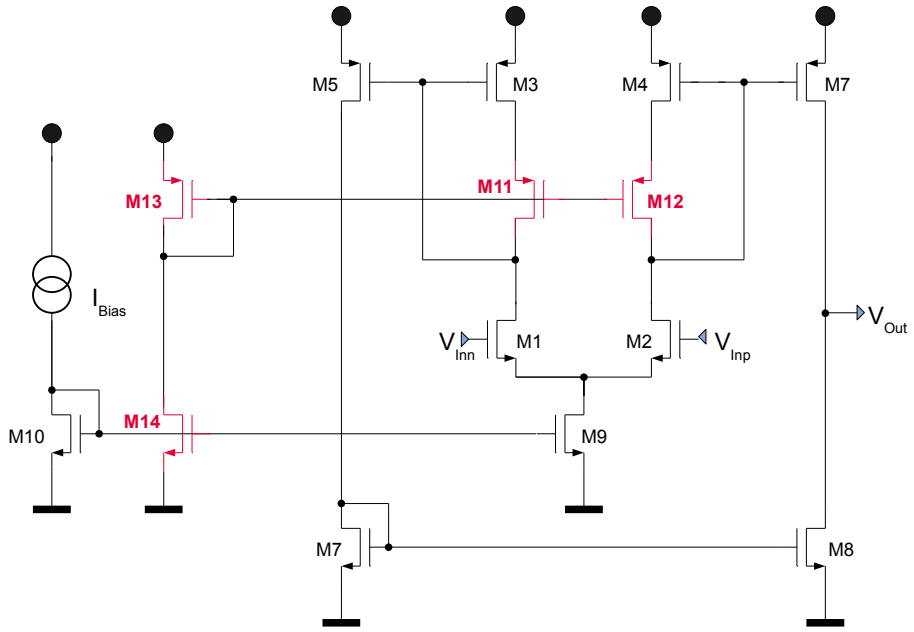


Figure 2.9: Class AB Current Mirror OTA High Swing Cascode

2.4.1 Basics

The final outcome of this approach is the same as previously. The goal is to increase the V_{GS} of the current mirror transistors M_5 and M_7 given a nonzero v_{id}. While in steady state, all transistors are in saturation and M_{11} and M_{12} act as cascode transistors just like a high swing cascode. In order to increase the output current when needed, M_{11} and M_{12} are used to force M_3 and M_4, respectively, into the linear region when v_{id} is applied. More current and a stable V_{GS} for M_{11} and M_{12} will cause them to increase the potential at their sources. This decreases V_{DS} of M_3 and M_4, eventually forcing them into the linear region. Once in triode region, V_{GS} increases, yielding the desired result.

In terms of quiescent current, this circuit should be better than the previous, because when v_{id} is zero, M_3 and M_{11} as well as M_4 and M_{12} work like a high swing cascode and do not generate any unnecessary voltage which could then be converted to current by the mirroring transistors. In comparison, the source degeneration topology, will always result in a larger $V_{GS-M5,6}$ because $V_{DS-M11,12}$ will not be zero even if there is no differential voltage applied. Considering the input common mode range while v_{id} is nonzero the voltage at the gate of M_3 and M_4 cannot drop lower than the sum of V_{DS-M9} and $V_{DS-M1,2}$ in order for the circuit to work properly. Note that $V_{DS-M1,2}$ at v_{id} nonzero can be of substantial size due to a large V_{GS}.

2.4.2 Implementation

An extra branch consisting of M_{13} and M_{14} is creating V_{Bias} for M_{11} and M_{12} again. Eq. 2.4.1 shows the conditions for M_3 and M_4 to be in saturation. Similarly to before, the power consumption is temporarily ignored and I_{Bias} is chosen to generate V_{Bias}. This results in M_{11} and M_{12} having $\frac{1}{2}\ V_{GS-M13}$, therefore leaving enough of a voltage drop from their sources to V_{DD} for M_3 and M_4 to operate in saturation, given steady state conditions. Increasing v_{id} causes an increase in current through either M_{11} or M_{12} and an increase in their respective V_{GS} as seen in Eq. 2.4.2. This limits V_{DS} of M_3 or M_4, eventually forcing it into the linear region. The conditions for entering the linear region are shown in Eq. 2.4.3, while the dependency of I_D and V_{GS} in triode is shown in Eq. 2.4.4.

$$V_{GS-M13} \geq V_{GS-M11,12} + V_{DS-M3,4} \tag{2.4.1}$$

$$I_D = \frac{\mu_n\ C_{ox}}{2}\ \frac{\mathrm{W}}{\mathrm{L}}(V_{GS}\text{ - }V_{TH})^2\ (1{+}\lambda V_{DS}) \tag{2.4.2}$$

where λ is the channel length modulation.

$$V_{DS} \leq V_{GS} + V_{TH} \tag{2.4.3}$$

$$I_D = \mu_n\ C_{ox}\ \frac{\mathrm{W}}{\mathrm{L}}\ ((V_{GS}\text{ - }V_{TH})V_{DS}\text{ - }\frac{{V_{DS}}^2}{2}) \tag{2.4.4}$$

Eqs. 2.4.4 and 2.4.2 show the change of V_{GS} by simply changing its operation region. Since the current stays the same, V_{GS} increases significantly. The mirror transistors, still in saturation, then transform this voltage increase into a current boost.

Simulations have shown that it is advantageous to use transistors with a somewhat smaller V_{TH} for M_{11} and M_{12} compared to M_{13}. This makes it easier to ensure that M_3 and M_4 are in saturation if no v_{id} is applied.

In order to decrease the power consumption, simple scaling of the bias current and the transistor size of M_{13} can be used to reduce the steady state current flow in this branch.

2.4.3 Variation

Fig. 2.10 shows another possibility to complete the output class AB qualification. It is the same configuration as as shown in Fig. 2.9 except that M_{11} has been moved to the last diode in the negative signal path. This is an advantage with regard to power consumption because the increase in current is given by M_8 instead of M_7. Looking at other requirements, such as the offset, this configuration becomes quite a problem. In order to avoid creating a new branch, the voltage at the gate is taken from the diode connected M_{10}. With proper scaling this can be done, but the difference in the operating

points of the cascode transistors M_{11} and M_{12} at steady state is very difficult to overcome. This offset is due to different mobilities and uneven behavior over process, temperature and mismatch.

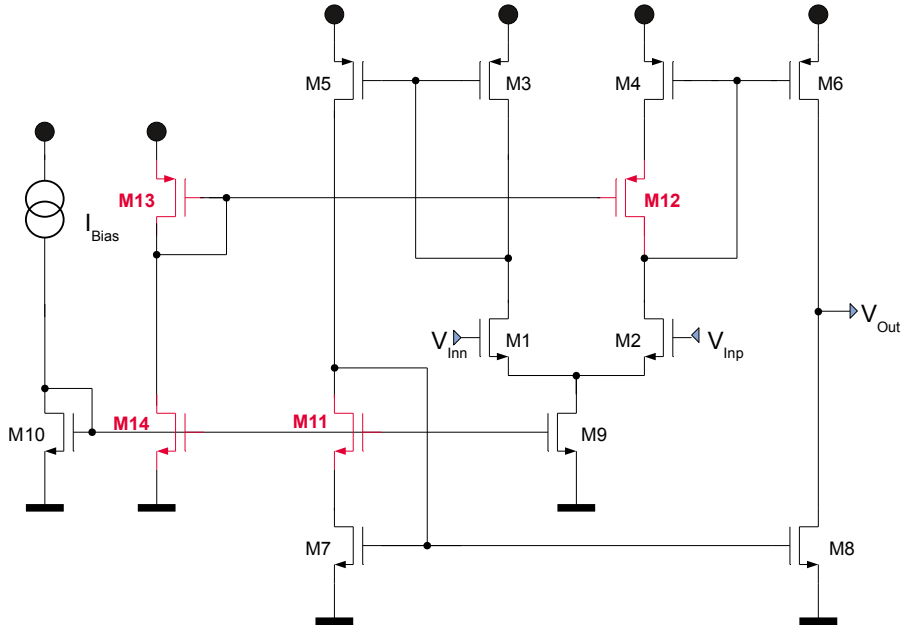


Figure 2.10: Class AB Current Mirror OTA High Swing Cascode Variation

2.4.4 Results

Fig. 2.11 shows the simulation results of the settling time as well as energy used during this time period for the regular current mirror OTA (CM N-OTA) as well as the implementation with the adaptive biased high swing cascode (A-Bias HSC). The first thing to notice is that the A-Bias HSC seems to have a high phase margin. This yields a constant settling behavior over the temperature without any sudden drops occurring. Even though the settling time is slightly longer compared to the time needed by the CM N-OTA, this adaptive biasing variation shows great improvement regarding energy consumption in the given time period. Once again, only the rise time is taken into account here due to the aforementioned reasons. It can also be seen that at low temperatures the rise time is a little bit longer due to a higher V_{TH}. As the temperature rises, the $V_{GS-M3,4}$ increases due to a decrease in V_{TH}. Since this is the same V_{GS} for M_5 and M_6 the output current will change proportionally. At high temperatures the mobility effects control the behavior of the OTA. The mobility decreases with higher temperatures eventually increasing the settling time again.

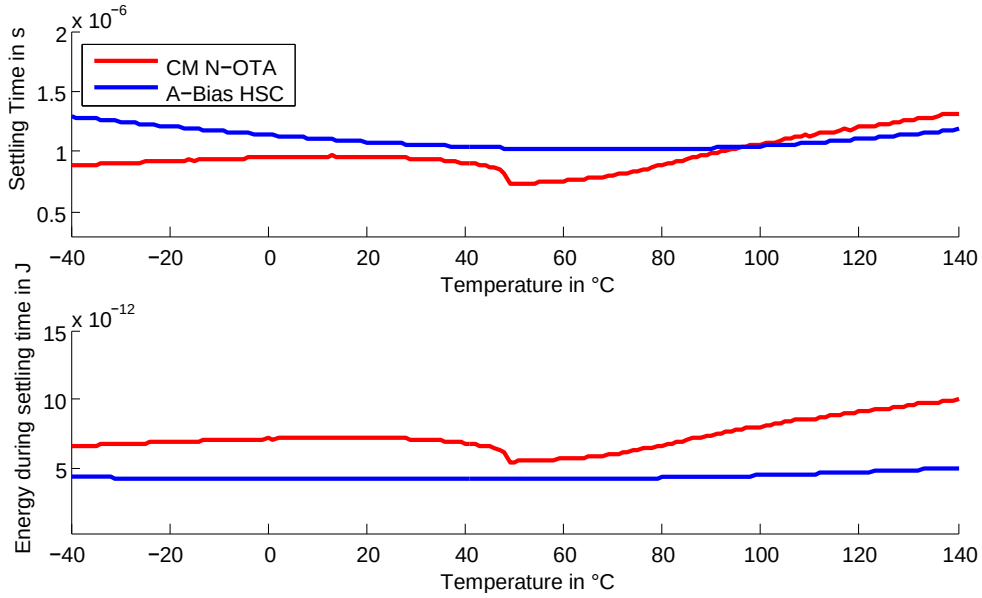


Figure 2.11: Current Mirror OTA vs. Adaptively Biased OTA HSC 1

The standard deviation of the final output value over process and mismatch variations of the adaptive biased current mirror OTA with a high swing cascode was found to be 1 mV.

Next the sum of the rise and fall times of the regular current gain OTA will be compared to the OTAs in Figs. 2.9 and 2.10. The modified version of the OTA with a high swing cascode uses less current in the far left branch of the OTA because the adaptive biasing is implemented to increase the current through M_8, instead of M_5 of the original version. Therefore, in order to get a useful comparison, the fall time has to be included, because when a negative input step is applied, the current will be mirrored through the far left branch, affecting the overall power consumption. These results are shown in Fig. 2.12.

It is obvious that the modified high swing cascode OTA (A-Bias HSC2) uses the least energy while settling just as quickly. This difference is mainly achieved during the negative input step as the regular high swing cascode OTA (A-Bias HSC1) has an extra branch carrying the output current which is quite large. Even though the total time of A-Bias HSC1 is higher than CM N-OTA, the energy used to do so is substantially less. Both adaptive biased OTAs show quite an improvement regarding energy conservation. However, as mentioned, the huge drawback of A-Bias HSC2 is its offset at 2 mV.

Tab. 2.5 summarizes the quiescent currents needed measured at room temperature. The difference in the quiescent currents between the two high swing cascode implementations is simply that the modified version multiplies the $\frac{I_{Bias}}{2}$ by a factor of 3 at a later stage compared to the original. A-Bias HSC1 needs $\frac{I_{Bias}}{2}$ through M_3 and M_4 each. Given

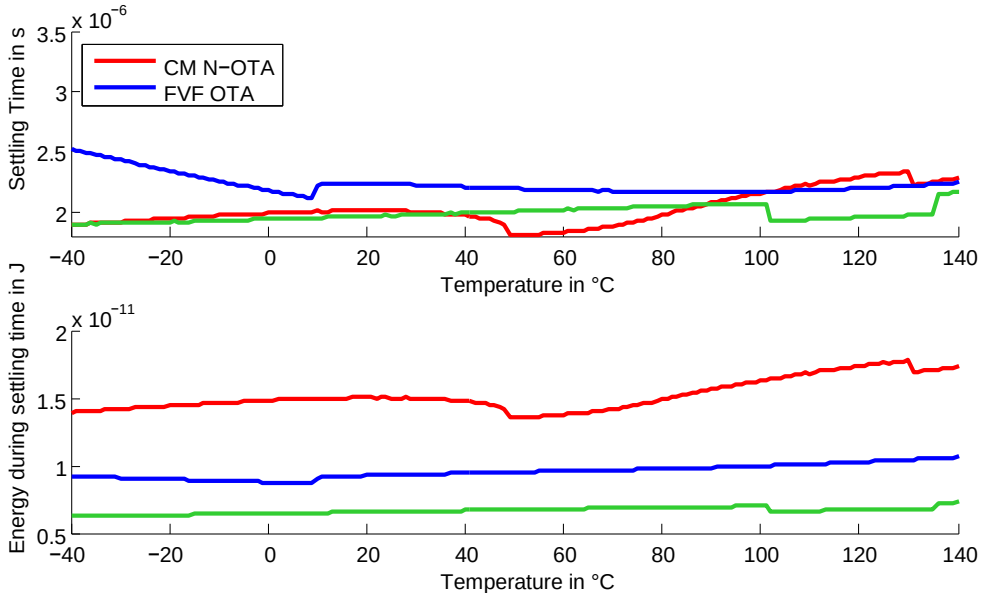


Figure 2.12: Current Mirror OTA vs. Adaptively Biased OTA HSC 2

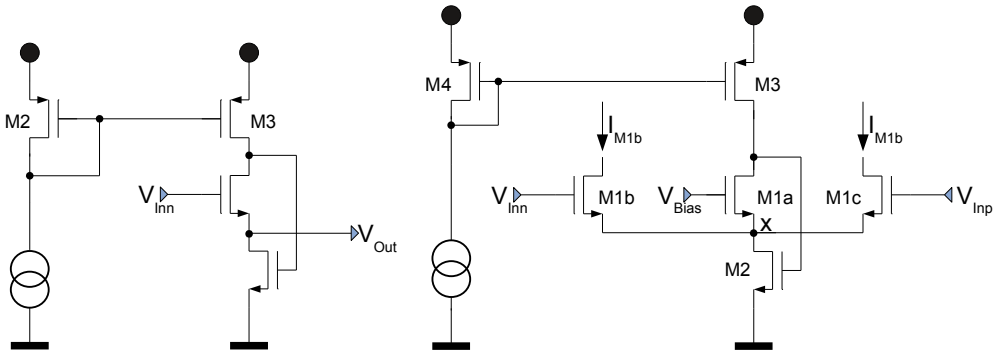
that the current mirrors are scaled M_5 and M_6 then each has $\frac{3I_{Bias}}{2}$, each yielding a total of roughly $4I_{Bias}$. This does not take the branch generating the gate voltage for M_{11} and M_{12} into account because it is a fraction of I_{Bias} and therefore neglected for this quick approximation. Doing the same calculation yields a total of $3I_{Bias}$ for A-Bias HSC2. These calculations are good reflections of the obtained results in Tab. 2.5.

Input Stage	$I_{Out-Min}$ in μA	$I_{Out-Max}$ in μA	$I_{Vdd-Min}$ in μA	$I_{Vdd-Max}$ in μA
A-Bias HSC1	.948	3.59	2.65	4.35
A-Bias HSC2	1.02	4.42	2.04	5.18
NMOS	2.24	4.66	6.01	6.32

Table 2.5: Quiescent Current Consumption A-Bias HSC1 & A-Bias HSC1 & CM N-OTA

2.5 Flipped Voltage Follower

In order to achieve class AB behavior using the input stage, the flipped voltage follower (FVF) in Fig. 2.13(a) presented in [6] can be used. Adding a differential pair to the FVF (Fig. 2.13(b)) allows for it to be used as a differential to single ended converter capable of changing I_{Out} decisively, given a nonzero v_{id}.



(a) FVF (b) FVFDP

Figure 2.13: Flipped Voltage Follower and FVF Differential Pair

2.5.1 Basics

This circuit was originally designed to shift the input signal by a constant V_{GS}. In order to keep the applied voltage shift constant, the current through M_1 has to be kept constant as well (Fig. 2.13(a)). Using Kirchhoff's Current Law (KCL) at the output node it can be seen that M_2 supplies I_{Out} as well as M_1. Since I_{Out} can change but M_1 needs to be constant, M_2 has to be capable of adapting to the required sum of currents. This is done by connecting the gate of M_2 to the drain of M_3. If a change in I_{Out} occurs, M_1 and therefore M_3 decrease. In normal operating conditions, the current through a transistor is given by Eq. 2.4.2. Given that V_{GS-M3} is held constant by M_4, only V_{DS} can change along with the change in current. This causes a change in V_{GS-M2} and therefore the desired change in supplied current.

Given the above, I_{Out} is now used as the bias current for the differential pair as seen in Fig. 2.13(b). Choosing a proper V_{Bias} however is dependent on the requirements of the circuit. For an NMOS differential input pair, choosing a lower value enables a high SR whereas a higher value limits the maximum power usage. Both can be explained by looking at node x in Fig. 2.13(b). In steady state, this voltage is determined by V_{Bias} - V_{GS}. Setting V_{Bias} at a lower potential results in a low potential at node x and will therefore cause a large V_{GS-M1} if a positive input step is applied. This also explains the higher power consumption at steady state when V_{Inn} is higher than V_{Bias}. Choosing a higher voltage to bias M_{1a} reduces both, the SR as well as the overall power consumption of the circuit.

Special attention has to be given to the current mirrors at the output node. The output transistors have to be in saturation and therefore fulfill Eq. 2.4.2. If an input step is applied, the class AB input stage creates a large V_{GS} at the respective diode connected transistor of the current mirror (M_8 and M_{10} in Fig. 2.16). This V_{GS} is mirrored to

the output transistor and it cannot be larger than the sum of transistor's V_{DS} and V_{TH}. Using a transistor with higher transconductance causes the diode connected transistor to have a lower V_{GS} at the same current.

2.6 FVF OTA

An implementation of a class AB input stage can be seen in Fig. 2.14 [8]. Compared to Fig. 2.16 this architecture uses one FVF for the positive and one for the negative signal path. Therefore, its ICMR is only capable of reaching the upper supply voltage.

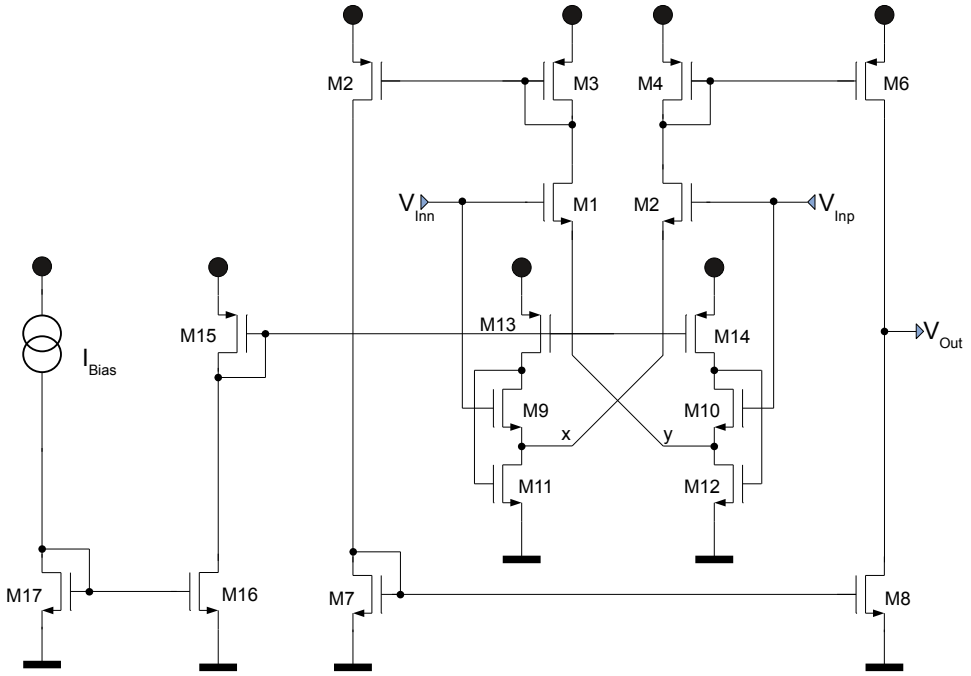


Figure 2.14: FVF OTA

2.6.1 Basics

Instead of making use of a fixed V_{Bias} like the original FVF, this circuit uses the differential voltages as cross coupled supply bias voltages. The voltage at the non-inverting input controls the source of the input transistor of the inverting input and vice versa. If a positive input step is applied, I_{M2} increases due to an increase in V_{GS} at this transistor (Fig. 2.14). Since the current through M_{10} is held steady its V_{GS} is constant and causes an increase of the potential at node y. So a positive input step increases I_{M2} by raising

the voltage at its gate while at the same time I_{M1} is decreased due to an increase of the potential at its source.

Compared to the circuit in Fig. 2.16, this architecture (or a PMOS input stage) is capable of handling either, a positive and negative input step. Two FVF are used to supply the current to the input stage. This can be a disadvantage because I_{Bias} has to be present in both branches. If an increase in SR is needed, eventually I_{Bias} will have to be increased, consuming more power. Even though a large SR can be obtained it is difficult to choose the dimensions of the transistors to accurately obtain a given settling time. However this being said a rough estimate can be obtained by looking at M_{11} and M_{12}. Either transistor has to at least sink I_{Bias} from the FVF. The maximum current the transistor can handle is given by its dimensions as well as the maximum V_G which is equivalent to V_{DD} minus $V_{DS-M13,14}$. It must be kept in mind, however, that this is only the maximum available current and it can only be used for a short time since the output will adjust accordingly, which causes an increase of the potential at the inverting input. Another aspect of this circuit that needs to be analyzed carefully is the ICMR. It is dependent on the FVF rather than the differential input pair along with the current mirrors. As mentioned, M_9 and M_{10} have to be in saturation in order for the circuit to work properly. The least amount of current through M_{11} and M_{12} is I_{Bias}. Given this current, a proportional voltage depending on the transistor parameters will be set at the gate of M_{11} and M_{12}. Ideally, the maximum of the input potential should not exceed this value by more than $V_{TH-M9,10}$ in order for the FVF input transistor to stay in saturation. The minimum is given by the sum of $V_{GS-M9,10}$ and $V_{DS-M11,12}$.

2.6.2 Implementation

In order to obtain dimensions for the differential pair, the approach from Sec. 2.2.2 was used. Although commonly used in the current mirror OTA, the current mirrors here do not need to be a multiple of their respective diode connected transistors because the increase in current to get a higher SR is done by the input stage. Given that this input stage is capable of generating a high enough current by itself, a multiple mirror transistor would only cause a constant high current at the output even when in steady state, therefore unnecessarily using more power. Furthermore, the current mirrors are implemented with transistors with a higher transconductance in order to avoid a large V_{GS} during the input step. The input transistors of the FVF can have the same dimensions as the differential input pair. It is however crucial that $M_{9,10}$ are in the same operating region at all times. If this is not the case, nodes x and y are subject to change depending on the operating region and the currents of M_1 and M_2 will adjust accordingly. To prevent this from happening, M_{11} and M_{12} have to have a large V_{GS} in order to avoid setting the voltage at the drain of M_{11} and M_{12} too low. Using a transistor with a higher V_{TH} will automatically increase the needed V_{GS} for it to be in saturation. Furthermore the length can be increased to force a larger difference in V_{GS}.

2.6.3 Results

The rise time, along with the energy of the flipped voltage follower (FVF) OTA, is compared to the regular current mirror OTA (CM N-OTA) in Fig. 2.15. At low temperatures, the flipped voltage follower is clearly better, because even though it needs the same amount of energy, the time needed to complete the input step is about half that of the regular OTA. However, as the temperature rises so does the input step time period. The threshold does not affect the current over temperature because the voltage at node X is determined by Eq. 2.6.1. I_{M2} is determined by its gate-source voltage. Given that V_{TH-M2} changes with the temperature as well, this effect is limited.

$$V_X = V_{TH-M9} + V_{DSAT-M11} \tag{2.6.1}$$

The effect forcing an increase in rise time and energy over temperature is the mobility. It is inversely proportional to the temperature and causes a reduction of the current through M_2 as well as the output current.

As the current decreases over temperature the phase margin increases. Given that the pole locations of the OTA are the same, a decrease in current results in a reduction of GBW and therefore phase margin. This results in less peaking and a growth in settling time.

Between 60°C and 61°C the peaking in the input step response decreases to less than 1 mV, causing a drop in settling time as well as energy. The requirement of settling within 1 mV over process and mismatch variations was achieved with less than 0.9 mV for the standard deviation.

The quiescent and active current of the OTA as well as the output currents are shown in Tab. 2.6. It can be seen that the FVF has the largest increase in output current. However, since the bias current of the OTA is modified, the current consumption increases heavily as well, because the large current flows through several branches.

Input Stage	$I_{Out-Min}$	$I_{Out-Max}$	$I_{Vdd-Min}$	$I_{Vdd-Max}$
	in μA	in μA	in μA	in μA
FVF DP	1.44	12.1	7.75	25.7
NMOS	2.24	4.66	6.01	6.32

Table 2.6: Quiescent Current Consumption FVF & CM N-OTA

2.7 FVF Rail-to-Rail

A rail-to-rail FVF can be seen in Fig. 2.16. This design is a little bit of a compromise, as instead of using a fixed V_{Bias}, it is connected to the negative input terminal. When used

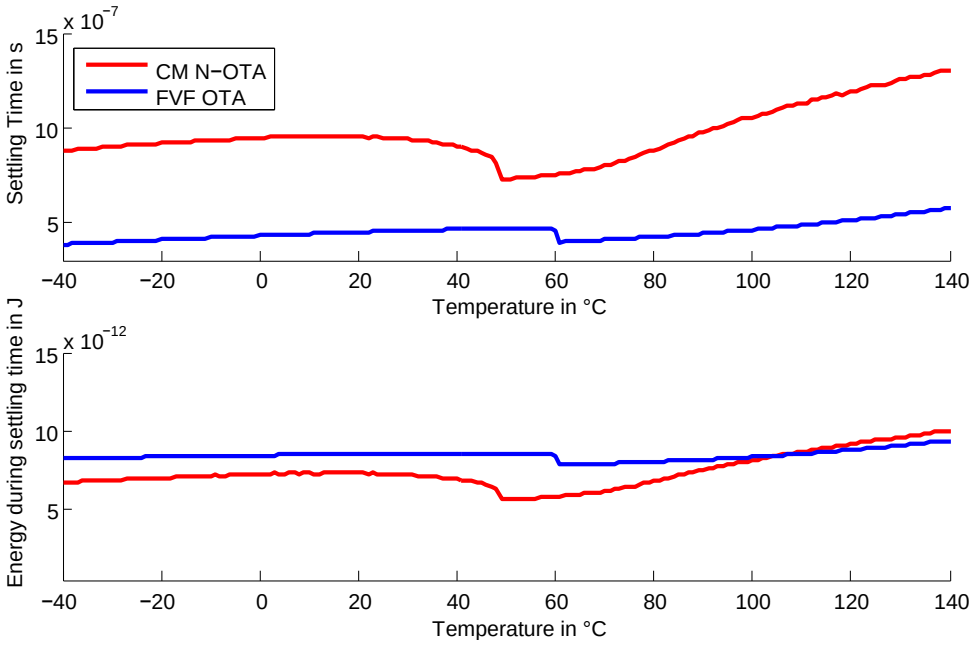


Figure 2.15: Current Mirror OTA vs. FVF OTA

as a buffer, this gives an increased SR if needed, while still reducing power consumption once the signal has settled.

2.7.1 Basics

Setting a fixed V_{Bias} means having to settle for either a smaller SR or more power consumption. Connecting the inverting input in its place gives another option which can be looked at as a compromise. In order to obtain the SR the transient behavior of the circuit is analyzed. Applying a positive input step yields a high SR, as explained in Sec. 2.5.1. However, as the output settles to its final value to follow the input signal, V_{Bias} is raised, and the potential at node x in Fig. 2.13(b) along with it. This only causes a reduction of the SR once the output value is close to the input. However, the overall power consumption is decreased for the same reason.

Although this circuit is a compromise between SR and power consumption it comes with many drawbacks. One is that the NMOS input stage can only support a positive input step. Assuming the circuit is in steady state and a negative input signal is applied, M_{1c} will shut off (Fig. 2.13(b)). This causes the current previously going through M_{1c} to divide evenly between M_{1a} and M_{1b}. An increase of I_{M1a} yields a lower V_{DS-M3}, which in turn decreases I_{D-M2}. This causes less current available to discharge C_{Load}. Due to this a rail-to-rail input stage can be implemented in which the NMOS stage is responsible

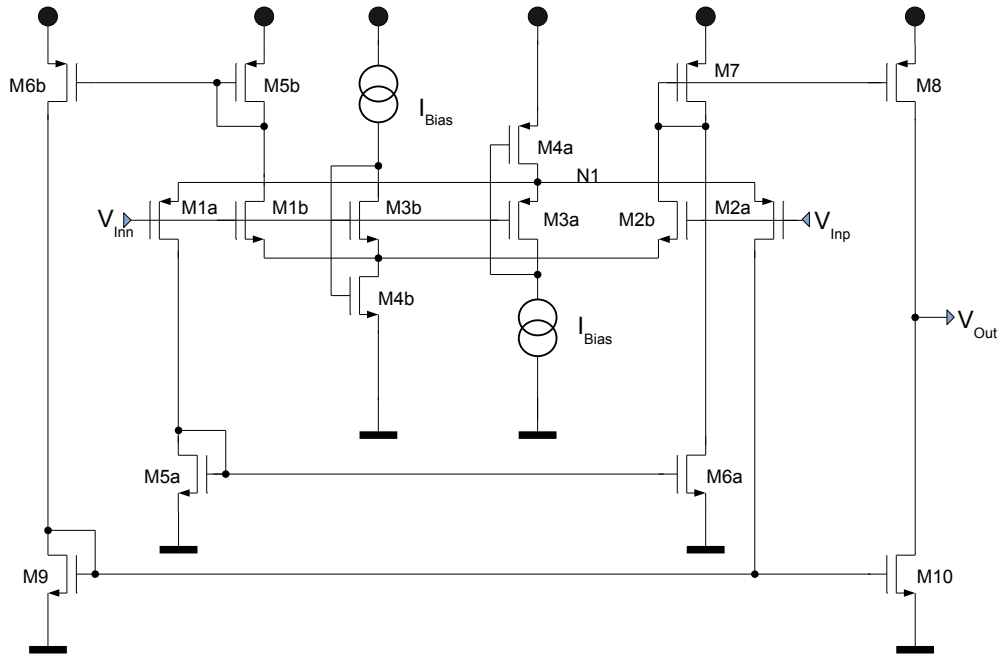


Figure 2.16: Rail-to-Rail FVF

for the positive while the PMOS handles the negative signal steps. Even though the inverting input signal controls the gate of M_{1a}, it is still necessary to have a path to the output as well. Once V_{OUT} is equal to V_{IN}, the negative output path is used to sink the current supplied by the positive output path in order not to change the value on the capacitor. Not having this branch would therefore cause the output signal to be either ground or V_{DD}. This yields many necessary but power consuming branches overall. An advantage of having to use an NMOS as well as a PMOS input stage is that the ICMR is increased, as shown in Eq. 2.7.1-2.7.3.

$$V_{InMax} = V_{DD} - V_{DSAT-MP5b} - V_{TH-MP5b} + V_{TH-MP1,2} \tag{2.7.1}$$

$$V_{InMin} = V_{DSAT-MN5a} + V_{TH-MN5a} - V_{TH-MN1,2} \tag{2.7.2}$$

$$V_{ICMR} = V_{InMax} - V_{InMin} \tag{2.7.3}$$

2.7.2 Implementation

The dimensions of the input differential pairs along with M_{3a} and M_{3b} as well as all the current mirrors have been implemented as mentioned in Sec. 2.2.1. Given that the

circuit is rail-to-rail the PMOS input transistors have been chosen a factor three larger due to the higher mobility of electrons compared to holes (Sec. 2.2.3, see [12] among other). Keeping in mind that this is a class AB input stage, the circuit's dimensions can be implemented two different ways. One is to choose input transistors with a larger V_{TH} in order to cause an overall higher V_{GS}. This helps keep the voltage across V_{GS} of the diode connected M_{5a} and M_{5b} a little bit lower, in turn helping M_8 and M_{10} stay in saturation if a large v_{id} occurs. The current mirrors along the path to the output can be scaled with larger width, decreasing V_{GS} and therefore allowing a higher SR. This, however, comes at the cost of accuracy. The current mirrored from the diode causes a low V_{GS} especially at low currents during steady state. Therefore the saturation voltage will be smaller and more susceptible to changes of V_{TH} due to process variations as well as mismatch. A different way to determine the dimensions is to settle for transistors with a smaller V_{TH} and more transconductance. Using this type of transistor for the input stage causes more current flow given the same applied voltages as well as dimensions. This in turn would cause the diode connected transistors M_{5a} and M_{5b} to increase their V_{GS}. Using the same type of transistor, however, yields a smaller voltage without having to increase the width of the transistor. Therefore, the same approach to determine the dimensions of the current mirror as described in Sec. 2.2.1 can be used. This also enables a better output swing for the circuit. Transistors M_{4a} and M_{4b} have been designed as described in Sec. 2.6.2.

2.7.3 Results

Fig. 2.17 shows the results of the flipped voltage follower rail-to-rail implementation (FVR R2R) compared to the regular current mirror OTA (CM N-OTA). The FVF R2R does need more current but is also quicker to settle. Somewhat surprising is the fact that the settling time actually decreases with temperature. This occurs because of the rail-to-rail input stage. When the input voltage increases, the potential at N1 in Fig. 2.16 is elevated due to the V_{GS} of M_{3a} held constant by the current sink. At low temperatures V_{TH} is higher, therefore eventually forcing M_{4a} into the linear region because its V_{DS} becomes too small. If this happens, the current sink could also be affected because V_{GS-M4a} increases to supply the same current. An increase in V_{GS-M4a} causes less V_{DS} for the current sink, forcing it into the linear region. Overall this yields very little current through M_{1a} as well as M_{3a}, because their conditions are very similar. This current is then mirrored via M_{5a}, M_{6a} to the diode connected M_7 where it is combined with the current from M_{2b}. At high temperatures, V_{TH} decreases causing less of a raise in potential at N1. This difference is enough to keep M_{4a} in saturation at 140°C. As intended, the current sink stays saturated and the current stays steady through M_{3a}. Given only a different V_{DS}, the current through M_{1a} is very similar. Once again it is then added to the current through M_{2a} and mirrored at the output stage, resulting in less settling time.

The overall maximum and minimum total as well as output currents of the FVF R2R

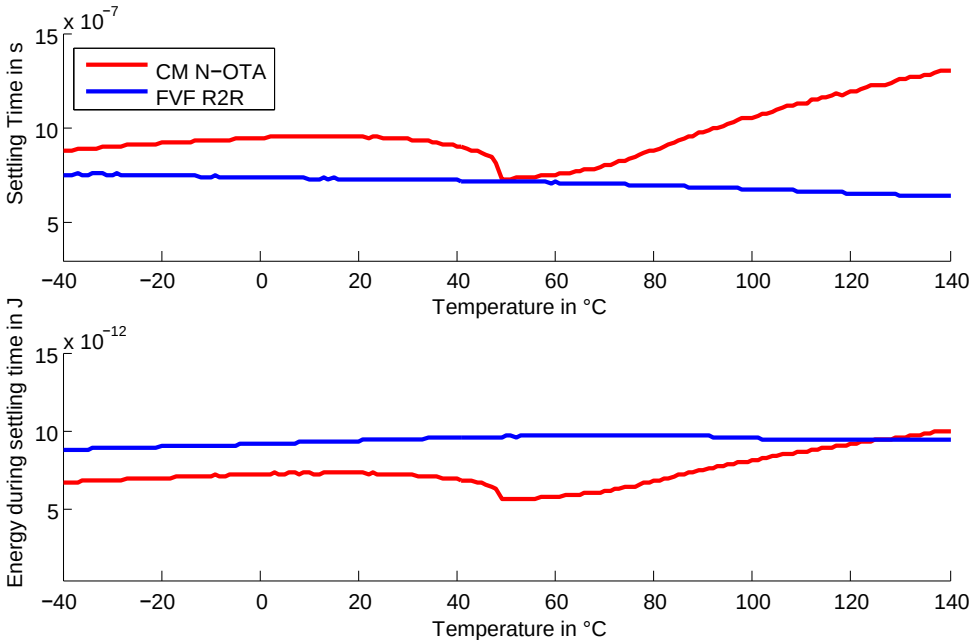


Figure 2.17: Current Mirror OTA vs. FVF OTA R2R

are compared to those of the regular current mirror OTA in Tab. 2.7.

Input Stage	$I_{Out-Min}$ in μA	$I_{Out-Max}$ in μA	$I_{Vdd-Min}$ in μA	$I_{Vdd-Max}$ in μA
FVF R2R	1.37	16.2	4.6	27.2
NMOS	2.24	4.66	6.01	6.32

Table 2.7: Quiescent Current Consumption FVF R2R & CM N-OTA

An increase in the output current given a v_{id} is clearly accomplished. However, the rail-to-rail needs a certain minimum amount of current through all the branches. Even when scaling the current, it will add to the energy consumption. The OTA was implemented with a standard deviation over process and mismatch of 1 mV.

2.8 Adaptive Bias OTA Comparison

A variety of different ways to obtain class AB OTAs has been compared, stretching from a version with very little change, to the original current mirror OTA with the source degeneration or high swing cascode, to more complex implementations including the

FVF. Overall, it can be said that the output current can be heavily increased given a v_{id} with class AB OTAs while saving energy when no v_{id} is applied. A quick summary of the different rise times along with their respective energy consumption is shown in Fig. 2.18.

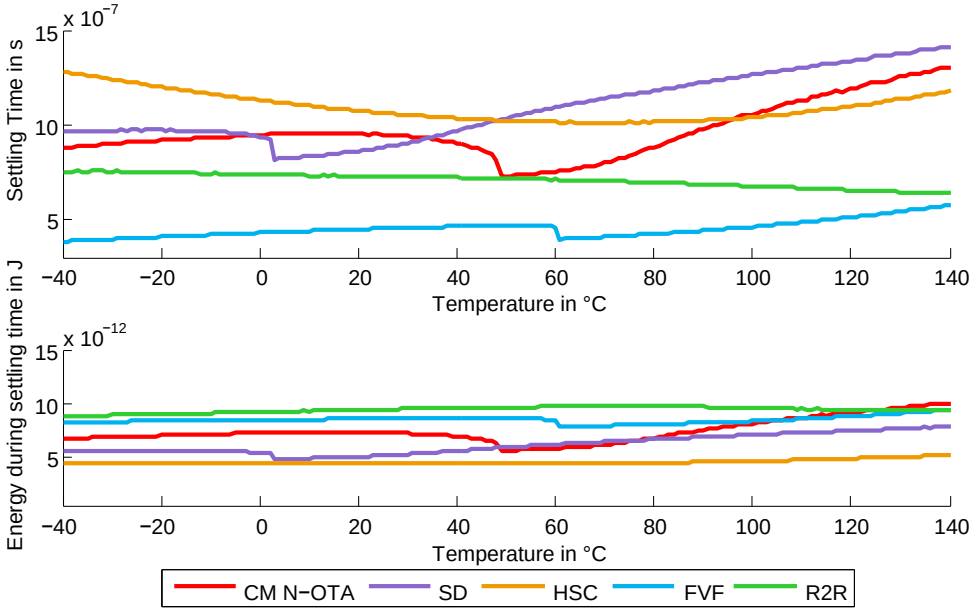


Figure 2.18: Rise Time & Energy Summary

The HSC and FVF implementations probably show the best results. Given that the FVF only needs about half of the time to complete the input step response, its energy would be halved if the response was to be completed at about 1 μs. While the HSC implementation has a limited common mode input voltage, the FVF is more likely to struggle with the offset of the OTA, as the voltages for the diode connected current mirrors should be smaller due to the larger current through the input stage. This results in a larger $\frac{g_m}{I_D}$, which is non-ideal for current mirrors. If a large common mode input voltage is required, the FVF R2R is probably the best choice. Overall, parameter requirements such as area, offset, as well as input common mode voltage, will dictate which of the above listed adaptively biased OTAs is best suited for a given application.

For completeness, figures of merit (FOM) obtained from [7] are shown in Tab. 2.8. FOM_S and FOM_L are defined by Eqs. 2.8.1 and 2.8.2 respectively.

$$FOM_S = \frac{\text{GBW}\cdot C_{Load}}{\text{Power}}\ [(\text{MHz}\cdot\text{pF})/\text{mW}] \tag{2.8.1}$$

$$FOM_L = \frac{\text{SR}\cdot C_{Load}}{\text{Power}}\ [(\text{V}/\mu\text{s}\cdot\text{pF})/\text{mW}] \tag{2.8.2}$$

OTA	FOM_S	FOM_L
CM N-OTA	1127	544
SD	1466	774
HSC	1091	1025
FVF	202	1011
R2R	209	1460

Table 2.8: FOM

The advantage of those FOMs is that they can be easily calculated and applied to all OTAs compared to the approach in this work. However, an OTA can also be easily designed to achieve a large FOM_L: simply by scaling the current mirror M_3 and M_4 and M_5 and M_6 (Fig. 2.3) by a factor of three, the slew rate will triple while the steady state power consumption doubles. While this gives the best-case ratio between lowest power consumption and largest slew rate possible, the efficiency of the OTA while doing so gets lost. Furthermore, it is not defined in those figure of merits if the steady state or dynamic power consumption is to be used. For the work in this thesis, the dynamic power consumption was used, as it shows the worst case, which is when the OTA has a constant nonzero differential input voltage. Another concern in FOMs is the area consumption. The FVF for instance will most likely have a larger layout than a regular OTA. While it is difficult to include the area consumption in an FOM, it would still be more beneficial to use a ratio of slew rate and power consumption while achieving the former, instead of only during steady state.

Chapter 3

Peak Detector

Another circuit block used in the sensor interface is the peak detector. It is the vital link between the differential to single ended amplifier and the input to the ADC as seen in Fig. 1.3. As its name suggests, the peak detector is used to detect the amplitude of the sinusoidal signal obtained from the impedance measurement.

3.1 Objective

For this application the frequency of the sinusoidal signal used can vary from 1 kHz up to 100 kHz. The minimum detectable peak is at 200 mV while the maximum should be as close to V_{DD}, which is 1.5 V, as possible. However, the expected input signals are between 200 mV and 300 mV. The time allowed for the peak detector to find the maximum voltage is less than 10 periods of the input signal. Once the output settles to the peak, this value should be held the over time. Since the ADC used to convert the signal has a resolution of 10 bits, it would be ideal to implement the peak detector with an accuracy of 1 mV. More accuracy is not needed as the ADC will not be able to detect the changes anymore due to its resolution. Overall, the peak detector, along with any biasing circuitry needed, is expected to be as energy efficient as possible.

Table 3.1 summarizes the requirements for the peak detector.

Parameter	**Value**	**Unit**
Frequency Range	1-100	kHz
Voltage Range	0.2-1.5	V
Detection Time	10τ	s
Offset	1	mV
Power Consumption	<10	μW

Table 3.1: Peak Detector Requirements

The possible output characteristics of the desired peak detector are shown in Fig. 3.1.

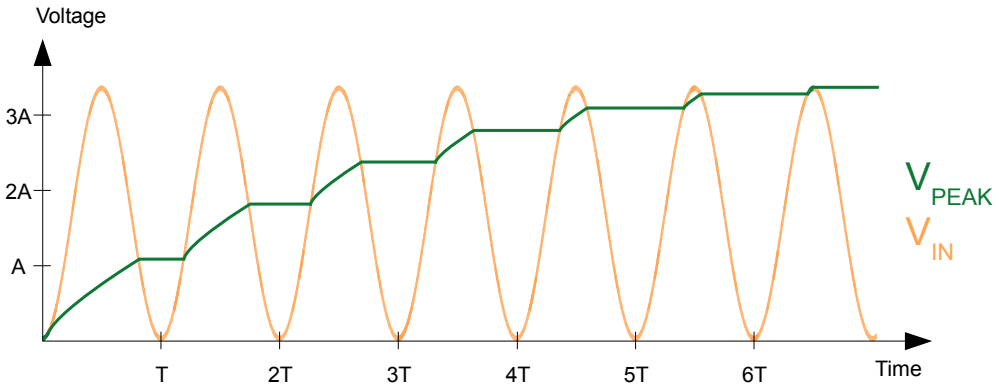


Figure 3.1: Peak Detector Output Characteristics

3.2 Simple Peak Detector

A very common implementation of a peak detector can be seen in Fig. 3.2[5]. A comparator is used to determine the greater between V_{In} and V_{Max}. It controls the gate of M_1 to allow current flow to charge C_{Peak} as well as turns off M_1 when V_{Max} equals V_{In}. M_2 is used to reset the peak detector.

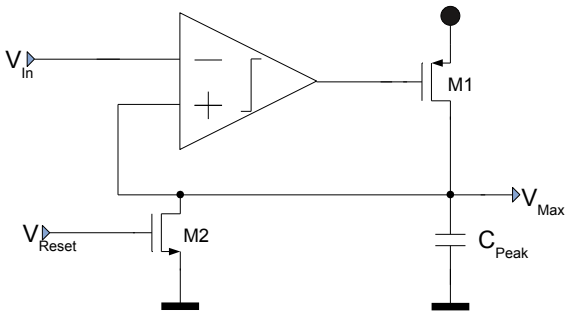


Figure 3.2: Simple Peak Detector Schematic

M_1 can be implemented as either an NMOS or PMOS transistor. When an NMOS transistor is used, the inverting and non inverting terminal of the comparator must first of all be exchanged. Further, the transistor will then be used in a common drain configuration. The output resistance can then be simplified to the reciprocal of the sum of g_m and g_{mb}. Using a PMOS transistor is equivalent to a common source stage with an output resistance of r_{ds}. Having a high output resistance of the overall circuit causes a higher gain resulting in more accuracy. The trade-off, however, is a lower pole frequency at this node limiting the circuit to the use at lower frequencies only. However, using a PMOS transistor also increases the output voltage swing. The current through the

transistor is determined by its gate-source voltage. Given that the source is constant at V_{DD}, the transistor will eventually function in the linear region, because V_{GS} exceeds the sum of V_{TH} and V_{DS} as the potential at the drain increases, until, if given enough time, it eventually approaches the source potential. Using the NMOS transistor, the source potential limits the maximum output voltage. As the output increases, V_{GS} decreases until it is less than V_{TH} turning off the transistor. The maximum output voltage is then described by Eq. 3.2.1. This anticipates that the transistor is in saturation, because just before it cuts off, Eq. 2.3.2 is fulfilled. Increasing the potential at the source can also be seen as an advantage, however. When V_{In} equals V_{Peak}, the output of the comparator is around $\frac{V_{DD}}{2}$. This potential is already large enough to either turn on the transistor or at least increase leakage current. In either case, this is unwanted behavior. Using the NMOS transistor ensures that even though the comparator does not settle its output to either low or high, the current through M_1 does not increase, due to a small V_{GS} mainly caused by a higher potential at the source. This, however, works better for larger values for V_{Peak}. For this application, the PMOS is chosen due to the larger output signal swing as well as the larger output resistance.

$$V_{OutMax} = V_{DD} \text{ - } V_{TH-M1} \text{ - } V_{DS-M1} \tag{3.2.1}$$

Having decided on a transistor type, choosing the dimensions, is another trade-off in itself. While a smaller transistor is advantageous with regards to charge injection when the transistor is turned off, a larger channel length increases the output resistance (g_{ds}) and has better performance once the transistor is turned off. Ideally, once the transistor is turned off, no more charge is released. In reality, however, the charge stored in the channel itself is approximated to be equally distributed to the node at the source and drain of the transistor [5]. This charge is proportional to the area of the transistor and can cause a costly difference in V_{Peak}. Furthermore, a smaller transistor has a small gate-source capacitance (C_{GS}), which is the load capacitance of the comparator. This capacitance is ideally small in order to be charged and discharged fast without having to use a lot of current. On the other hand, the length of a transistor is proportional to its output resistance. Having a large output resistance decreases the leakage current when the transistor is off, influencing the output voltage of the detector less than a shorter transistor would. In the end, a transistor with twice the minimum channel length is implemented for M_1. This substantially increases the transistor's g_{ds} while not increasing C_{GS} too much. The bulk of the PMOS switch is connected to V_{DD} instead of the source potential. This yields a larger V_{TH}, which can only be advantageous. When V_{Peak} has been charged to the maximum of the input signal, the comparator will approach $\frac{V_{DD}}{2}$ as V_{In} reaches another peak. This can already be enough to turn on the switch and falsely charge C_{Peak} further. Increasing V_{TH} results in the comparator having to swing its output further in order to start current flow through M_1, giving it more room for error.

The discharge transistor M_2 is, similarly to M_1, used as a switch. It is only needed to reset the circuit and should otherwise ideally not have any effect on the circuit. Therefore, the transistor with the least amount of leakage is chosen. Furthermore, to strengthen this feature, a longer channel is implemented. The width of the transistor is also three to four times the minimum width in order to ensure that the transistor is capable of discharging the capacitance independent of whether M_1 is on or off.

Another parameter that can be chosen is the size of the capacitor C_{Peak}. While a large capacitor contributes to the accuracy of the peak detector, it also costs a lot of valuable area. Eq. 3.2.2 shows the relation between charge, capacitance and voltage. The voltage across the capacitor is affected less if a large capacitance is used given the same charge. This is an important aspect when V_{Peak} is approaching the value of V_{In}. As the comparator is not ideal, it needs some time to increase the voltage at the gate of M_1 once the voltages are the same. During this time, current is still flowing thereby increasing V_{Peak}, causing an error. For the reasons mentioned above this error can be minimized by using a larger capacitor. Similarly, given leakage current, the output is affected more when using a small capacitor. In order to not use too much space, a capacitor of 4 pF is used for the peak detectors in the following sections.

$$\mathrm{V} = \frac{\mathrm{Q}}{\mathrm{C}} \tag{3.2.2}$$

Another approach to limit the current through M_1 is to use a current mirror which controls its maximum current as seen in Fig. 3.3. In this circuit, I_{Bias} is mirrored to M_{10} via M_8. Given that M_1 operates most of the time in the linear region, it will have a large V_{GS} in order to increase its current. This results in a small V_{DS-M10} eventually forcing it to operate in the linear region as well. Once this occurs, the maximum output current is limited to less than I_{Bias} according to Eq. 2.4.4. I_{Bias} can be approximated using Eq. 3.2.2. The maximum voltage is V_{DD} for the detector, and charge can be substituted by the current multiplied by time. The least time is given by 10τ of 100 kHz, where τ is the period, in which the detector needs to be able to charge to the maximum voltage.

Having discussed the basics of a general peak detector, a leakage compensated, a clocked-signal as well as a differentiator-based peak detector, is presented in the following sections.

3.3 Low Leakage Peak Detector

The peak detector explained in Sec. 3.2 is used with some additions, to improve leakage behavior, resulting the circuit shown in Fig. 3.3. As in the the original, the comparator, as well as the charging transistor M_1, can be seen. The current mirror consisting of M_8 and M_{11} simply limits the current through M_1 by setting a maximum of I_{Bias}, as previously described. A leakage compensation network is implemented as well as a low

leakage discharge solution. The output of the buffer generates V_{Peak_Guard}, which can then be used as the input signal by the ADC so that V_{Peak} is not strained any further.

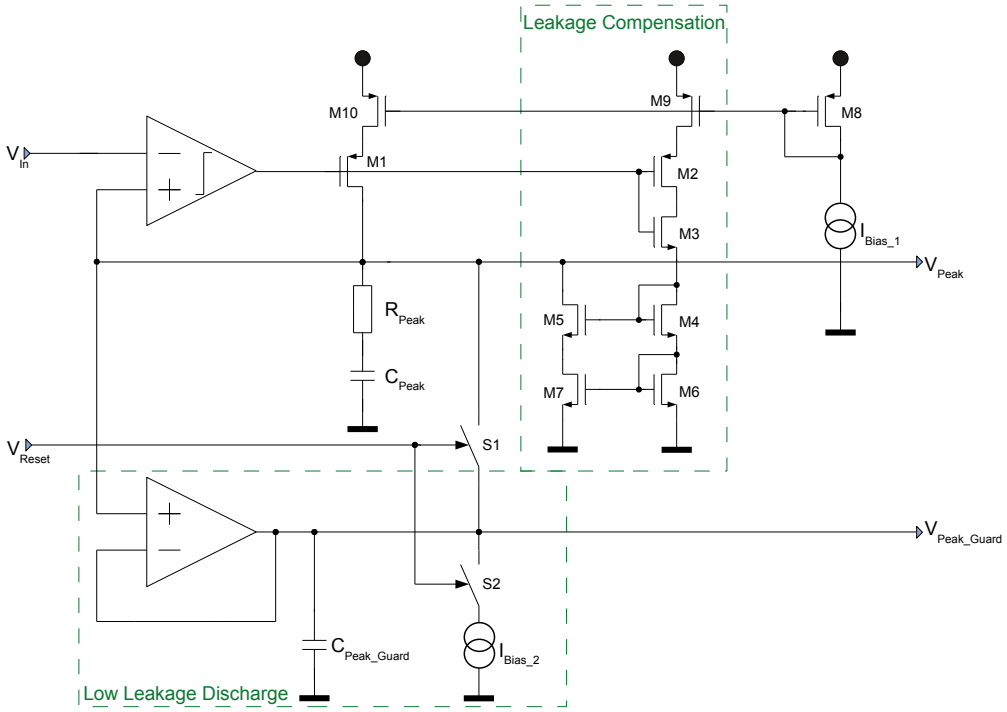


Figure 3.3: Low Leakage Peak Detector Schematic

3.3.1 Implementation

The comparator is the key factor in determining the accuracy of the final V_{Peak}. Given the frequency specification for the peak detector, the comparator's dominant pole needs to be higher than 100 kHz in order to maintain the same gain throughout the bandwidth in use. According to [2], an open loop comparator should be used due to the lack of a clock signal. Given these requirements, a clamped push-pull output comparator was chosen. This comparator has the same architecture as a current mirror OTA. It furthermore consists of a favorable push-pull output stage as well as current scaling to increase the output current. The comparator was implemented with a PMOS input stage due to the input signal requirements of at least 200mV. This causes a less accurate V_{Peak}, because the lower input voltage determines the potential at the node connecting the sources of the input pair. An NMOS input stage has the advantage that the higher potential, which eventually is V_{Peak}, determines this potential. If the OTA with the NMOS input stage from Fig. 2.3 would have been used, once the input signal amplitude has been detected,

I_{M2} would eventually equal I_{Bias} as V_{Inp} is greater than V_{Inn}. Given that M_1 is off, the potential at node N1 will be determined by V_{GS-M2}, causing it to only adjust when V_{Peak} changes. The same theory applies for the PMOS input stage. This time however, the potential is determined by the lower voltage, which in most cases is V_{In}. Given a sinusoidal input signal, this signal will be reflected on this node and affect V_{Peak} through capacitive coupling effects.

Having decided on the topology for the comparator, its load capacitance was approximated to be less than 1 pF. Given this load capacitance the comparator was implemented with a gain of 40 dB as well as a bandwidth of 100 kHz at room temperature. The gain of the comparator is supported by the gain of the output stage of the peak detector, which is given in Eq. 3.3.1.

$$A_v = g_{m,M1} \cdot R_{Out} \tag{3.3.1}$$

where

$$R_{Out} = g_{ds,M1} \parallel R_{Peak} + \frac{1}{\mathrm{j}\omega \mathrm{C}} \tag{3.3.2}$$

R_{Peak} is used to offer more output resistance at high frequencies when the capacitor behaves as if it is short circuited. As can be seen by the equations above, it is beneficial for the gain if the transistor configured in a common source circuit has a large g_m. This can be achieved by increasing the width of the transistor, however, as mentioned previously, this increases the load capacitance of the comparator and eventually slows it down. Therefore, the width was chosen to be twice the minimum of the process.

The leakage compensation network consists of two branches. The first is used to sense the leakage current, while the other draws this current out of C_{Peak}. M_9 mirrors the current of M_8, just as M_{10} does. Similarly, M_2 has been implemented in the same way as M_1; namely, their gate, source and bulk voltages are the same. This results in the same current being drawn through the two transistors. M_6 is used to mirror the current generated by M_2 and sets an appropriate V_{GS} for M_7, which is then responsible for drawing this current out of C_{Peak}. Transistors M_4 and M_5 are used as cascode for the current mirror. This causes the original current mirror to be more accurate, due to the same V_{DS}, as well as raise the potential at the gate of M_4 proportional to its current. Finally, M_3 is implemented as a switch. Given a low output voltage by the comparator, M_1 can charge C_{Peak} because at a low potential the NMOS transistor M_3 will be turned off. Once the comparator output switches to high, the PMOS switches M_1 and M_2 will be off and therefore only have leakage current. M_3 is on and the leakage current can be mirrored by M_6 and M_7 to compensate the I_{M1}. In the case that V_{In} is reaching another maximum and V_{Peak} is already close to this value, the comparator output will be around $\frac{V_{DD}}{2}$. This causes current to flow through M_1 and charge C_{Peak} further. As this current will be very small due to a smaller V_{GS}, the compensation network will copy

this current. This may not be ideal, as V_{Peak} may not be at the maximum of the input signal yet. In order to prevent this, the cascode of the current mirror assists. Instead of using the gate of M_3 to turn the transistor off, at slightly larger currents the cascode current mirror raises its V_{GS} eventually elevating the potential of the source of M_3 until it is turned off. This sets a limit to the maximum current that can be compensated for by the network. Since this compensation is dependent on the equivalence of M_1 and M_2 only a PMOS implementation is possible because if an NMOS would be used instead, the potentials of their sources would be different. While the source of M_1 would have the potential of V_{Peak}, the potential of the source of M_2 would be mainly determined by the cascoded current mirror. Therefore the respective currents would not be equivalent and a compensation is not possible anymore.

The second improvement made to the circuit is the reduction of the leakage current through the discharge switch. While the peak detector is in normal operation, the discharge NMOS transistor will be off. Even in this state, the transistor has a finite resistance. Given a large enough voltage drop across the transistor, a certain amount of leakage current will drain the capacitor and reduce V_{Peak}. To minimize this leakage, a buffer has to be implemented in order to generate V_{Peak_Guard}. The source of the switch is then connected to this voltage instead of the current sink. A second switch is needed now to connect V_{Peak_Guard} to the current sink. The two switches are both controlled by V_{Reset}. This enables the reset function similarly as before, with the exception that when V_{Reset} is low, the leakage across S_1 is minimized while the leakage across S_2 is compensated by the buffer. Furthermore, V_{Peak_Guard} can be taken as input signal to the ADC, as it is less sensitive than V_{Peak}. Attention has to be given to the discharge current I_{Bias2}, as it must be large enough to quickly discharge V_{Peak} as well as V_{Peak_Guard} since they are in parallel when V_{Reset} is activated. Given that the functionality of the peak detector was of highest priority, a regular current mirror OTA was chosen as the buffer used to create V_{Peak_Guard}. As mentioned in Chap.2, an AC analysis is not suitable for an adaptively biased OTA, therefore stability cannot be confirmed. I_{Bias} for the buffer has been reduced and a load capacitor, C_{Peak_Guard}, has been implemented. Those two changes cause the OTA to move its dominant pole to lower frequencies, as well as reduce the GBW, resulting in a stable buffer. The reduction in I_{Bias} is possible here because once V_{Peak} has reached the maximum V_{In} it will not change quickly. Therefore, there is no need for the buffer to be able to quickly adapt to changes. However, this is an ideal example for the use of an adaptively biased OTA, as it would be capable of following V_{Peak} quickly while still reducing current consumption once the final peak value is obtained.

3.3.2 Results

The implemented peak detector in Fig. 3.3, including all biasing circuitry, uses less than $6\,\mu$W at an area of less than $5400\,\mu m^2$. Its layout, presented in Sec. 3.3.3, has been

extracted to obtain the simulation results presented in this section. The test signal used as input is the positive half wave of a sinusoidal signal centered at 200 mV. This is the same signal as would be available on the sensor interface. The top graph of Fig. 3.4 shows the output of the low leakage peak detector (LLPD) given a 1 kHz sinusoidal input signal at different amplitudes at three different temperatures compared to the ideal output voltage. The bottom graph shows the amplitude of the input signal subtracted from the measured output signal.

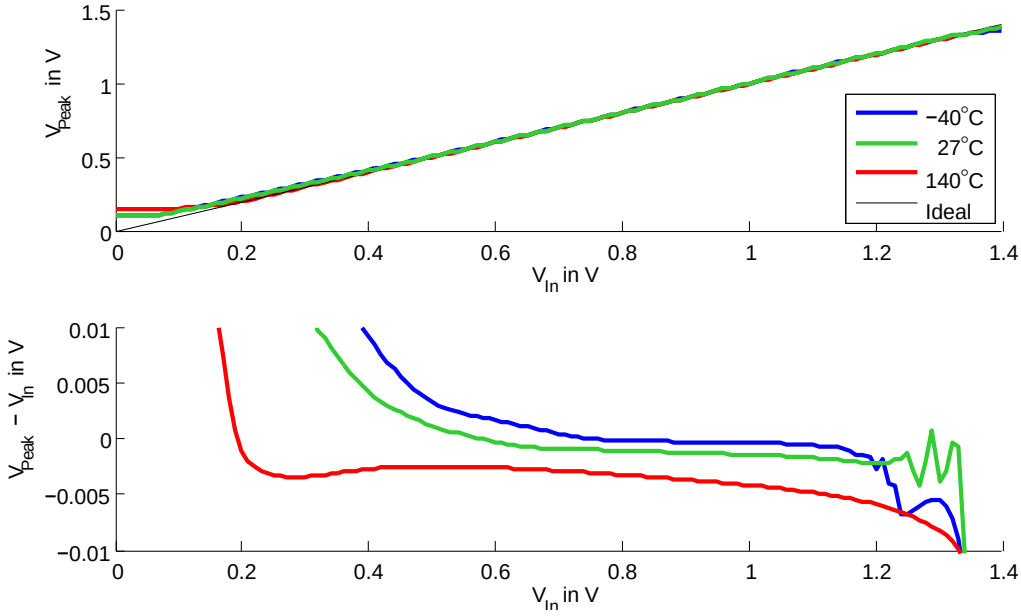


Figure 3.4: LLPD: Amplitude Sweep at 1 kHz Sinusoidal Input Signal

At a temperature of -40 °C the peak detector has a greater offset at lower input values. This is caused by leakage current into C_{Peak} from the discharge switch. Even though the discharge has been improved and therefore its effect has been minimized, it is still noticeable over time at very low frequencies. As the input value increases, this effect decreases due to the leakage compensation circuit. Since V_{Peak} is also equal to the sum of V_{DS-M5} and V_{DS-M7}, it causes a slight increase in current there. However, this is a positive effect, as the peak detector is capable of charging C_{Peak} but not discharging it. Since it is impossible to keep the peak value perfectly steady, it is advantageous to slightly decrease it as it will be increased by the next peak of the input signal. Overall, once the leakage of the switch is compensated for, the circuit shows very linear behavior with little offset until its maximum input of just below 1.2 V. At this point the input common mode range of the PMOS input stage of the comparator limits the output range of the peak detector. A very similar behavior is observed at room temperature. The leakage current has only slightly increased and the curve is shifted to the left. At 140 °C,

the leakage current through M_1 is dominant, therefore the leakage through the discharge switch becomes negligible. The compensation network draws any excess current out of C_{Peak} to keep the maximum value almost steady. Due to this charging and discharging process a larger offset occurs, but the range of linearity is greatly increased. Finally, the output range is also increased, mainly due to the decrease in threshold of the input stage transistors of the comparator.

Much more uniform behavior of V_{Peak} can be observed in Fig. 3.5 where the corresponding output voltage of an amplitude sweep is shown at 10 kHz.

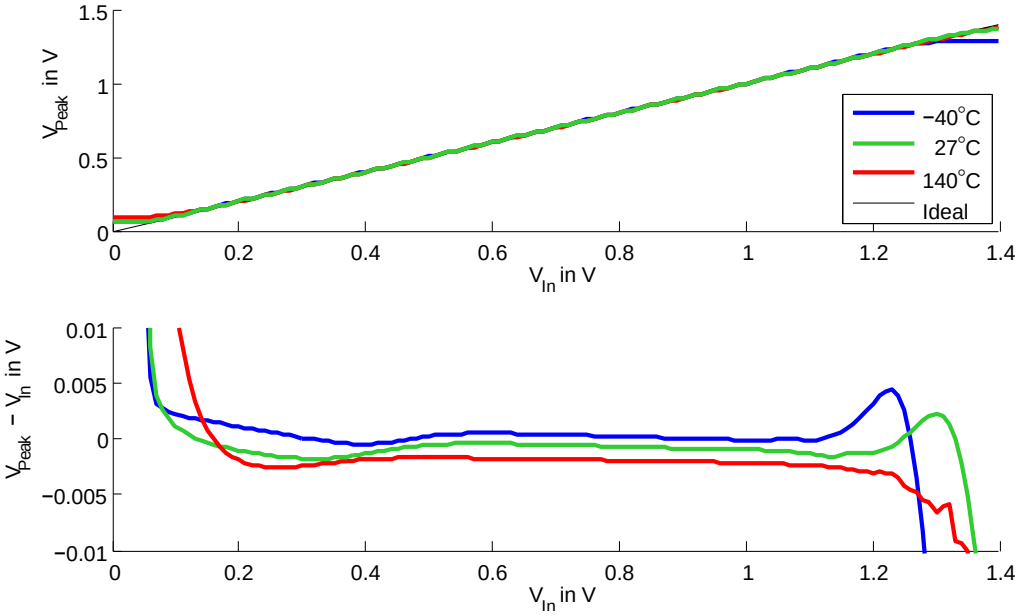


Figure 3.5: LLPD: Amplitude Sweep at 10 kHz Sinusoidal Input Signal

At a temperature of −40 °C, an offset between V_{Peak} and the maximum of V_{In} of 1 mV is achieved at 200 mV. It then decreases to less than −0.5 mV, until it finally rises to over 1 mV again at an input voltage of 1.17 V. The low temperature curve already shows a great improvement of the peak detection circuit compared to the 1 kHz graph. This was expected, as it is due to the leakage of the PMOS transistor in the discharge transmission gate. At 10 kHz the time period has become short enough for the leakage current to have no effect on the overall circuit performance. One effect that is still visible, however, is the gain of the comparator. At lower input voltages the gain is clearly less than at higher, causing a larger deviation from the ideal output voltage. At low input voltages the potential at $N\,1$ in Fig. A.1 drops, as it is controlled by the gate-source voltages of the differential input pair, causing an increase in V_{DS-M9}. As seen in Eq. 2.4.2, this results in an increase in I_{Bias}, changing the operating point of the OTA. Even though g_m of the input stage is increased, r_{ds} of both output stage transistors is decreased. The

effect of the current of a transistor on its output resistance can be seen in Eq. 3.3.3, obtained from [3].

$$r_{ds} \approx \frac{1}{\lambda I_D} \tag{3.3.3}$$

Since the changes in transconductance and output resistance are not equivalent a drop in gain at lower common mode input voltages can be observed. The output voltage at 27 °C shows a similar result, with a minor shift towards the negative offset as leakage is starting to slightly affect the circuit. At 140 °C, leakage once again dominates, and the compensation network is used to cancel this behavior. This is done by successfully obtaining an almost linear function in the range of 200 mV to 1.24 V. Once again, this comes at the cost of an increased offset between the ideal and the measured peak voltage of 2 mV, due to the charging and discharging process.

Fig. 3.6 shows the results peak detector given a 100 kHz input signal with varying amplitude. It consists of all of the aforementioned effects as well as a new one: at an input voltage of about 500 mV slight peaks are observed. Given a certain input voltage at this frequency, the current to charge C_{Peak} is too little to achieve a high voltage across the capacitor. Therefore, more than one period is needed to do so.

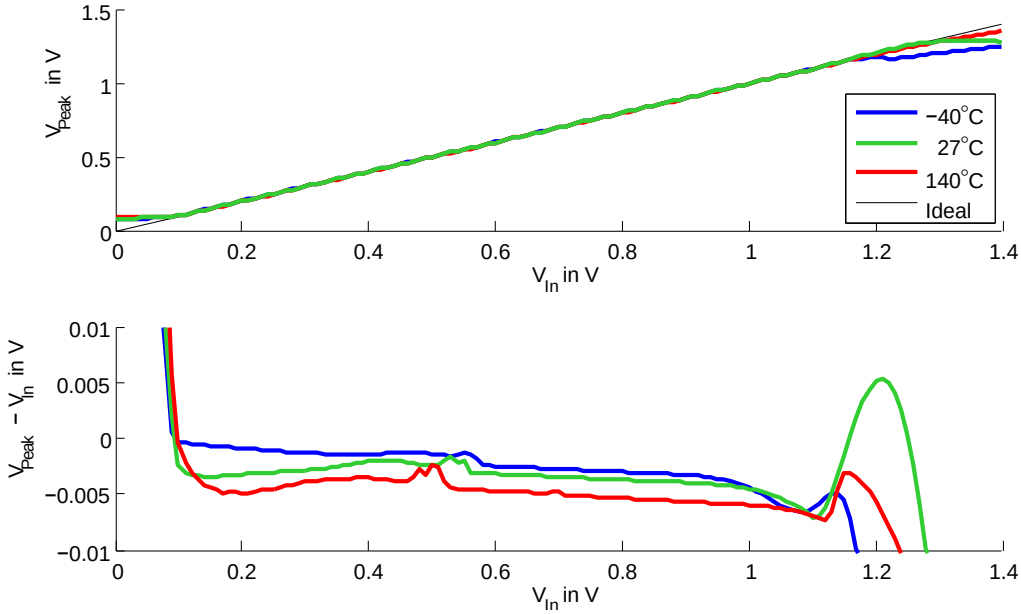


Figure 3.6: LLPD: Amplitude Sweep at 100 kHz Sinusoidal Input Signal

The curve representing the output peak at −40 °C shows the effect of the leakage of the PMOS transistor in the discharge switch at low input voltages again. As the output voltage increases, unevenness in the curve occurs at 550 mV. This is due to the fact

that above this voltage two periods are needed to charge C_{Peak} to the maximum input voltage. Furthermore, V_{Peak} can overshoot due to stability problems. In order to reduce this effect, the peak detector has been implemented with config bits to increase the bias currents. Enlarging I_{Bias1} results in an decrease in r_{ds-M1}. This causes less overall gain for the peak detector which results in a less accurate output voltage as well as a higher pole frequency at the output node when charging. A higher pole frequency yields more stability, which is desired here. The unevenness in the output curve is caused by the compensation network. As previously described, the switch M_3 will cut off when the charging current is larger. However, if one peak of the input signal is almost enough to find the maximum, the detector will charge C_{Peak} close to this value. During the second period, as V_{Peak} is already close to its desired value, the comparator will not fully turn on M_1, resulting in less charging current. If this current is not large enough, M_3 will not turn off, and the compensation network copies this current, resulting in an error in the final output value. This can be observed in Fig. 3.6, as around 450 mV the accuracy increases, due to more gain of the comparator, but then the curves of all three temperatures have a small drop before two periods are needed to charge C_{Peak}. At this point the charging current during the second period is large enough to shut off the compensation network, and therefore a much better representation of the actual peak value can be detected. This explains the rise when V_{Peak} is compared to the actual peak of the input signal. Between 1 V and 1.1 V the output curves start to drop indicating that the comparator's ICMR has been exceeded. At higher temperatures this value increases, due to a decrease in V_{TH}. Furthermore, the unevenness, caused by using two periods instead of one to detect the peak, shifts to the left, because the leakage current increases due to an decrease in V_{TH}. Overall a large deviation occurs here in comparison to the input signal with lower frequencies. This is due to the comparator. The preliminary goal of a comparator whose gain is above 40 dB at 100 kHz is achieved. However, the pole at the comparator output is at less than 100 kHz and therefore changing the gain over the given frequency range.

The effect of the leakage compensation network is shown in Fig. 3.7. The positive half wave of a sinusoidal signal with an amplitude of 600 mV and a frequency of 10 kHz is used as input for the peak detector. The detector has been implemented once with and once without the compensation network.

At a temperature of 140 °C it can be seen that over a longer period of time the uncompensated output voltage keeps rising. Every time the input reaches another peak, the output of the comparator drops just enough to enable leakage through M_1. The result is an ever-rising output voltage. The compensation network on the other side works as previously described. If the current is small, and therefore leaking, it is mirrored and then subtracted at the output again. Due to this charging and discharging process, small ripples do occur at V_{Peak}, but it is kept at the peak of the measurand instead of increasing over time.

Fig. 3.8 shows the output of the peak detector over a frequency sweep. An input

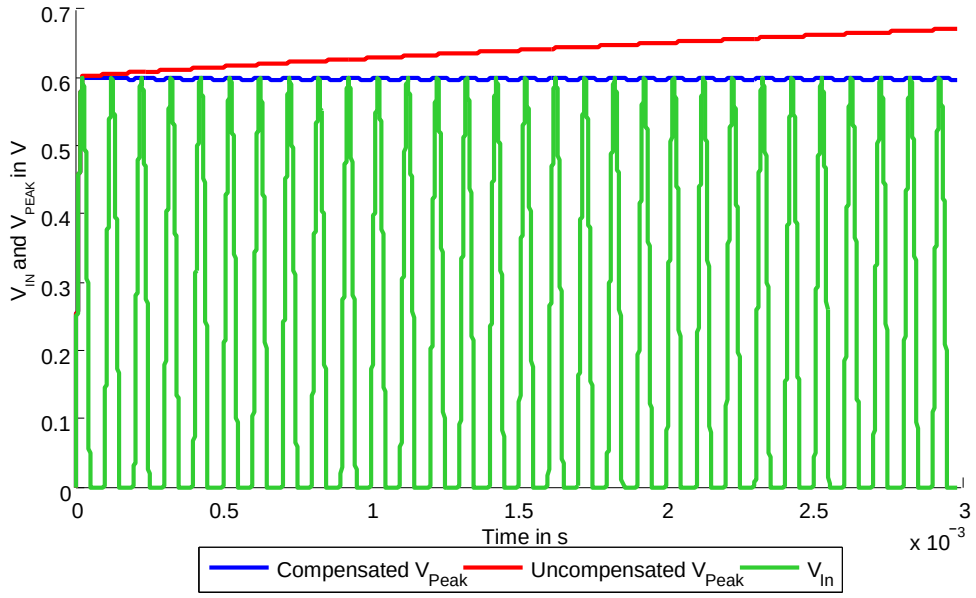


Figure 3.7: Uncompensated vs. Compensated Detector

voltage of 600 mV is chosen, as it is in the middle of the voltage range.

The output voltage of all temperatures is fairly constant up to a frequency of 60 kHz. At this and higher frequencies two or more periods are needed to charge up to the peak voltage. Afterwards the peak detector loses accuracy, implying that the dominant pole of the comparator is around this range. From this point it can be seen that the accuracy decreases similarly to the bode plot of the comparator. The sudden drop in output voltage occurring at 10 kHz for both the −40 °C as well as the 27 °C curve is due to a change in measurement time. This drop does not occur at high temperatures due to the leakage compensation network as previously shown.

3.3.3 Layout

The layout of the peak detector circuit from Fig. 3.3 is shown in Fig. 3.9. Tab. 3.2 highlights the different sections of the layout.

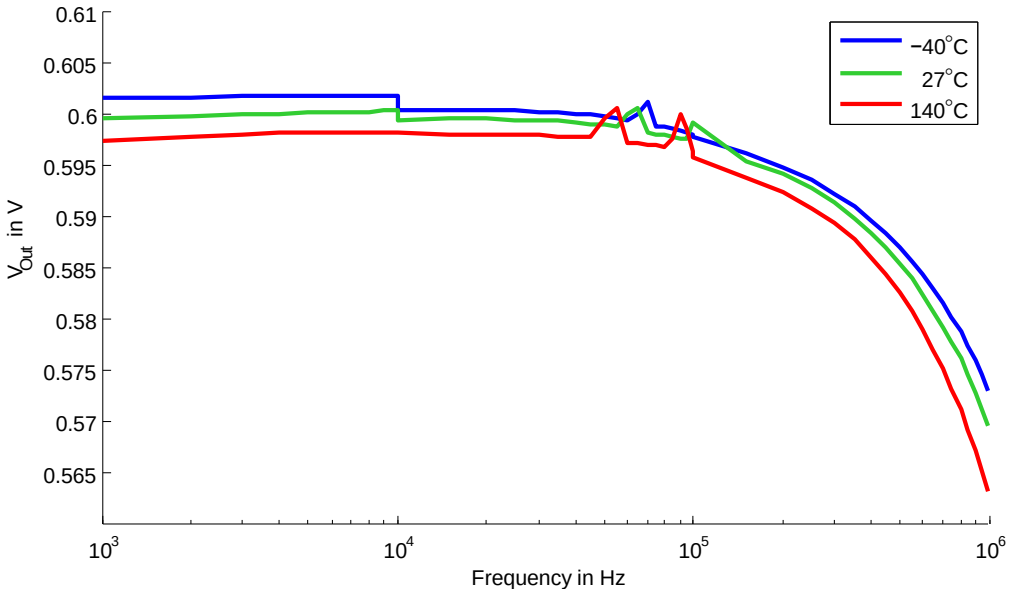


Figure 3.8: LLPD: Frequency Sweep at 600 mV Sinusoidal Input Signal

Label	**Explanation**
1	C_{Peak}
2	Current Selection Inverters
3	Biasing Current Mirrors
4	T-Gates, S_1, S_2
5	Current Selection Switches
6	M_1, M_2
7	Discharge Transistors
8	R_{Peak}
9	Inverter for Current Selection
10	Biasing Current Mirrors
11	Comparator
12	Leakage Compensation
13	Discharge Leakage Buffer
14	C_{Peak_Guard}

Table 3.2: Peak Detector Requirements

The NMOS and PMOS current mirrors are used to supply the different sections of the peak detector. The transistors have been interchanged with each other to attempt

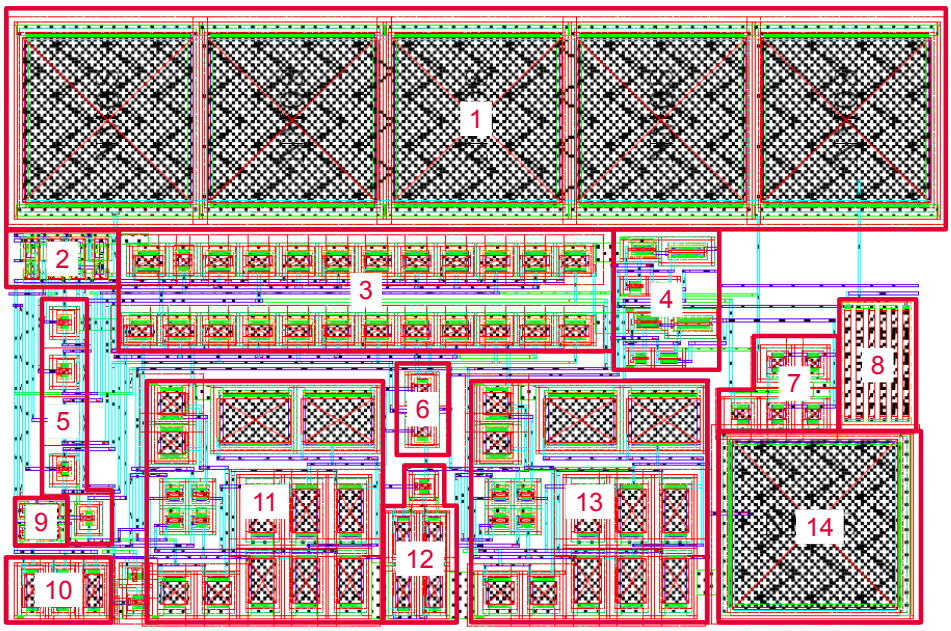


Figure 3.9: LLPD Layout

to compensate for mismatch. Since the bias current can vary to a certain extent there was no need to use dummy structures to improve the current mirror's accuracy over mismatch. Most important is the matching of the current supplied to M_1 and M_2. This is resolved as those transistors are in the middle of the interchanged current mirrors.

Ideally, M_1 and M_2 are identical in order for the leakage compensation network to work properly. To fulfill this requirement, their layout must be given special attention. They are placed in a similar environment with exactly the same setup for their gate, source and drain connections. Since enough space was available, they are implemented with no other bordering transistors. The combination of those actions allows for the transistors to function in almost an identical manor.

Furthermore special attention is given to the differential input pair of the comparator as well as the buffer. Each input pair is made up of 4 transistors which are aligned in a common centroid layout to minimize the effect of linear gradients on the offset.

3.3.4 Conclusion

A simple low power peak detector using a PMOS transistor to charge V_{Peak} has been modified to improve its behavior over long periods of time. Given enough time, leakage current, as well as the non-ideal comparator, eventually modify the output of the detector. To prevent this, a leakage compensation as well as a low leakage discharge network have

been implemented. Together they minimize the effect leakage can have on the output voltage, as shown in Sec. 3.3.2. However, the drawback is that much more area is needed than in the simple version of the peak detector. The accuracy of the peak detector is mainly based on the comparator. For this application the bias current was chosen to be low to minimize power consumption. If more exactness is needed the comparator can also be implemented with a cascoded output stage for the overall gain, or the current can be increased to improve the result at higher frequencies. The buffer used to generate V_{Peak_Guard} serves two functions. First, it generates a copy of V_{Peak} needed for the low leakage discharge network. Furthermore, it can also be used as input to the ADC as it is less sensitive. Overall, a buffer will be needed, so only another transmission gate has to be added to complete the discharge network. Therefore, only a small amount of more area has to be given up in order to gain this advantage. It has been shown that the leakage compensation network performs best at high temperatures. Depending on the application, it may be well worth including it, because similarly to the transmission gate, the total area consumed is rather small. Whereas other implementations either need a clock signal or an OTA to detect a maximum, this implementation is solely based on the clamped comparator. This is an advantage regarding power consumption but a limitation when considering the frequency of the input signal.

3.4 Clocked Signal Detector

A different approach to detecting the maximum of an input signal is shown in Fig. 3.10. Delaying a copy of the input signal and then comparing it to its original allows for the comparator to detect not only the maximum but also the minimum of the sinusoidal input signal. In order to show the full use of the detector, the signal to be measured is a sine with a DC offset of 600 mV.

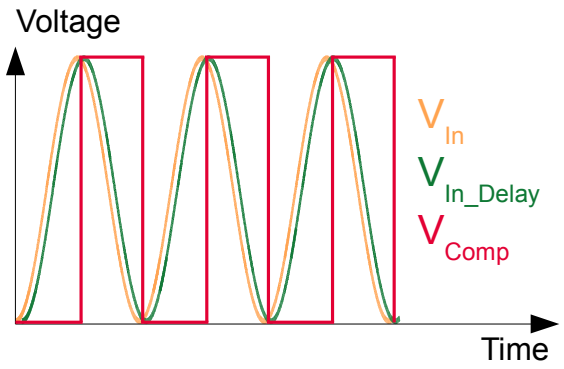


Figure 3.10: Clocked Signal Detector Principle

However, in order to measure maxima and minima with this approach, much more

circuitry compared to the original peak detector must be used. Fig. 3.11 shows a simplified representation of the implemented schematic. The circuit now consists of an extra sample and hold to delay the input signal, as well as another buffer to charge C_{Max} and C_{Min}. Even if adaptively biased OTAs are used, the current consumption will exceed that of the regular peak detector.

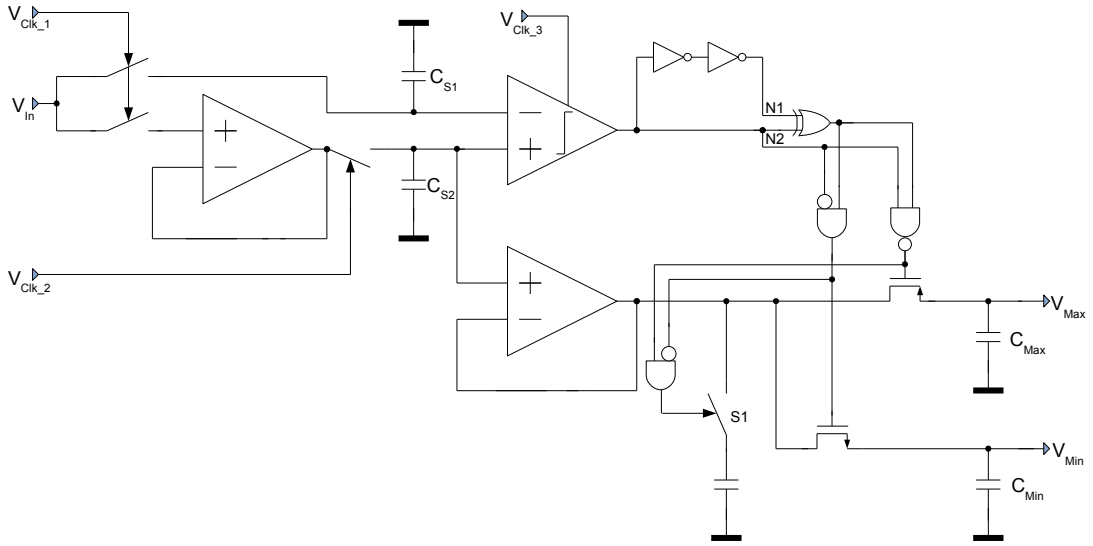


Figure 3.11: Clocked Signal Detector Schematic

3.4.1 Implementation

Three clock signals are needed in order to implement this circuit. Fig. 3.12 shows the timing diagram needed to achieve the delay as well as synchronize the comparator. V_{Clk_1} is used to sample the input voltage onto C_{S1} as well as the input of the buffer. V_{Clk_2} is non-overlapping with V_{Clk_1}, and used to create the delayed input sample stored on C_{S2}. The comparator, shown in Fig. 3.13, is then clocked by using V_{Clk_3}, which has the same period as V_{Clk_1} but a shorter duty cycle. All in all, the comparator will be forced to decide once the newest sample is stored on C_{S1}, which is just before C_{S2} stores the same sample. As seen in Fig. 3.10, the comparator output switches to a logic high once the voltage across C_{S2} is greater than C_{S1} and vice versa.

Since the overall system is clocked, a clocked comparator is implemented, as it has certain times when it is not used. This is advantageous for instance when V_{Clk_2} is high because the voltage across C_{S2} changes and it could result in a fluctuating output at the comparator. When using a clocked comparator the reset phase can then be chosen during this time. The schematic of the implemented comparator is shown in Fig. 3.13.

The input stage of the comparator is once again designed to have a large g_m by

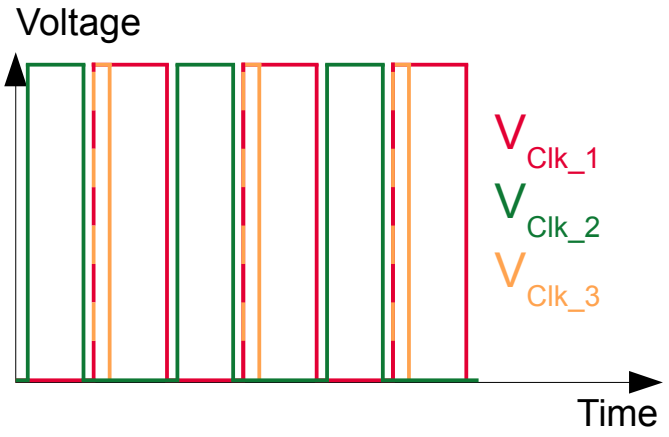


Figure 3.12: Clocked Signals

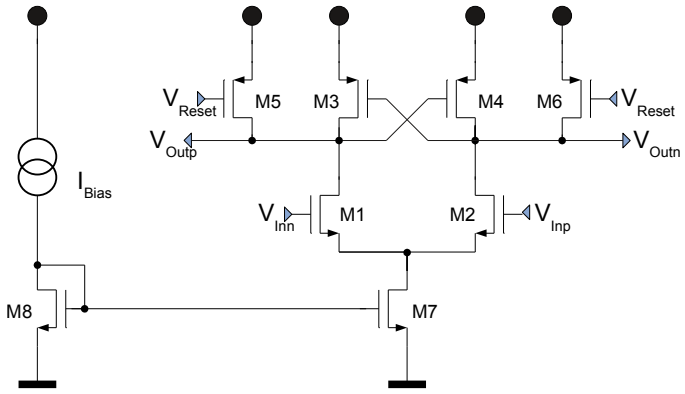


Figure 3.13: Clocked Comparator

choosing a large width. The channel length is slightly increased to keep the offset to a minimum. The latch consisting of M_3 and M_4 has a higher g_m as well. Once the input stage has decided upon which signal is larger, the voltage at either V_{outp} or V_{outn} starts to drop, controlling M_3 and M_4 respectively. A larger g_m then causes a much faster rise in potential at the opposite output node. The dimensions of M_5 and M_6 have to be chosen so that they are capable of reseting both output nodes to V_{DD}, effectively setting $V_{DS-M5,6}$ to zero. An advantage of using this clocked comparator is the small propagation delay. However, since a differential output is used, a differential to single ended OTA has to be used. This further increases the propagation delay.

Since the comparator only detects the greater of its input signals, therefore signaling once a change occurs, current starved inverters along with an XOR-gate can be used to set a time limiting the charging time during which the switches are open. In this

constellation the inverters determine the amount of time to charge the capacitors. The XOR-gate is used to cut off this time period, while the AND and NAND-gates determine whether a rising or falling edge occurred. Once the output of the comparator switches to high, the current starved inverters delay this signal. At this time, the XOR-gate has a logic zero and a logic one at its two input terminal. It therefore delivers a logic one at its output. This value is then input to the AND-gate, where the second input is the comparator output inverted, as well as a NAND-gate along with the output of the comparator. The output of the AND-gate results in a zero keeping the NMOS switch open so as not to change the voltage across C_{Min}. The NAND-gate receives a zero as well as a one which yields a zero. This closes the PMOS switch, allowing for C_{Max} to charge. In the meantime, the current starved inverters backtrack the one from the comparator output to eventually deliver it at the input of the XOR-gate. Once this happens the XOR-gate has a one at both inputs, which causes a zero at the output. A zero from the XOR-gate and a one from the comparator output result in the NAND-gate opening the PMOS switch. The NMOS switch stays open as the comparator output is inverted to a zero which is anded with another zero from the output of the XOR-gate. The same theory applies if the comparator switches from a logic high to low. Initially, the XOR-gate delivers a one, which, anded with an inverted zero from the comparator, closes the NMOS switch to charge C_{Min}. As a result, the PMOS switch stays open. Once the zero has passed through the inverters the XOR-gate changes to a zero as well, forcing the NMOS switch to open. Table 3.3 gives an overview of the states of the switches depending on the output of the comparator. Note that S_1 is implemented as a transmission gate with an inverter and uses positive control logic.

Comp Out	**XOR Out**	**NMOS-Switch**	**PMOS-Switch**	**Switch S_1**
0	0	0	1	1
⌟⌜	1	0	0	0
1	0	0	1	1
⌝⌞	1	1	1	0

Table 3.3: Logic Summary

Instead of implementing a transmission gate, only the PMOS transistor was chosen as a switch to charge C_{Max} as its values are above $\frac{V_{DD}}{2}$. Similarly, the NMOS switch is fully closed given a low potential at its source. Finally, since C_{Max} and C_{Min} are only connected to the output of the buffer for short amount of times, another capacitor is connected via S_1, which is a transmission gate, as lower and higher voltages may occur. S_1 is controlled by another AND gate, which uses the signals from the NMOS and PMOS switch, controlling $V_{Max,Min}$ in order to only be connected when neither of those is closed. This capacitor is very small as its purpose is to only keep the buffer

stable. It is disconnected once a maximum or minimum is detected, as it would only be an unnecessary load slowing down the buffer.

The schematic used for the current starved inverter is shown in Fig. 3.14. The time needed for the inverter to either raise or lower its output is proportional to the available current. Given that the fastest signal to detect is 100 kHz, the time for both inverters can be approximated as follows. Given a supply voltage of 1.2 V, the maximum input signal in order for the buffers to work properly would be 500 mV V_{PP}. Looking at a table of a sinusoidal signals with this V_{PP}, it can be seen that between 87 ° and 93 ° the offset is less than 1 mV. For a 100 kHz sinusoidal signal this is equivalent to just under 200 ns. Within this time span, the inverters have to pass through the respective logic value as well as the other gates to open and close the switches in time. With this time limit, the current through the inverters can be trimmed until the time limit is reached.

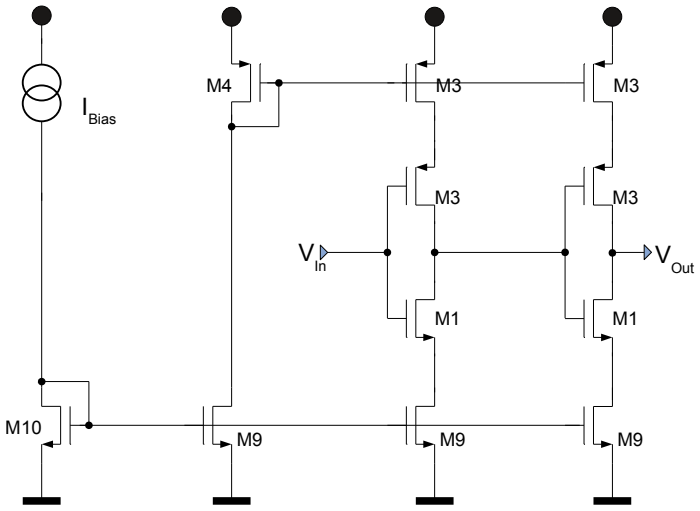


Figure 3.14: Current Starved Buffer

Since different clock signals are already used in this circuit, flip flops with the same time interval may be used instead of using current starved inverters. With either implementation, if the input signal has a lower frequency, either the clock frequency or I_{Bias} can be reduced. If a higher accuracy is required they can be increased as well.

The buffer delaying the input signal as well as the one used to charge $C_{Max,Min}$ is the adaptively biased OTA from Sec. 2.6. The buffer at the output must especially be capable of charging C_{Max} quickly. In order to do so, a change in bias current is ideal, since otherwise the buffer only has to be able to follow the input signal, whereas in this case the capacitor may have to be charged from zero to close to V_{DD}. Since the original objective was to detect the peak of a sinusoidal input signal, an NMOS input stage was chosen. This limits the ability to detect minima, as only the PMOS input stage can reach

the lower supply voltage.

The clock frequency of the overall circuit was chosen with 1 MHz at ten times the maximum input signal frequency. This is actually one way of reducing power consumption. If the input signal is sampled 10 times during one period the sampling clock is delayed to allow the maximum and minimum to occur during these sampling times. If this cannot be done, the clock frequency has to be increased in order not to miss the target areas.

3.4.2 Results

Given the topology of this signal detector, the input test signal has been adapted in order to get the best use of the circuit. Instead of only the positive half wave, a sinusoidal signal at different frequencies with an offset of 600 mV is used. A sweep over the amplitude at three temperatures has been performed. For this implementation a V_{DD} of 1.2 V has been used. On average, this architecture has a power consumption of less than 36 μW.

Fig. 3.15 shows the simulation results if a 1 kHz signal with the aforementioned offset is applied to the clocked signal detector (CSD). The amplitude is increased from zero to 200 mV in 5 mV steps.

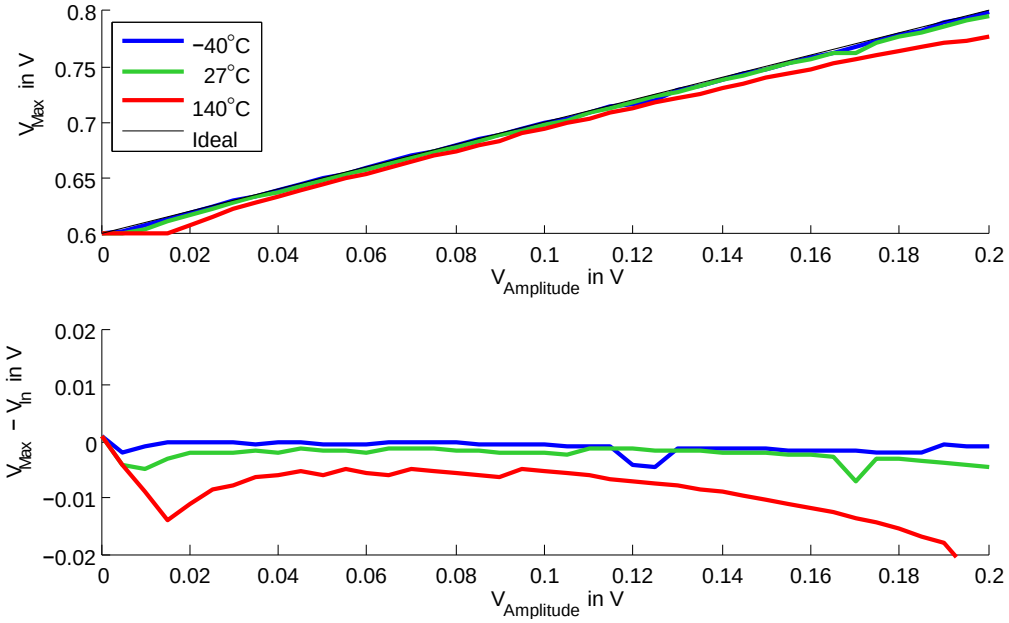


Figure 3.15: CSD V_{Max}: Amplitude Sweep at 1 kHz Sinusoidal Input Signal

It can be seen that the detector needs a certain minimum amplitude to work properly. Especially at low frequencies and a very small amplitude, the voltage change across C_{S1} and C_{S2} is very small within one time step. Due to errors caused by non-ideal factors such as the offset of the buffers used or leakage and charge injection, the change in voltage

within a given time step may be too small to be accurately detected. Once the amplitude is large enough to not be affected by those parasitics, the peak detector closely follows the ideal output response. Some peaks and drops do occur, but are the result of a shortened and less accurate simulation, due to having to use a clock cycle in the system, which significantly increases simulation times. The deviation of the output signal to the input signal is proportional to the amplitude. This behavior can be explained by the use of several buffers throughout the detector circuit. The circuit error is given by Eq. 2.2.11. If the OTA is used as a buffer the feedback factor β equals one. When the gain of the OTA is constant, it can be seen that accuracy is dependent on the input amplitude. A higher input signal yields a larger deviation from the desired output signal. The only way to correct the error would be to improve the OTA's gain, for instance by implementing cascodes in the output stage if needed.

Fig. 3.16 shows the obtained results for an input signal with a frequency of 10 kHz. The bottom of the graph shows a very consistent output signal once the aforementioned minimum is exceeded.

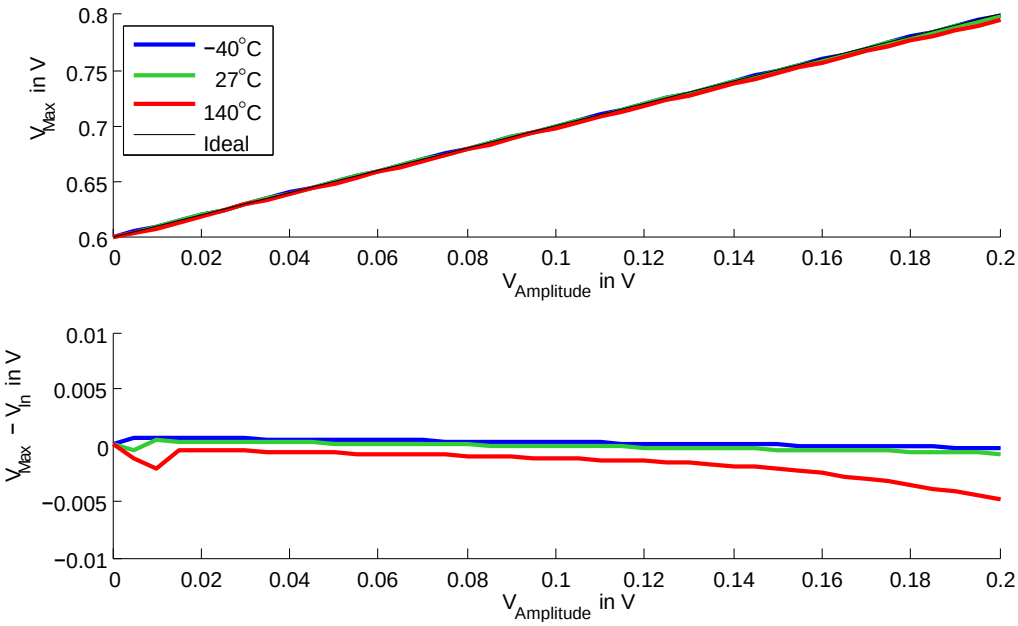


Figure 3.16: CSD V_{Max}: Amplitude Sweep at 10 kHz Sinusoidal Input Signal

The offset in accuracy over the temperature range is caused by the buffers as well. At higher temperatures the gain of the OTA decreases. An increase in temperature results in larger currents due to a decreasing V_{TH}. This causes a rise in V_{GS}, effectively decreasing the overall output resistance and therefore the gain of the OTA. Once again, Eq. 2.2.11 shows that less gain will cause a greater deviation of the final output value compared to

its respective input signal.

The output of the clocked peak detector, given a 100 kHz sinusoidal input signal, is shown in Fig. 3.17.

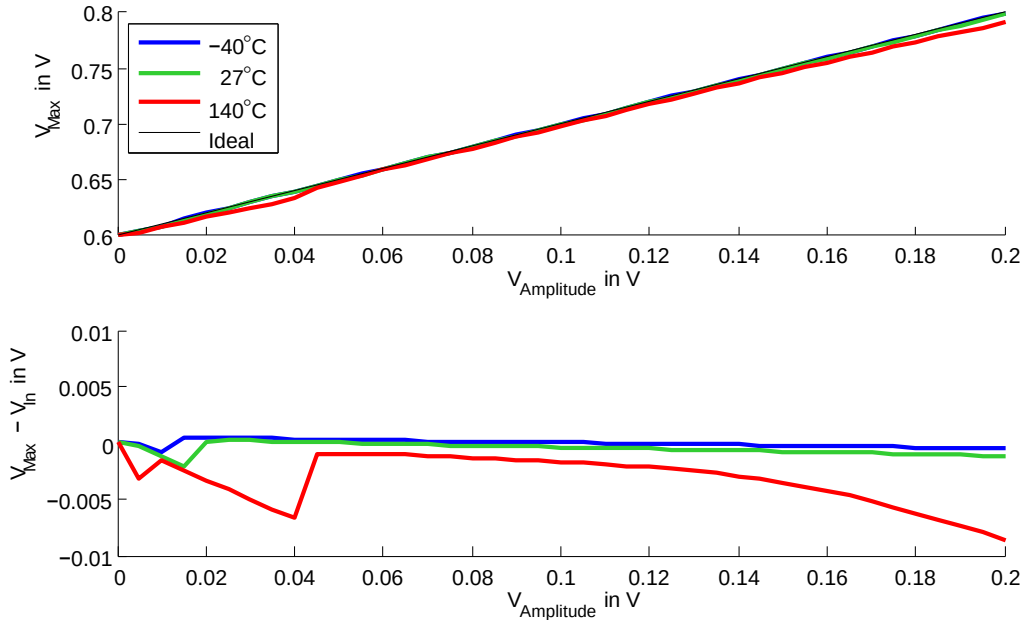


Figure 3.17: CSD V_{Max}: Amplitude Sweep at 100 kHz Sinusoidal Input Signal

Overall, similar behavior to the 10 kHz input signal can be observed. Once the minimum input amplitude is exceeded, the peak detector output gives a good representation of the input. However, the overall deviation has slightly increased, which is due to the fact that at this frequency the buffer has a lower gain than at lower frequencies. The minimum voltage needed for the detector to work increases with temperature as the difference in voltages across C_{S1} and C_{S2} becomes smaller. At 140 °C the voltage across C_{S2} is less than the actual amplitude because the buffer is less accurate. Once the sinusoidal signal stored across C_{S1} begins to drop, V_{CS1} is theoretically at its maximum and should be detected as such by the comparator. However, due to the offset, for a short amount of time the signals are equivalent and the comparator cannot detect any difference. Therefore, the detected peak occurs later, and the final value does not represent the actual amplitude of the input signal.

Figs. 3.18 through 3.20 show the minimum output voltages recorded along with their deviations from the ideal.

Overall, the minimum value detected shows behavior equivalent to the maximum value. However, when looking at the deviation from the ideal magnitude, the curve slightly increases. Similarly to before this is explained by Eq. 2.2.11. The smaller the signal

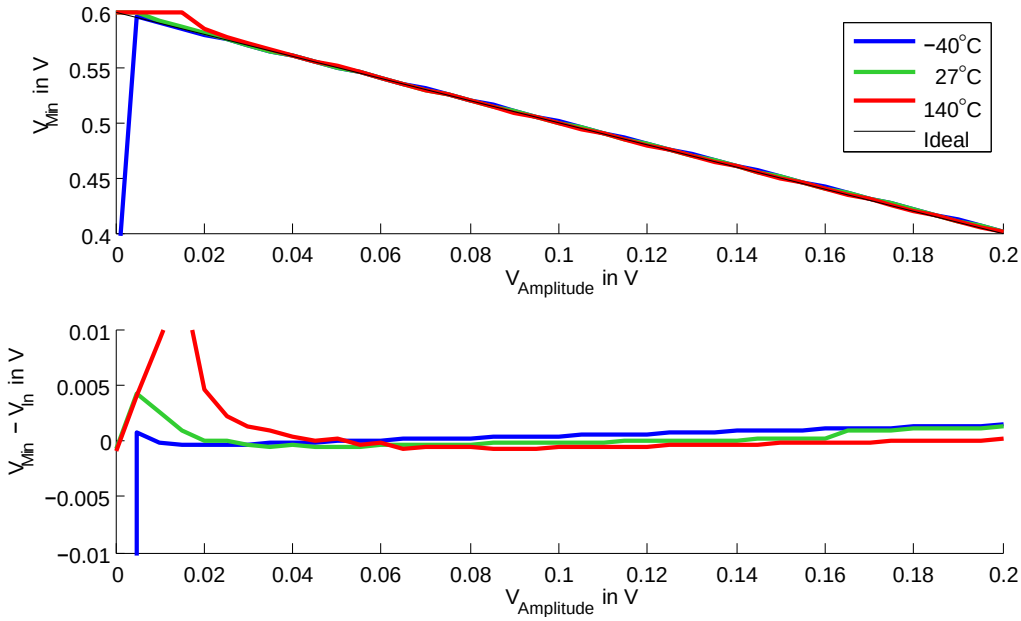


Figure 3.18: CSD V_{Min}: Amplitude Sweep at 1 kHz Sinusoidal Input Signal

amplitude, the more accuracy can be obtained when using a buffer.

3.4.3 Conclusion

The implemented clock signal detector is based on the principle of comparing a delayed version of the input signal to the original. Therefore the maximum occurs once the buffered input is larger, and the minimum at the point when the held-up signal becomes smaller than its counterpart. As presented in the results section, accuracy is mainly dependent on the gain of the implemented buffers and can be improved by using a cascoded output stage. Since a clock signal is used to sample and create the delayed signal, the fastest detectable signal is simply dependent on the available clock. This is an advantage compared to the low leakage peak detector, where the maximum detectable frequency is dependent on the OTAs used in the system. If the input signal is well known, the clock frequency can be adapted in order to reduce current consumption throughout the system. Probably the biggest advantage besides detecting the minimum is robustness against leakage. Instead of charging the capacitor to a certain voltage in this implementation the output simply follows the input during the permitted time periods. So every time a peak is detected, the buffer charges C_{Max} to its input voltage but never beyond that. Therefore, leakage caused by inaccuracy through the comparator does not have any effect upon the output voltages. However, the discharge network from Fig. 3.3 may still be used in order to reset the signal detector without affecting the measured

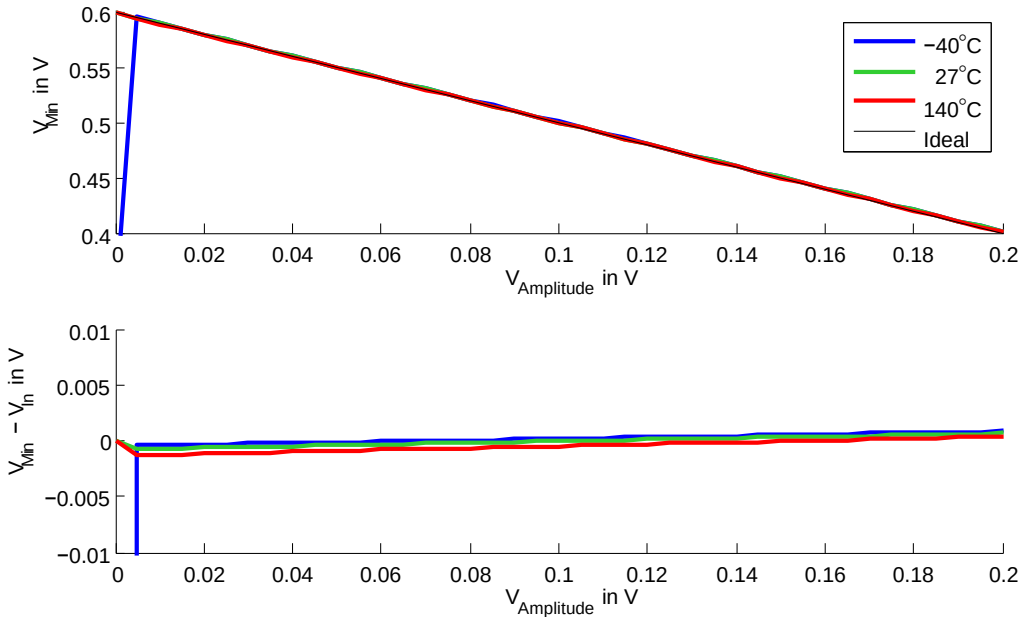


Figure 3.19: CSD V_{Min}: Amplitude Sweep at 10 kHz Sinusoidal Input Signal

output values during normal operation.

The ability to detect the minimum as well as maximum of a sinusoidal input signal comes with a couple of drawbacks, mainly concerning area and power consumption. Not included in this detector was the generation of the clock signal. Depending on availability, the clock signal might need to be generated, which would result in more circuitry and further increase current consumption. Furthermore, one buffer has to be used to create the delayed input signal whereas another buffer charges the output capacitors. Depending on the desired input signal range, rail-to-rail buffers might need to be used in order to guarantee functionality as the amplitude increases. Both buffers need additional capacitors as they are adaptively biased. This allows them to quickly follow the input signal, which is needed when there is only a small time period to load the output capacitors to their final value. However, if not compensated, the output will oscillate and current consumption would increase even further. Additionally, it is beneficial if C_{S1} and C_{S2} are not kept to a minimum as any leakage and charge injection would have more negative effects.

3.5 Differentiator-Based Signal Detector

In order to detect the maximum of the input sinusoidal signal the differentiator can be used as well. Differentiating a sine simply results in the cosine as shown in Fig. 3.21.

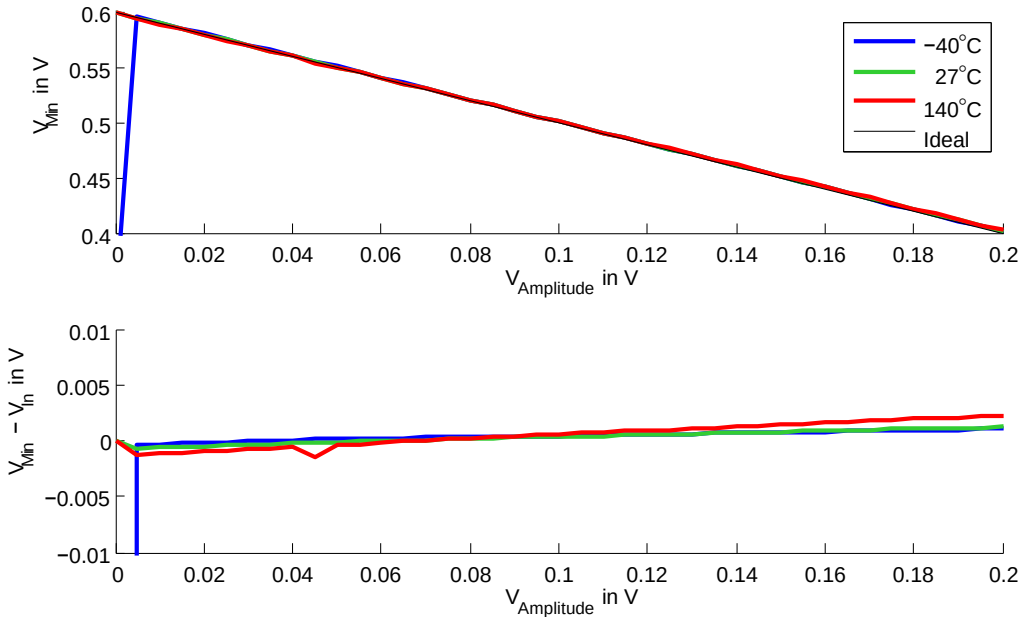


Figure 3.20: CSD V_{Min}: Amplitude Sweep at 100 kHz Sinusoidal Input Signal

Every time the cosine crosses 600 mV the sine is either at a maximum or minimum depending on whether the cosine rises or falls. In order for this theory to work an offset of $\frac{V_{DD}}{2}$ is a prerequisite. Similarly to the clocked signal detector, this circuit's advantage is also the capability to detect the minimum with hardly any extra circuitry.

This approach shares a lot of the attributes of the aforementioned detectors. Despite the capability of detecting the peak as well as a valley, no clock signal is used in this implementation. However, along with the capacitors for the maximum and minimum value another one has to be used for the differentiator. Furthermore, given the nature of a differentiator, the approximate range of the input signal frequency has to be known in order for the resulting cosine signal to not become too small for the comparator to easily decide once the signal crosses 600 mV. Eq. 3.5.1 shows the effect the capacitor may have on the input signal of the differentiator [1].

$$V_{Diff} = \text{-}C_{Diff}R_{Diff} \cdot \frac{\partial \text{Asin}(2\pi ft)}{\partial \text{t}} \tag{3.5.1}$$

where A is the amplitude. The resulting cosine is then given as

$$V_{Diff} = \text{-}C_{Diff}R_{Diff} \cdot 2\pi \cdot \text{f} \cdot \text{A}\ \cos(2\pi \text{ft}) \tag{3.5.2}$$

Once V_{Diff} crosses $\frac{V_{DD}}{2}$ monoflops are used to open switches allowing the output capacitor to charge to either the maximum or minimum of the input signal. Similarly to

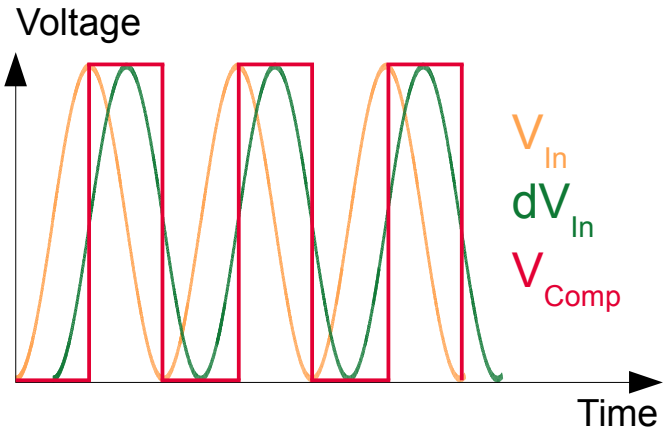


Figure 3.21: Differentiator Signal Detector Principle

the clocked signal detector current starved inverters or flip flops could be used instead.

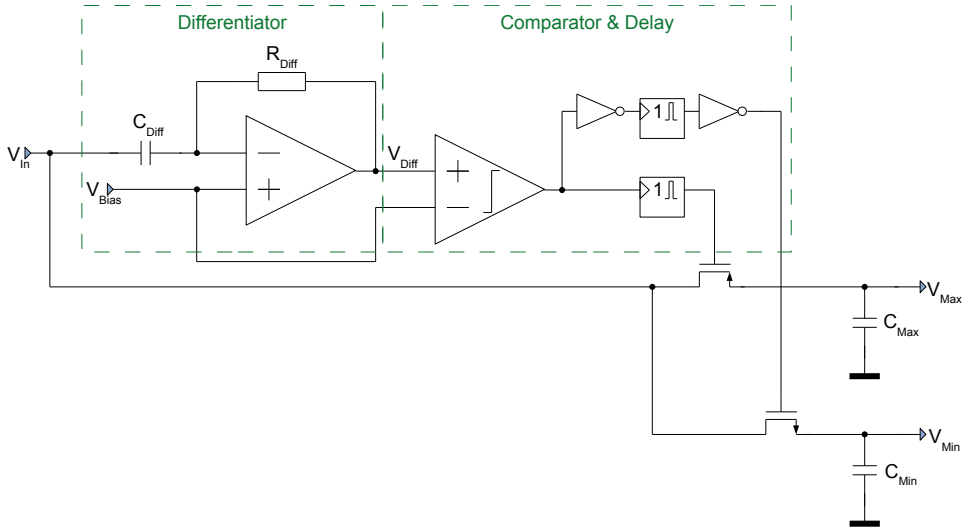


Figure 3.22: Differentiator Signal Detector Schematic

3.5.1 Implementation

Since the input signal frequency varies as does the amplitude C_{Diff} was made adjustable with two select bits. If the frequency is known the capacitor can be chosen accordingly for V_{Diff} not to become either too large or small allowing the comparator to make a quick decision. Fig. 3.23 shows the equivalent circuit used for C_{Diff}.

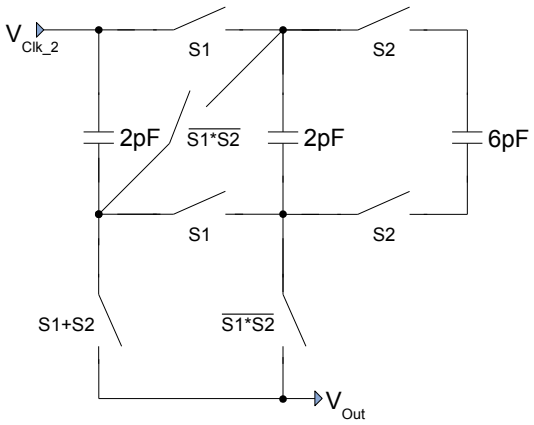


Figure 3.23: Differentiator Capacitance Network

Tab. 3.4 shows the different available capacitances respectively to the select bits.

S_1	S_2	**Capacitance**
0	0	1 pF
0	1	2 pF
1	0	4 pF
1	1	10 pF

Table 3.4: Differentiator Capacitance Truth Table

R_{Diff} was chosen with 1 MΩ as it gives good results for V_{Diff} in combination with the different capacitances.

The comparator used in this design has the topology of a Miller OPA as seen in Fig. 3.24. One advantage compared to the current gain structure is that in this two stage OPA the overall gain is a combination of first and second stage which is typically fairly large. Since the capacitance at the output node is small the dominant pole is automatically at higher frequencies. In order to ensure that the non-dominant pole is even higher the capacitance at node $N1$ (Fig. 3.24) was kept to a minimum. When considering the resistance at this node, a trade-off occurs. A large resistance would increase the gain of the first stage helping the overall circuit gain but also decreases the non-dominant pole frequency. To avoid risking a shift of the second pole, the length of the PMOS current mirror along with M_5 was slightly reduced and the output resistance along with it. These steps result in a uniform gain within the given frequency range. Another advantage here is that the comparator only has to have a higher gain at $\frac{V_{DD}}{2}$ as V_{Diff} will be compared to this value. So the maximum accuracy is only needed close to this value instead of the entire input range of the comparator.

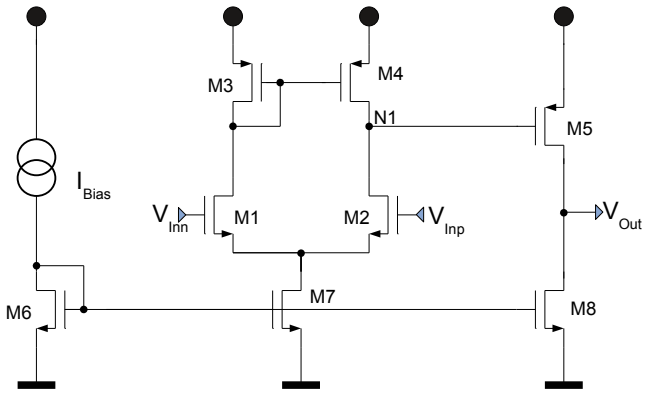


Figure 3.24: Comparator

Once the comparator has detected that V_{Diff} has crossed $\frac{V_{DD}}{2}$ monoflops are used to set a time limit to close the switches to charge V_{Max} and V_{Min}. If V_{Diff} rises above 600 mV the output of the comparator switches to high. Briefly, the monoflop, Fig. 3.25, switches to zero effectively closing the PMOS transistor to allow C_{Max} to charge. The sub circuit of the monoflop is shown in Fig. 3.25.

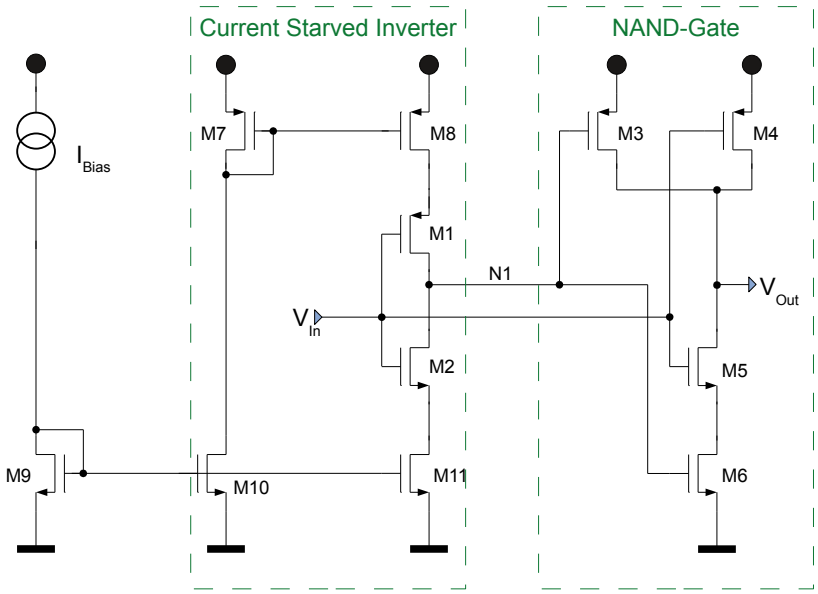


Figure 3.25: Monoflop

The monoflop consists of two main components: a current starved inverter and a NAND-gate. The former is responsible for the amount of time when the monoflop's

output is zero while the latter does the actual resetting to V_{DD}. The delay time can therefore be controlled by the supply current I_{Bias}. Once the comparator switches its output to high the potential at node $N1$ is still high, because the inverter is slowed down. Therefore both inputs to the NAND-gate are at logic high turning on both NMOS transistors and resulting in a zero at the output allowing C_{Max} to charge. Once the inverter has changed the potential at $N1$ to a logic low, the NAND-gate flips its output to a logic high and opens the switch again. In order to use the same monoflop architecture, two inverters are used to detect the falling edge of the comparator output and control the NMOS switch for C_{Min}. Tab. 3.5 summarizes the behavior of the monoflop given different inputs.

V_{In}	V_{N1}	V_{Out}
0	1	1
⌐	1	0
1	0	1
¬	0	1

Table 3.5: Monoflop Truth Table

3.5.2 Results

The differentiator-based signal detector implemented has a power consumption of less than 18 μW given a V_{DD} of 1.2 V. The corresponding output signals to an input amplitude sweep at 10 kHz and 100 kHz are presented in this section. At a frequency of 1 kHz the capacitance of the differentiator would have to be in the order of 100 pF for V_{Diff} to not become too small. However, this capacitance would be extremely large if implemented on chip and is therefore not an option for a peak detector. Furthermore the OPA used would have to be adjusted as it would have to be capable of supplying enough current. As the size of C_{Diff} can be adjusted simulation results with higher input signal frequencies have been obtained.

The simulation results when using an input sinusoidal signal with a frequency of 10 kHz and a varying amplitude of the differentiator signal detector (DSD) are shown in Fig. 3.26. The difference of the measured output compared to the input is shown on the bottom half of the graph. C_{Diff} was adjusted to be 10 pF.

A certain minimum is needed as if the input signal amplitude is too small, the comparator will not be able to differentiate in time between V_{Diff} and $\frac{V_{DD}}{2}$. However a very interesting result is that temperature does not really have an effect upon V_{Max}. As the comparator determines when the sampling of the input signal takes place, and its gain is very large due to its two stages, little variation is expected there. Furthermore, the output capacitor is not under the influence of any leakage current which could affect

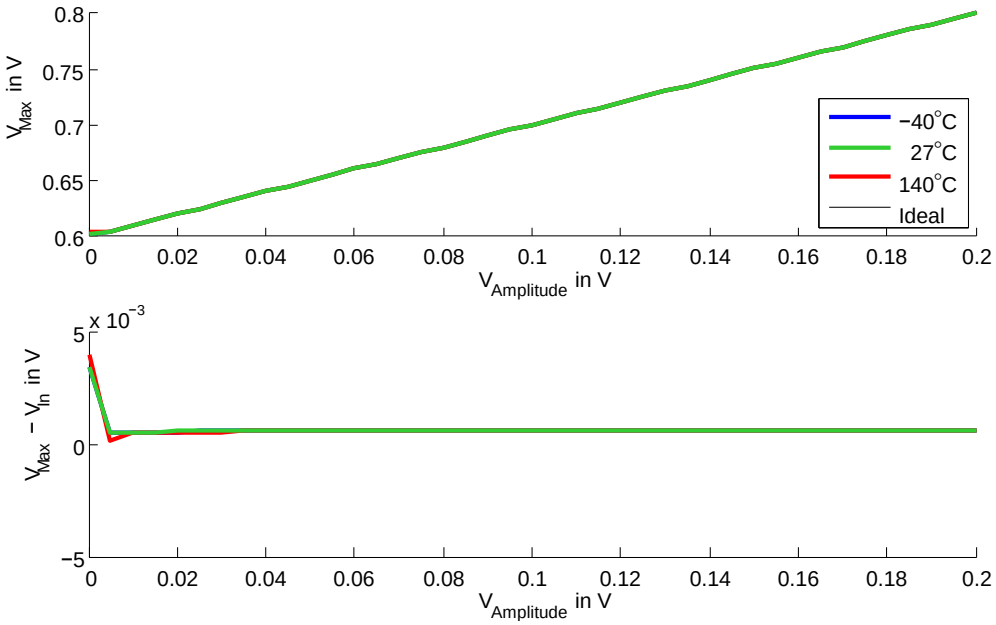


Figure 3.26: DSD V_{Max}: Amplitude Sweep at 10 kHz Sinusoidal Input Signal

the final outcome. The only switch present here is kept at the lowest potential compared to the low leakage detector which fluctuates. The error over the amplitude range is kept to a minimum throughout the amplitude range. This is possible as only the times when V_{Diff} crosses $\frac{V_{DD}}{2}$ are important. The error at the minimum and maximum of V_{Diff} are not of relevance as the signal at this point and time is not used any further since the signal used to charge C_{Max} is V_{In}. Most critical is the error at $\frac{V_{DD}}{2}$ which stays constant according to Eq. 2.2.11 allowing this kind of performance. Furthermore the comparator's gain is higher at the given voltage rather than if it would have to work at the limits of its ICMR.

Nearly the same behavior can be observed if the input signal frequency is increased to 100 kHz as shown in Fig. 3.27. There are slightly more fluctuations over temperature as there are at lower frequencies but overall the deviation of the output signal to the input amplitude is minimal. In order to accommodate V_{Diff}, C_{Diff} was decreased to 1 pF by setting S_1 and S_2 to zero.

The time period of the monoflop when its output is zero is determined by I_{Bias} of the inverter. For both, the 10 kHz as well as the 100 kHz simulations, the same current was used, so overall the same time frame to charge C_{Max} was allowed. However, at the higher frequency the time at which the sinusoidal is at its maximum is substantially less. Since this bias current is affected by temperature, slight variations of V_{Max} are therefore to be expected.

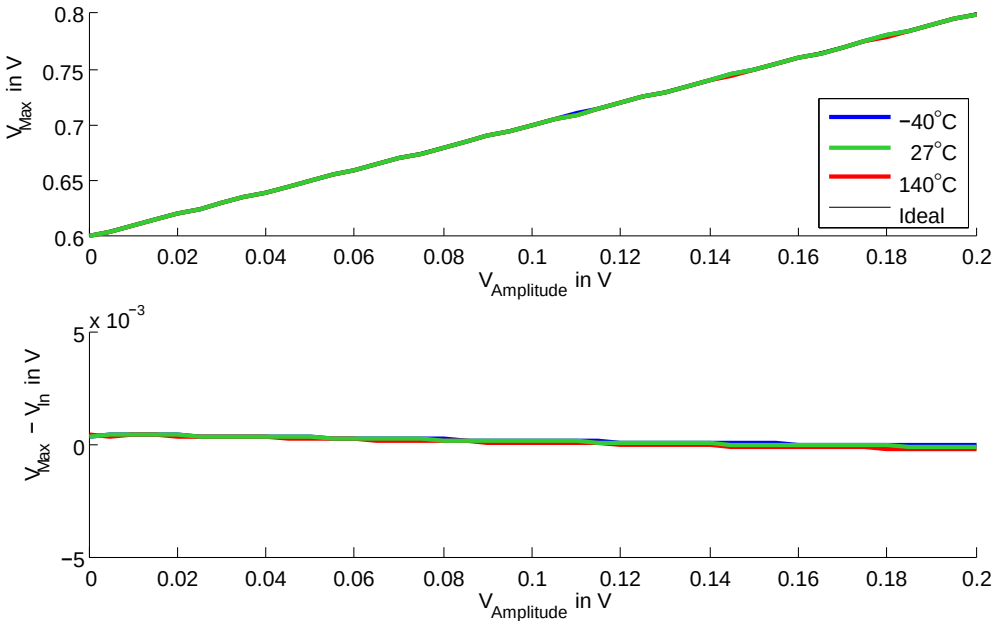


Figure 3.27: DSD V_{Max}: Amplitude Sweep at 100 kHz Sinusoidal Input Signal

The minimum voltage detected with input signal frequencies of 10 kHz and 100 kHz are shown in Figs. 3.28 and 3.29, respectively. The minimum voltages detected represent a good replica of their maxima. At a lower frequency once a certain amplitude is exceeded V_{Min} drops very constant and shows little temperature dependency. Only once the amplitude is large enough to reach the limit of the input common mode range of the OPA the temperature influences the signal detector's performance. Given an increase in frequency the previously described behaviors occur again. The temperature has more of an affect similarly to V_{Max} and as the signal amplitude is increased so does the deviation due to the OPA's limitations.

3.5.3 Conclusion

The differentiator-based approach to signal detecting gives a mixture of attributes from the low leakage and clocked signal detector. While no clock signal is used for the measurement, the capability of detecting both the maximum and minimum of the input signal is still available without having to add a lot of circuitry. The current consumption has improved compared to the clocked implementation but is still no match for the low leakage peak detector. The linearity of the output signal as well as the deviation compared to the input amplitude is quite astonishingly accurate.

The substantial drawback for this type of detector is the limitation of the frequency bandwidth. Ideally, the input signal frequency is well know, so that C_{Diff} can be adjusted

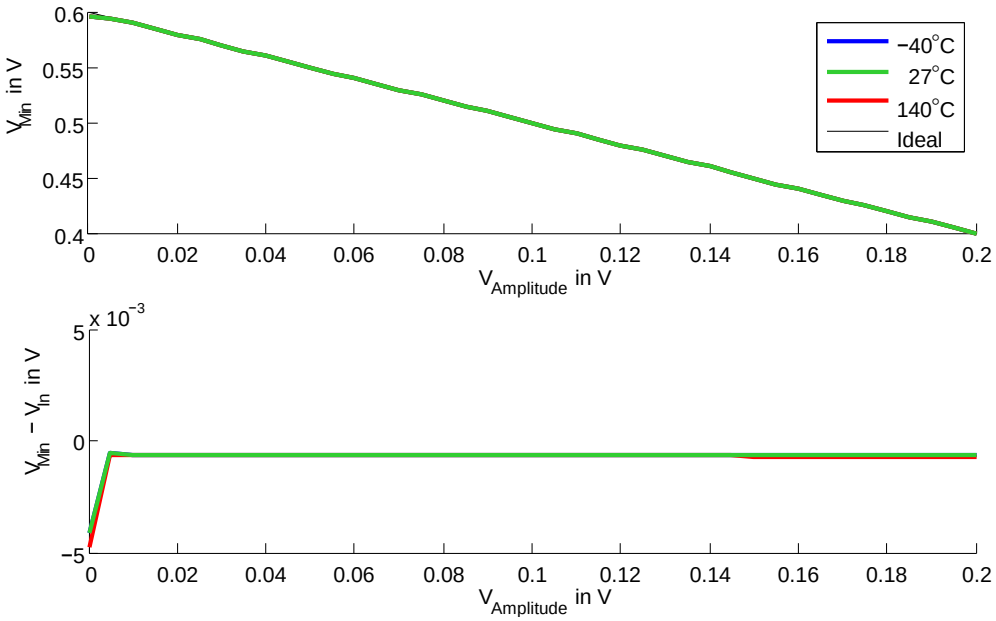


Figure 3.28: DSD V_{Min}: Amplitude Sweep at 10 kHz Sinusoidal Input Signal

accordingly. The low end of the frequency range is determined by the availability of the size of the capacitor which consumes a lot of area. Instead of the capacitance, R_{Diff} could also be adjusted, once again at the price of valuable space. The upper limit of the frequency is determined by the bandwidth of the OPA as well as the comparator used. C_{Diff} does not limit here as long as R_{Diff} can be adjusted accordingly. The bandwidth of the OPA can only be increased at the cost of a larger current consumption and is also a trade-off with respect to its gain. Compared to the clocked signal detector the highest possible frequency is limited here as well. Furthermore at higher frequencies the time of the output of the monoflop might need to be adjusted. This would result in more cycles needed to reach V_{Max} and V_{Min}.

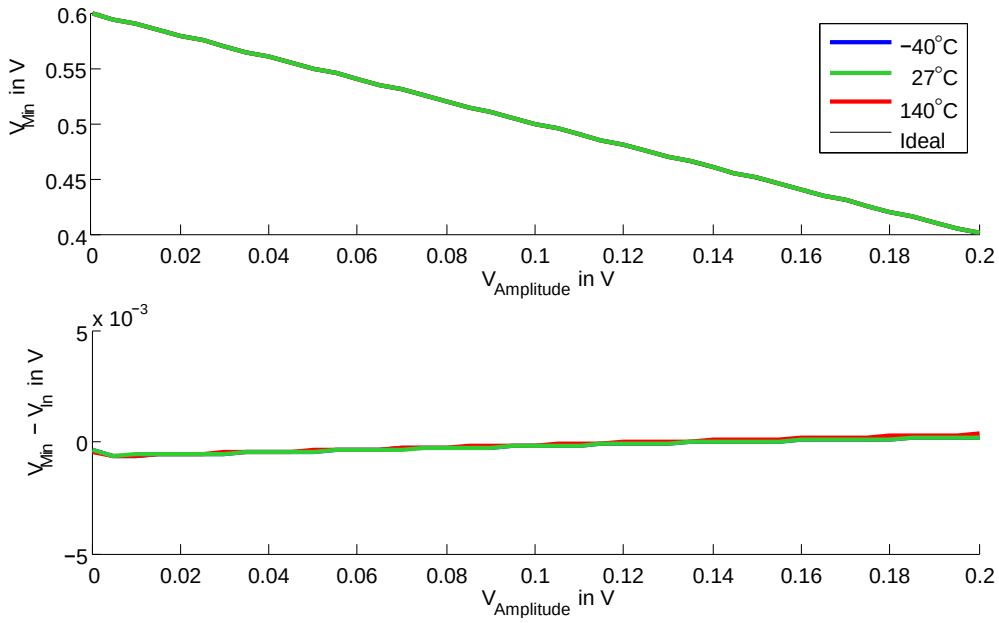


Figure 3.29: DSD V_{Min}: Amplitude Sweep at 100 kHz Sinusoidal Input Signal

Chapter 4

Conclusion

The objective of this thesis was to build different subcircuits for a sensor interface which is to be used for biological applications. Specifically, the adaptively biased OTA needed to be analyzed to obtain a more energy efficient ADC. Different, already known approaches have been tested and a new rail-2-rail implementation using the flipped voltage follower has been developed. This architecture allows for a large slew rate if needed as well as low power consumption while in steady state over the largest possible input common mode range. The different topologies have been designed and compared using a new figure of merit, which is defined as the energy consumed by the OTA while following an input step. Furthermore, the steady state as well as dynamic power consumptions are compared to show the increase in performance when needed.

The second part of this thesis was to develop a peak detector given the aforementioned specifications. Three different topologies have been developed including the low leakage peak detector, the clocked signal detector as well as the differentiator-based signal detector. While the latter are capable of detecting the maximum and minimum of the input signal, they also consume a lot more energy as well as area. As only the maximum needs to be detected and power consumption is of concern, the LLPD has been layouted. To further improve the performance, an adaptively biased OTA can be implemented for the buffer. Even though no issues have been observed during simulations, adaptively biased OTAs are known to have problems with stability. To avoid this, the peak detector has been implemented with a regular current gain OTA as it is the first tape out and the general functionality of the detector itself is of highest priority.

Appendix A

Schematics

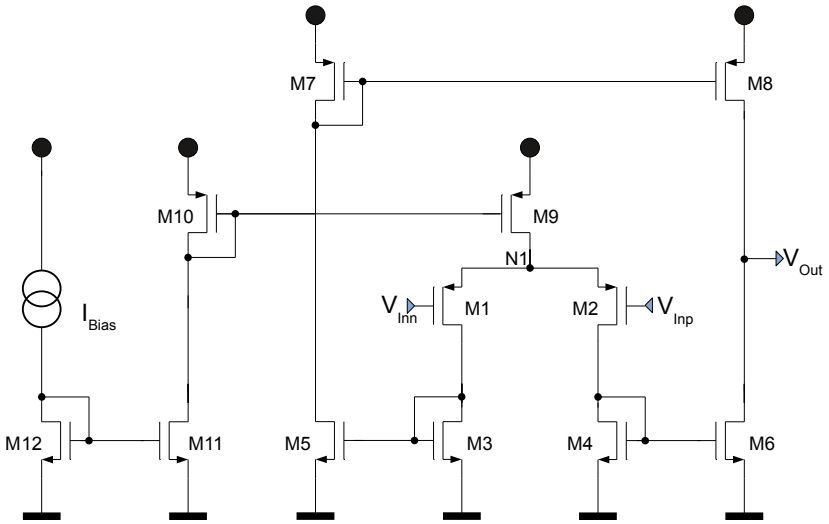


Figure A.1: PMOS Current Mirror OTA

Bibliography

[1] *Wikipedia, the free encyclopedia*, March 2011.

[2] Allen, P. E. and D. R. Holberg: *CMOS Analog Circuit Design*. Oxford University Press, 2002.

[3] Auer, M. Graz University of Technology, 2009. Analog Integrated Circuit Design and Simulation 1.

[4] Auer, M. Graz University of Technology, 2009. Analog Integrated Circuit Design and Simulation 2.

[5] Baker, J.: *CMOS, Circuit Design, Layout and Simulation*.

[6] Carvajal, R. G., J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J. A. G. Galan, A. Carlosena and F. M. Chavero: *The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design*. IEEE Transactions on Circuits and Systems, 52, No.7:1276–1291, 2005.

[7] Ferri, G., V. Stornelli, A. D. Marcellis and A. Celeste: *A rail-to-rail DC-enhanced adaptive biased fully differential OTA*. IEEE, pp. 527–530, 2007.

[8] Galan, J. A., A. J. Lopez-Martin, R. G. Carvajal, J. Ramirez-Angulo and C. Rubia-Marcos: *Super Class-AB OTAs With Adaptive Biasing and Dynamic Output Current Scaling*. IEEE Transactions on Circuits and Systems, 54,No.3:449–457, 2007.

[9] Gray, P. R., P. J. Hurst, S. H. Lewis and R. G. Meyer: *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Inc., 2001.

[10] Heer, R., J. Wissenwasser, M. Milnera, L. Farmer, C. Höpfner and M. J. Vellekoop: *Wireless powered electronic sensor for biological applications*. 32nd Annual International Conference of the IEEE EMBS Buenos Aires, Argentina, pp. 700–703, 2010.

[11] Mancini, R.: *Op Amps For Ever*. Texas Instruments, August 2002.

[12] Razavi, B.: *Design of Analog CMOS Integrated Circuits*. McGraw Hill, 2001.

[13] Wissenwasser, J., M. J. Vellekoop and R. Heer: *Highly sensitive passive radio frequency identification based sensor system*. Rev. Sci. Instrum. 81, 2010.