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RING OSCILLATOR FREQUENCY BASED CV and VARIABILITY CHARACTERIZATION

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Kurzfassung

Diese Arbeit befasst sich mit verschiedenen messtechnischen Anwendungen von Ringoszillatoren. Anhand von Frequenz- und Strommessungen kann die mittlere Kapazität einer Ringoszillatorstufe bestimmt werden. Eine zusätzliche kapazitive Last in jeder Stufe ermöglicht gezielte Messungen von bauteilspezifischen Kapazitäten mit Auflösung im Picofarad-Bereich. Die Eingangskapazität des Inverters und parasitäre Elemente werden dabei durch Vergleich mit einem Referenzoszillator berücksichtigt. Vorteilhaft bei dieser Messmethode ist, dass lokale Parameterschwankungen über eine Vielzahl von Stufen gemittelt werden. Konkret werden die Überlappungskapazität von NMOS und PMOS Transistoren und die Oxidschichtdicke von PMOS Transistoren gemessen.
Eine weitere Anwendung finden Ringoszillatoren bei der Bestimmung von Mismatch Variationen. Werden die zusätzlichen Lasten entsprechend dimensioniert, so kann die Frequenz des Oszillators sensitiv gegenüber der Variation des gewünschten Parameters gemacht werden. In dieser Arbeit wird die Variation der Einsatzspannung von NMOS und PMOS Transistoren untersucht.
Zum Schluss wird der Einsatz von Ringoszillatoren zur Verifikation von Transistormodellen vorgestellt. Gegenstand dieser Untersuchungen sind Hochvolt-LDMOS Transistoren.

Abstract

The focus of this thesis is the feasibility of ring oscillator structures for process controll and device characterization purposes. By measuring the oscillation frequency and the oscillator's current consumption, the average capacitance of one inverter stage can be deduced. Inserting an additional capacitive load makes measurements of specific device capacitances with picofarad resolution possible. The inverter's capacitance and parasitic elements are taken into account by comparisons with reference oscillators. The advantage of this method is that local variations are averaged over the number of stages. In particular, the overlap capacitance of PMOS and NMOS transistors and the oxide thickness of PMOS transistors are captured with this method.
On the other hand, ring oscillators can be used to determine mismatch variations. The oscillation frequency can hereby be made sensitive to a specific parameter by appropriately dimensioning the load. Investigations regarding the threshold voltage variability are conducted for NMOS and PMOS transistors.
Finally, ring oscillator structures to benchmark transistor models are introduced. This is done for high voltage LDMOS transistors.

STATUTORY DECLARATION

I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

August 2012 Jacob Reyes

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Chapter 1

Introduction

Modeling the behavior of integrated devices is essential for the design process of integrated circuits. With the help of simulations, the designer develops his/her product to fulfill the specifications the customer requires. To completely characterize the product, prototypes are produced and measurements compared to simulations and specifications. Therefore, the specific device models need to be appropriately accurate to correctly predict the behavior of the integrated circuit.

A fundamental step of modeling devices consists of determining how physical properties influence the device operation. A field effect transistor's (FET) capacitance, for instance, strongly influences the switching speed and parasitic effects such as the Miller capacitance. It is therefore necessary to accurately determine the gate oxide thickness that specifies the transistor's gate and overlap capacitances. Furthermore, this particular property is part of a set of parameters that semiconductor foundries provide to characterize their different technologies. Thus, monitoring the gate oxide thickness early on during fabrication allows the foundry to center its line and achieve improved conformity between different lots, for which device parameters can vary quite considerably otherwise.

This project investigates the feasibility of ring oscillator structures for parameter measurements. The first part in Chapter 2 focuses on transistor capacitances, specifically the overlap capacitance and oxide thickness. Ring oscillators with dozens of stages are designed with additional load transistors in each stage. The load capacitances are determined through frequency and current measurements. Compared to DC measurements, this technique is dynamic and more closely resembles device operation on products. Moreover, by using many stages in series, statistical variations are reduced and average values obtained for the parameters. Ideally, matching influences are thereby reduced and only process variations are of significance. Thus, the variation of the parameter from die to die, wafer to wafer and lot to lot can be monitored. The goal is to develop circuits and implement them in scribe lines to monitor the parameters and their variation.

Chapter 3 deals with the threshold voltage variation. Ring oscillators can be designed to be very sensitive to a specific parameter whose variation strongly influences the oscillation frequency. Compared to the structures in Chapter 2, these oscillators comprise only a small number of stages. Therefore, mismatch between the devices will have the greatest impact on the measurement results. The influence of process variation is minimized by

comparing only devices in close proximity to each other. Again the goal is to develop a circuit for scribe line monitoring.
Finally, ring oscillators are used to benchmark transistor models. In Chapter 4 this is demonstrated for high voltage FET devices for which simulations are compared to measurements on silicon. The performance of the device models can thus be evaluated.

Chapter 2

CV Characterization

In this chapter MOSFET capacitances are investigated with the help of ring oscillators (RO). To begin with a study of the available literature on CV characterization with ring oscillators is conducted in section 2.1, with a focus on a number of papers published by a group at IBM [1–3] and the BSIM3v3 manual [4]. In section 2.2 measurement techniques to extract the oxide thickness and overlap capacitances are developed. The corresponding circuits are introduced in section 2.3. The goal is to develop circuits that can be used to measure manufacturing acceptance parameters (MAP). The layout for these circuits will be introduced in section 2.4. Sections 2.5 and 2.6 deal with the measurement setup and measurement results. Finally, a conclusion regarding this measurement technique will be given in section 2.7.

2.1 Literature Studies

2.1.1 Capacitance Measurement with Ring Oscillators

Ring oscillators are built up of n identical stages connected in a loop as illustrated in figure 2.1. The resulting oscillation is the consequence of the delay each stage introduces when it switches states. The frequency f can be determined as in equation (2.1), where d is the delay per stage and n the number of stages. This is a good approximation for $n \gg 1$ consistent with Bhushan *et al.* [3].

$$f = \frac{1}{2 \cdot n \cdot d} \tag{2.1}$$

As mentioned, the delay d is the time it takes a single stage to change states from low to high. According to [1] it is characterized by the series resistance R_{sw} in the respective path and the capacitances C_s that need to be charged.

$$d = R_{sw} \cdot C_s \tag{2.2}$$

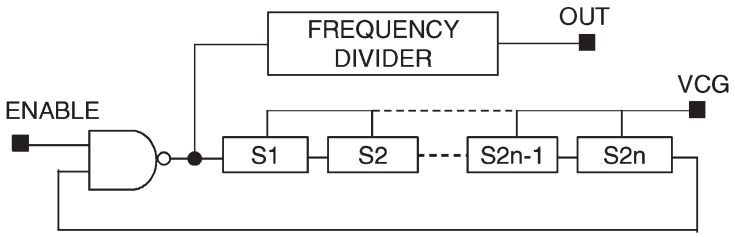


Figure 2.1: Schematic of a ring oscillator structure taken from [3]. Here, the oscillator is made up of $2n$ identical inverter stages with loads ($S_1 ... S_{2n}$), a NAND gate to enable the oscillation and a frequency divider. V_{CG} is the voltage applied to the MOSFET loads between each inverter stage.

Therefore, inserting a capacitive load C_L in between each stage – for example a MOSFET load as in figure 2.2 – increases the delay proportional to C_L. Given in [3], the capacitance C_S of one stage is calculated as

$$C_s = \frac{2d(I_{DDA} - I_{DDQ})}{V_s} \tag{2.3}$$

with I_{DDA} and I_{DDQ} being the average oscillator current in its oscillating and quiescent states and V_s the inverter's supply voltage. Comparing loaded ring oscillators – i.e. ring oscillators with an additional load between each stage – with a reference oscillator solely comprised of inverter stages makes it possible to accurately measure the load capacitances. The result is an average value over the number of stages n. For the designs in [3] the quiescent current I_{DDQ} plays a more prominent role as they are implemented in a 65-nm technology. This project, however, is designed in a 0.35-μm technology in which leakage currents are orders of magnitudes smaller than the currents in the oscillating state. Thus, their influence is negligible.

One measurement described in [3] is a CV characteristic of the MOSFET load. The gate voltage V_{CG} is increased after each capacitance measurement so that the transistor passes through all of its operating regions. The load capacitance is then plotted as a function of gate voltage. As the voltage at the drain and source oscillates between the negative and positive supply voltage of the inverter stages, the resulting capacitance represents an average over a cycle of oscillation. Figure 2.3 depicts what the result should look like theoretically.

When the transistor is switched off only the gate to drain and gate to source overlap capacitances are active, which corresponds to capacitance C_1 in fig. 2.3. This is the case as only capacitances that are recharged each period have an influence on the delay. Once the transistor is switched on and a channel has formed, the gate to channel capacitance increases the overall load capacitance, C_3. In between, the channel is forming and the capacitance increases linearly. From the capacitance in inversion and depletion an estimate for the active electrical channel length can be obtained. A silicon on insulator (SOI) process is used for the described technique. For a standard CMOS technology parasitic effects due

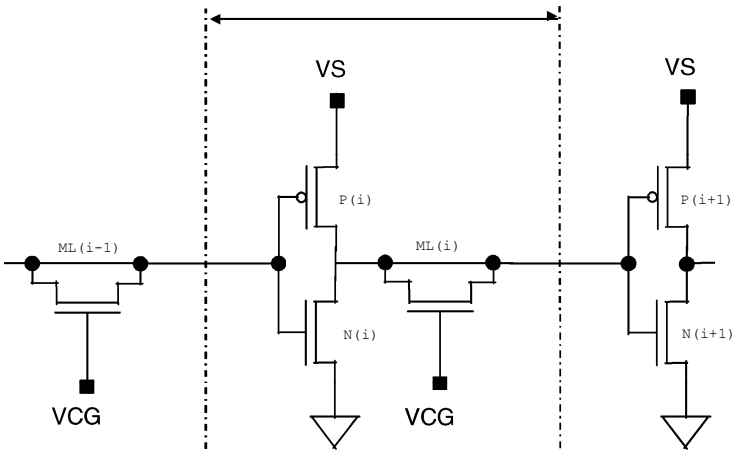


Figure 2.2: Schematic of one cell of a loaded ring oscillator as illustrated in [3]; $P_{(i)}$ and $N_{(i)} \cdots$ inverter transistors, $ML_{(i)} \cdots$ load transistor, $V_S \cdots$ supply voltage, $V_{CG} \cdots$ gate voltage of load transistor.

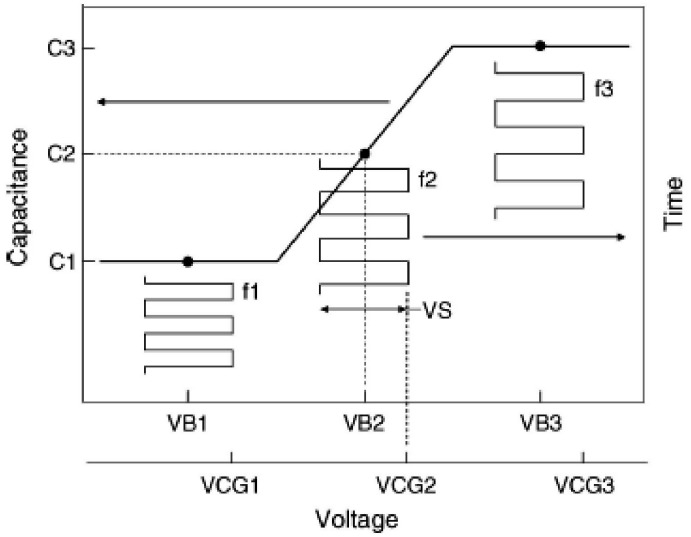


Figure 2.3: The load capacitance is measured for different gate voltages V_{CG} to obtain the above curve which is taken from [3]. The results C_1,C_2 and C_3 are values averaged over the voltage swing V_s at the drain and source. The average voltage is denoted as V_B.

to the interaction with bulk, i.e diffusion capacitances, channel to bulk capacitance and bulk to substrate capacitance, also need to be considered.

2.1.2 Capacitance Modeling in BSIM3v3

The FET model used in this project is the BSIM3v3 model [4]. A basic calculation of a MOSFET capacitance is given in equation (2.4). Bulk capacitances are not included in this equation. The gate to drain and gate to source potentials are the same for these considerations and thus the overlap capacitances for the respective regions. This is accounted for by the parameter **cgds** in equation (2.4). The quantity $C(W, L)$ represents the sum of the overlap capacitances and the oxide capacitance as function of width W and length L of the transistor, and is given by

$$\begin{aligned} C(W,L) = \mathbf{C_{ox}} \cdot \overbrace{(W - 2 \cdot \delta W)}^{W_{\text{eff}}} \cdot \overbrace{(L - 2 \cdot \delta L)}^{L_{\text{eff}}} \\ + \mathbf{cgbo} \cdot \overbrace{(L - 2 \cdot \delta L)}^{L_{\text{eff}}} + 2 \cdot \mathbf{cgds} \cdot \overbrace{(W - 2 \cdot \delta W)}^{W_{\text{eff}}} \end{aligned} \tag{2.4}$$

with the gate capacitance parameter $\mathbf{C_{ox}}$, gate to bulk overlap capacitance parameter **cgbo** and gate to drain/source overlap capacitance parameter **cgds**. L and W are the drawn length and width respectively. The parameter $\mathbf{C_{ox}}$ depends on the permittivity $\epsilon = \epsilon_{SiO_2} \cdot \epsilon_0$ and the thickness $\mathbf{T_{ox}}$ as in

$$\mathbf{C_{ox}} = \frac{\epsilon}{\mathbf{T_{ox}}}. \tag{2.5}$$

The effective channel length L_{eff} and width W_{eff} are calculated with equations (2.6) - (2.9) which are taken from the BSIM3v3 CV model [4]. Due to unideal effects during the fabrication process, the device's actual geometry deviates from the drawn values. Some of these effects are illustrated in figure 2.4. The effective length of the transistor is mostly determined by the lightly doped drain (LDD) and source implants. The transistor is entrenched by field oxide, which does not stop abruptly once it reaches the transistor's boundaries but grows to a certain amount into the device. The width is decreased by this effect called bird's beak. Furthermore, the gate does not grow perfectly flat and rectangular but varies in thickness and area. This influences all of the device's capacitances toward the gate.

$$\delta W = \mathbf{DWC} + \frac{\mathbf{Wl}}{L^{\mathbf{Wln}}} + \frac{\mathbf{Ww}}{W^{\mathbf{Wwn}}} + \frac{\mathbf{Wwl}}{L^{\mathbf{Wln}} \cdot W^{\mathbf{Wwn}}} \tag{2.6}$$

$$\delta L = \mathbf{DLC} + \frac{\mathbf{Ll}}{L^{\mathbf{Lln}}} + \frac{\mathbf{Lw}}{W^{\mathbf{Lwn}}} + \frac{\mathbf{Lwl}}{L^{\mathbf{Lln}} \cdot W^{\mathbf{Lwn}}} \tag{2.7}$$

$$L_{\text{eff}} = L - 2 \cdot \delta L \tag{2.8}$$

$$W_{\text{eff}} = W - 2 \cdot \delta W \tag{2.9}$$

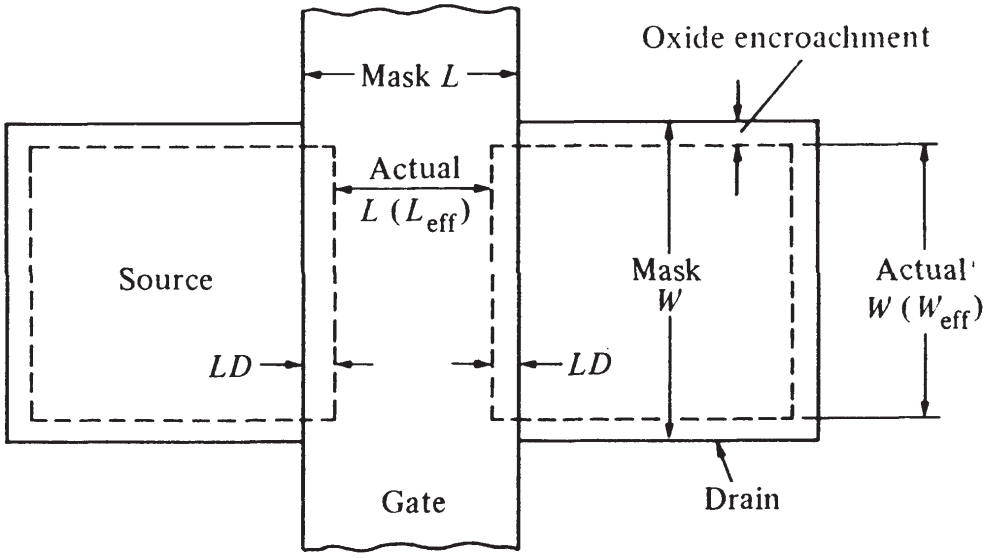


Figure 2.4: Active area of a FET transistor as illustrated in [5] . The drawn length is reduced by two times LD and the width by the oxide encroachment on both sides. LD corresponds to δL in equation (2.8).

Further attention needs to be paid to the parameter **cgds** from equation (2.4). The drain and source are connected to the same potential as stated above. Due to the symmetry MOSFET devices generally show, it therefore suffices to inspect only one side. Instead of keeping separate parameters for the gate to drain and gate to source overlap their influence is combined in the parameter **cgds**.
The overlap capacitances are calculated in the BSIM3v3 model according to the following equations [4]. **CGDO** and **CGDL** are the overlap capacitance parameters.

$$T0 = V_{gd} + \delta \quad (\delta = 0.02) \tag{2.10}$$

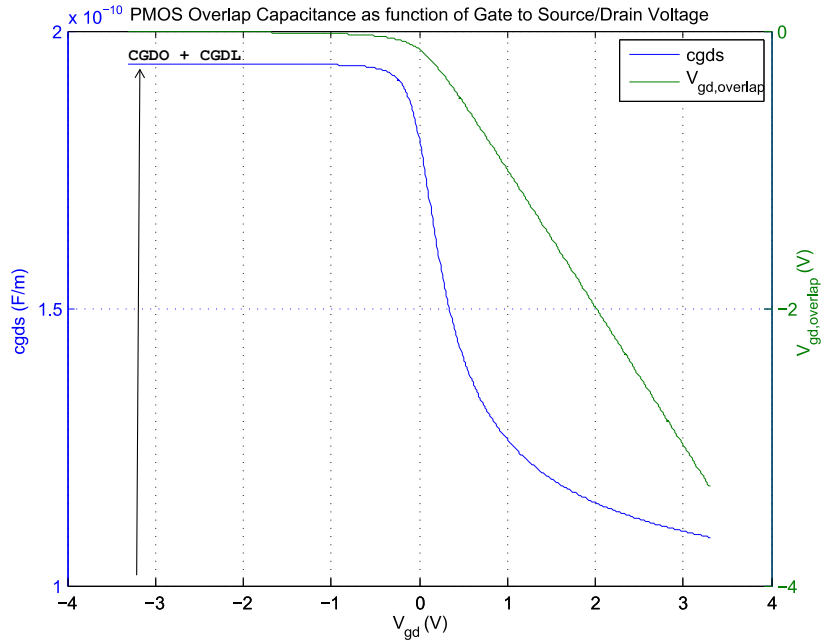
$$T1 = \sqrt{(T0 \cdot T0 + 4.0 \cdot \delta)} \tag{2.11}$$

$$T2 = 0.5 \cdot (T0 - T1) \tag{2.12}$$

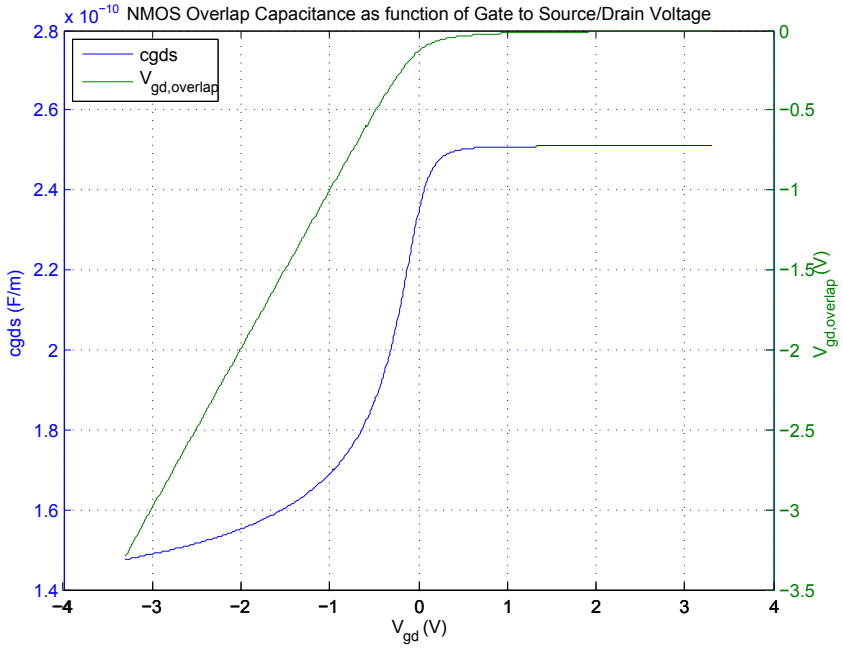
$$T3 = \sqrt{\left(1 - \frac{4 \cdot T2}{\mathbf{Ckappa}}\right)} \tag{2.13}$$

$$\mathbf{cgds} = \mathbf{CGDO} + \mathbf{CGDL} - \mathbf{CGDL} \cdot \left(1 - \frac{1}{T3}\right) \cdot \left(0.5 - \frac{0.5 \cdot T0}{T1}\right) \tag{2.14}$$

with the BSIM3v3 parameters **CGDO**, **CGDL**, **Ckappa** and δ. Plotting these equations as function of gate to drain voltage V_{gd} yields figure 2.5a for a PMOS device. The overlap capacitance is modeled as a function of gate to drain/source voltage (V_{gd}). For negative gate to drain voltages (positive for NMOS), the model parameter $V_{\mathrm{gd,overlap}} = T2$ (2.12) is approximately zero and constant. Also constant is the gate to drain overlap capacitance, which has a value of $\mathbf{CGDO} + \mathbf{CGDL}$. Figure 2.5b shows the result for a NMOS device.

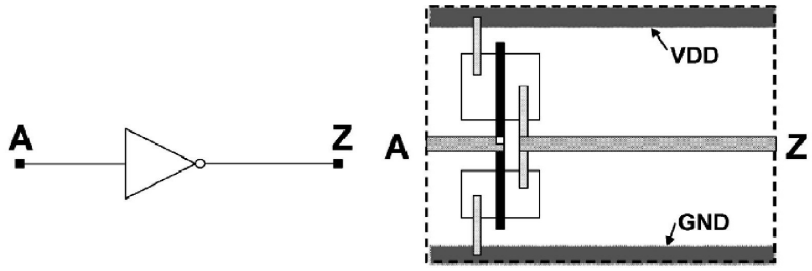


(a) PMOS gate to drain overlap capacitance parameter **cgds** and $V_{gd,overlap}$ as a function of V_{gd}. **CGDO** $= 8.6 \cdot 10^{-11} \frac{\mathrm{F}}{\mathrm{m}}$; **CGDL** $= 1.08 \cdot 10^{-10} \frac{\mathrm{F}}{\mathrm{m}}$; **Ckappa** $= 6 \cdot 10^{-01}$V.

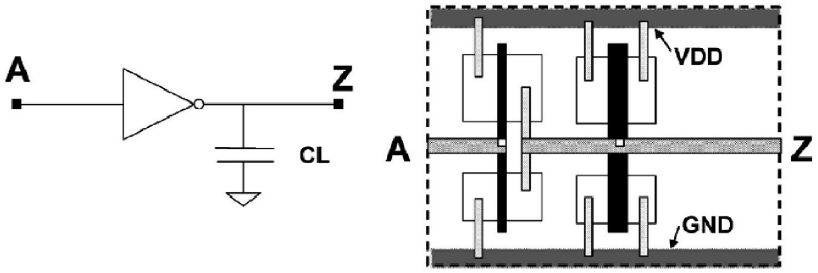


(b) NMOS gate to drain overlap capacitance parameter **cgds** and $V_{gd,overlap}$ as a function of V_{gd}. **CGDO** $= 1.2 \cdot 10^{-10} \frac{\mathrm{F}}{\mathrm{m}}$; **CGDL** $= 1.31 \cdot 10^{-10} \frac{\mathrm{F}}{\mathrm{m}}$; **Ckappa** $= 6 \cdot 10^{-01}$V.

Figure 2.5: Overlap voltage $\mathrm{V_{gd,overlap}}$ from equation (2.12) and overlap capacitance parameter **cgds** from (2.14) plotted as functions of gate drain voltage V_{gd}.



(a) Schematic layout of a reference inverter stage as shown in [1].



(b) Schematic layout of an inverter stage with a MOSFET load as shown in [1].

Figure 2.6: Schematic layout of inverter cells for loaded and reference oscillators.

The dependency on the gate voltage complicates the methods inspected so far enormously. Especially the technique for estimating L_{eff} is questionable, at least using the BSIM3v3 models. Since the overlap capacitances vary with the gate voltage, $(C_i - C_d)$ – the capacitance of the MOSFET in inversion minus the capacitance in depletion – does not only depend on the channel, which is an important assumption for extracting L_{eff}. Returning to the capacitance model from equation (2.4), it is essential to accurately determine its parameters to get a correct capacitance model. Theoretically, these could be extracted if the capacitance of the load is measured for different combinations of W and L. This is the focus of the next section and will therefore not be further elaborated here.

2.1.3 Layout Considerations

A crucial step for this measurement technique to be accurate is the layout of the circuit. The device currents in each inverter vary by a certain percentage due to mismatch which directly influences the delay per stage. Moreover, the extracted capacitance of the reference oscillator is subtracted from the capacitance of the loaded oscillator to correctly determine the load capacitance. In order to accomplish this, the inverter stages and parasitic elements in the unloaded oscillator need to be ideally identical with the respective devices in the loaded oscillator. Thus, the most important aspect of the layout is the best possible matching of the parasitic elements. With a good layout a frequency mismatch of smaller 1% is possible according to Bhushan *et al.* [3]. An example for the loaded and unloaded stage can be seen in figures 2.6a and 2.6b, where the only difference between the two stages is the transistor that makes up the load. Everything else is identical.

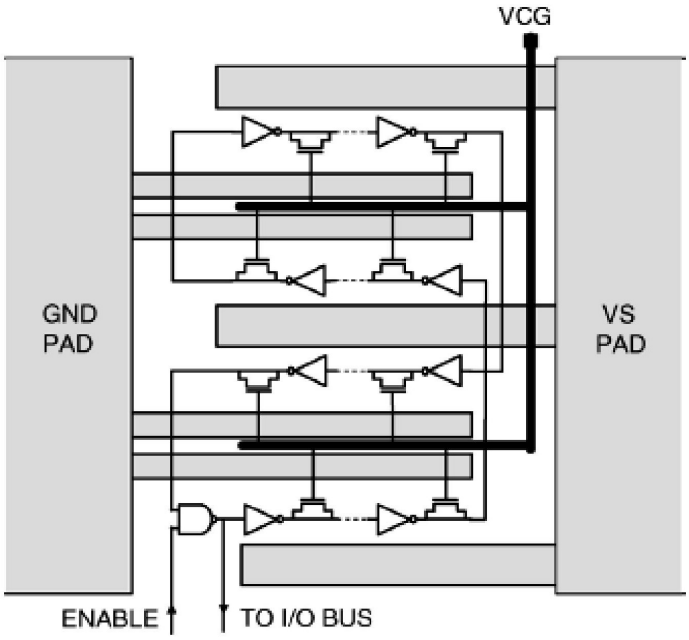


Figure 2.7: Basic layout of a ring oscillator for scribe line monitoring taken from [3].

Other considerations depend on the intended usage of the test structures. Ring oscillators designed for process monitoring should be preferably as small as possible in order to fit into a scribe line, for example as shown in figure 2.7. A layout using one metal layer only makes the test structures available as early as possible during fabrication [1].

Designs for parameter extraction each need their separate supply if absolute values are to be determined. Otherwise, the quiescent current will be the sum of $I_{DDQ}s$ of all the ring oscillators connected to the same supply. Oscillators which are put directly on a product circuit to monitor performance and aging are necessarily connected with the circuit's supply. Thus, only performance measurements are possible, for example the change in frequency over time [3]. These considerations regarding the supply are necessary when the quiescent current has a noticeable effect. For structures designed in a 0.35-μm

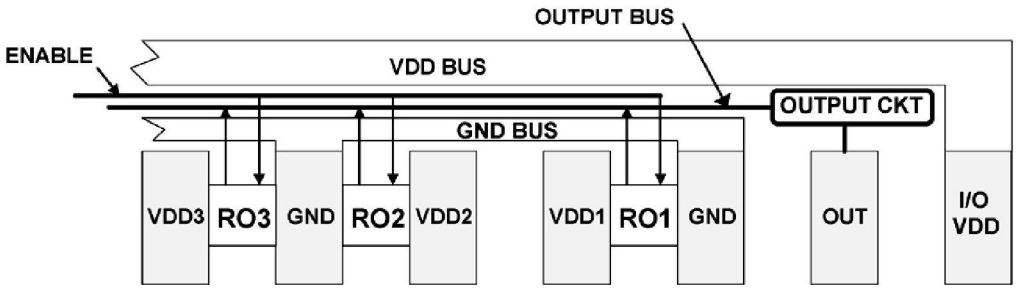


Figure 2.8: Schematic layout of individual ring oscillator designs illustrated in [1].

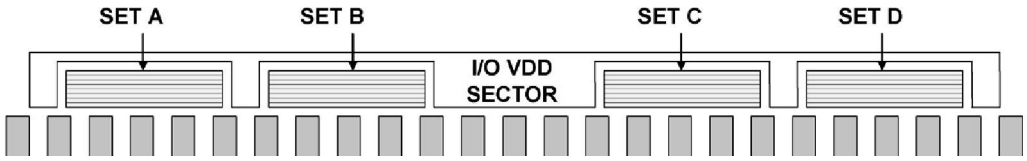


Figure 2.9: Schematic layout of macros containing several ring oscillators shown in [1].

technology, the quiescent current is orders of magnitudes smaller than the current drawn during oscillations and can therefore be neglected. Figures 2.8 and 2.9 present two different cases. In the first layout in figure 2.8 each ring oscillator has its own supply pad. The second example, on the other hand, requires much less space as a number of ring oscillators share one supply.

2.2 Parameter Extraction

The basic idea is to extract the parameters in equation (2.4) from frequency and current measurements of ring oscillators with different load dimensions. Those are specifically the oxide capacitance parameter $\mathbf{C_{ox}}$ which is inversely proportional to the oxide thickness $\mathbf{T_{ox}}$, the gate to drain/source overlap **cgds** and gate to bulk overlap **cgbo** capacitance parameters. Let us first look at the case with no corrections to the width and length (2.15) and without parasitics like diffusion capacitances and channel to bulk capacitance.

$$C = \mathbf{C_{ox}} \cdot W \cdot L + \mathbf{cgbo} \cdot L + 2 \cdot \mathbf{cgds} \cdot W \tag{2.15}$$

If for example the length of the load transistor is changed ($L_1 < L_2$), then the capacitance should change by

$$\Delta C = \underbrace{(\mathbf{C_{ox}} \cdot W + \mathbf{cgbo})}_{a_{\Delta L}} \cdot \underbrace{(L_2 - L_1)}_{\Delta L} \tag{2.16}$$

where $a_{\Delta L}$ is the rate of change with respect to the length of the load. Obviously, $a_{\Delta L}$ is a function of the width of the load transistor. Thus, its slope can be extracted by changing the width ($W_1 < W_2$).

$$\Delta a_{\Delta L} = \mathbf{C_{ox}} \cdot \underbrace{(W_2 - W_1)}_{\Delta W} \tag{2.17}$$

The slope $\mathbf{C_{ox}}$ of equation (2.17) corresponds to the oxide thickness $\mathbf{T_{ox}}$ as in $\mathbf{C_{ox}} = \frac{\epsilon_{SiO_2}}{\mathbf{T_{ox}}}$. Thus, for this ideal case, the oxide thickness can be measured with the following oscillators: RO_1 (W_1, L_1), RO_2 (W_1, L_2), RO_3 (W_2, L_1) and RO_4 (W_2, L_2). W_i and L_i are the width and length of the transistor load, the inverters themselves remain the same.

cgds can be extracted by calculating the regression line for equation (2.15) with respect to L and calculating the slope of the resulting offset $b_{\Delta L}$.

$$C = \underbrace{(\mathbf{C_{ox}} \cdot W + \mathbf{cgbo})}_{a_{\Delta L}} \cdot L + \underbrace{2 \cdot \mathbf{cgds} \cdot W}_{b_{\Delta L}} \tag{2.18}$$

The same procedure results in **cgbo** if it is first performed with respect to W and then L.

$$C = \underbrace{(\mathbf{C_{ox}} \cdot L + 2 \cdot \mathbf{cgds})}_{a_{\Delta W}} \cdot W + \underbrace{\mathbf{cgbo} \cdot L}_{b_{\Delta W}} \tag{2.19}$$

As only capacitance differences are processed there is no need for a reference oscillator, provided that the inverter stages introduce the same delay in every macro.

Applying this extraction method to equation (2.4), where the width and length corrections are included, yields the same result for the oxide thickness. **cgds** and **cgbo**, however, are not so easily determined anymore. The offsets $b_{\Delta L}$ and $b_{\Delta W}$ now become

$$b_{\Delta L} = 2 \cdot \mathbf{cgds} \cdot (W - 2 \cdot \delta W) - [\mathbf{C_{ox}} \cdot (W - 2 \cdot \delta W) + \mathbf{cgbo}] \cdot 2 \cdot \delta L \tag{2.20}$$

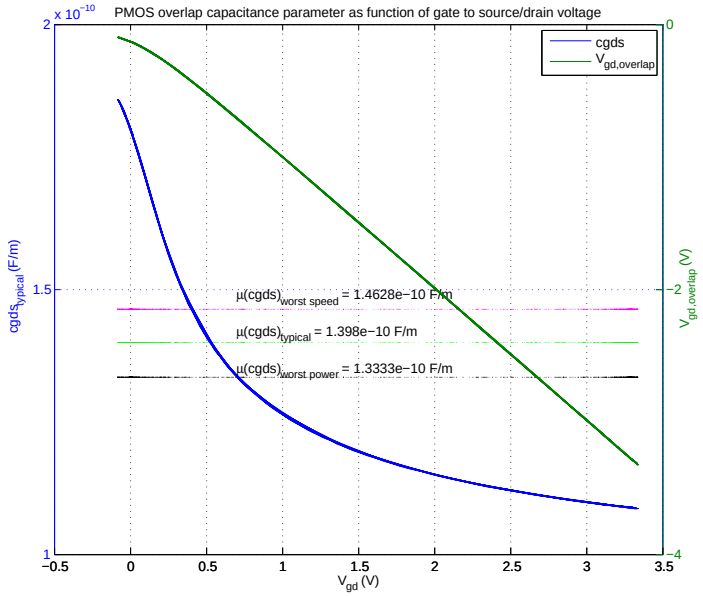
$$b_{\Delta W} = \mathbf{cgbo} \cdot (L - 2 \cdot \delta L) - [\mathbf{C_{ox}} \cdot (L - 2 \cdot \delta L) + 2 \cdot \mathbf{cgds}] \cdot 2 \cdot \delta W. \tag{2.21}$$

Without knowledge of δL and δW, **cgds** and **cgbo** cannot be extracted anymore. δL and δW could be taken from other measurements. However, this would also introduce additional uncertainties.
These considerations assume that all capacitances are active. As stated in section 2.1 only capacitances which are charged each period effectively influence the stage delay. Consequently, the gate to drain/source capacitance can be isolated by turning the load transistor off. If parasitic effects are still neglected, the total load capacitance is then simply given by

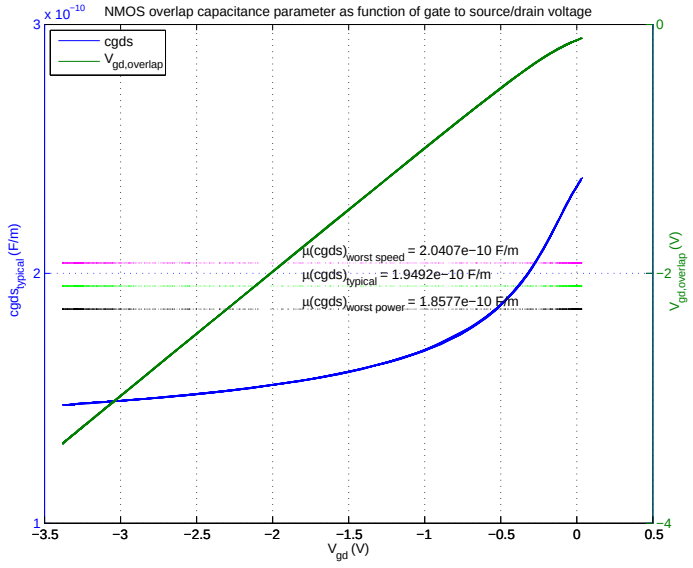
$$C = 2 \cdot \mathbf{cgds} \cdot (W - 2 \cdot \delta W). \tag{2.22}$$

Now two oscillators with load transistors of different widths suffice to extract **cgds**. As the overlap capacitance is modeled as a function of the gate to drain/source voltage, the measured value will represent an average over the range the voltage swings at those terminals. This is equal to the inverter supply voltage. The overlap capacitance parameter is constant only when the transistor is turned on and the source and drain regions are in accumulation. Figure 2.5a for instance shows the overlap parameter for a PMOS device. An estimate for this average value can be seen in figures 2.10a and 2.10b. It is obtained by calculating the capacitance parameter at each point of a simulated waveform and averaging over the resulting values.

The parasitics which have been neglected up to now are the drain and source to bulk capacitances, the channel to bulk capacitance and the bulk to substrate capacitance. The



(a) PMOS gate to drain overlap capacitance parameter $\mathbf{cgds}_{\text{typical}}$ and $V_{gd,overlap}$ as a function of V_{gd}. All values are calculated for simulated data points in the region from 0V to 3.3V. Also shown are the overlap capacitance parameters calculated with worst case conditions $\mathbf{cgds}_{\text{worst power}}$ and $\mathbf{cgds}_{\text{worst speed}}$.



(b) NMOS gate to drain overlap capacitance parameter $\mathbf{cgds}_{\text{typical}}$ and $V_{gd,overlap}$ as a function of V_{gd}. All values are calculated for simulated data points in the region from 0V to 3.3V. Also shown are the overlap capacitance parameters calculated with worst case conditions $\mathbf{cgds}_{\text{worst power}}$ and $\mathbf{cgds}_{\text{worst speed}}$.

Figure 2.10: Expected mean values for NMOS and PMOS overlap capacitance parameters

channel to bulk capacitance makes it impossible to derive the oxide thickness from the measurements described above. The reason is that in this case it is in parallel to the gate to channel capacitance once the device is turned on. Thus, its influence must be eliminated. This is achieved by shorting source, drain, and bulk. Now when the channel has formed the channel potential and bulk potential vary synchronously. Furthermore, the drain to bulk and source to bulk capacitances are also deactivated. The only parasitic capacitance remaining is the bulk to substrate capacitance. To eliminate it the bulk well is included in the reference oscillator. This will increase the size of the test structure considerably as a separate reference is now needed for each loaded oscillator. But otherwise the measurement extraction does not work for the investigated devices. The reference is now basically the same oscillator as the respective loaded oscillator without the load transistor gates.
Another drawback is that basic NMOS devices, which are placed directly in the substrate, cannot be used for the oxide thickness extraction. Moreover, the above considerations also do not work for a test structure to measure **cgds**. Equation (2.22) holds when the only capacitance active is the overlap capacitance. However, connecting the bulk to source and drain will also activate the bulk to gate capacitance. Thus, to measure the overlap capacitance the bulk is tied to a fixed potential and the transistor turned off. Then, comparing that to a reference that takes the source and drain to bulk capacitances into account, should make it possible to deduce the overlap capacitance. This works for both NMOS ans PMOS transistors. Consequently, different test structures are necessary to extract the oxide thickness and the overlap capacitance. In total that would be twelve oscillators – eight for the oxide thickness measurement and four for the measurement of **cgds**.

2.3 Ring Oscillator Circuit Design

2.3.1 Simulation Environment in Matlab

Given the nature of ring oscillators, creating a netlist mostly consists of copying the initial stage for as how many times as stages are desired. This type of work can be elegantly done by programming the structure in a loop, reducing the work from placing n stages to placing one stage. Matlab is an excellent tool for handling this type of work, which is why the bulk of the design process is done with the help of Matlab scripts. Furthermore, Matlab is a powerful tool for data analysis – both simulated and measured data – rendering the use of extraction and calculation methods possible that can be verified with simulated data.

The spectre simulator netlist is created with the help of Matlab scripts as stated above. Specifically, for the overlap capacitance characterization structure, these can be seen in the appendix in section A. The script *writeStage1OV.m* shown on page 81 creates the basic oscillator stage. It assembles a subcircuit consisting of the inverter and the load. These subcircuits are then assembled in the script *writeNet_ov_nand.m* (page 79). The task of writing the framework for the netlist is accomplished by *writehead.m* and *writeOptions_ov.m* which can be seen on pages 78 and 83. Although there are some differences between the loaded and reference ring oscillator, the basic structure of the netlist remains

the same. A complete netlist for a loaded ring oscillator can be seen in the appendix on page 86 following the mentioned scripts.
The oscillation period and average current consumption are calculated in *getdataoverlap.m* (page 89). To accomplish this, the indices where the amplitude is closest to $\frac{V_{DD}}{2}$ on every rising edge are saved. The period for each oscillation is calculated with these indices and the average taken. As the data points are not spaced equally around $\frac{V_{DD}}{2}$, a slight variation will result. Typically, the standard deviation is in the range of 0.1% and therefore $\frac{0.1\%}{\sqrt{n_p}}$ for the mean value, where n_p is the number of periods. The average current is calculated by numerically integrating the current over time using the trapezoidal rule and dividing by the total time.

2.3.2 Design of the Ring Oscillator Test Structures

With the simulation environment in place, the initial design was chosen to have 41 inverter stages. The reason for this choice was that a 41 stage oscillator has already been implemented for a standard 0.35-μm process. Although the inverter stages for the CV structures are smaller, the frequencies are not too far apart. Thus, the existing ring oscillator can be used to compare measurements done with the setup described in section 2.5 with monitored data in order to determine whether the setup is adequately accurate.

First Simulations with Ideal Capacitor Load

After having set up a design for the inverter stage, the next step was to verify the accuracy of the extraction method. First, an ideal capacitor is used as load for the inverter stages as illustrated in figure 2.11 to determine the accuracy of this extraction. The capacitance is calculated as

$$\begin{aligned} C_{cap} &= C_{ox} \cdot W \cdot L \\ C_{ox} &= \frac{\epsilon}{T_{ox}}. \end{aligned} \tag{2.23}$$

The capacitance is extracted from the data as described in equation (2.3) and the resulting values compared to the actual capacitance of equation (2.23). With the design in figure 2.11 the capacitance was simulated with 0.2% accuracy (simulated: $\mathbf{T_{ox}} = 7.736$nm; model value: $\mathbf{T_{ox}} = 7.754$nm). The simulation data can be seen in table 2.1.

Ring Oscillator with PMOS Load

Having reached an appropriate accuracy, the ideal capacitor was replaced with the PMOS load as shown in figure 2.12. The simplest model available in the design kit was first investigated, to ensure that the fundamental effects are understood before adding parasitic effects. The reason for choosing a PMOS device over a NMOS for the initial design is because the bulk of the NMOS cannot be shorted to source and drain as described in the previous section. The parameters of interest are $\mathbf{T_{ox}}$, **cgbo** and **cgds** from equation (2.4).

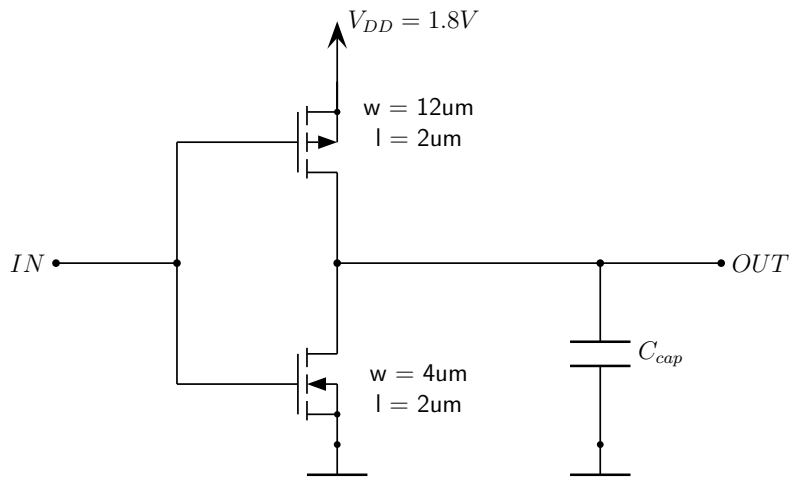


Figure 2.11: Ring oscillator stage with ideal capacitor as load. The complete ring oscillator consists of 41 of these stages.

Table 2.1: Simulation Data for ring oscillator with an ideal capacitor as load. I_{DDA}...average current consumption, f...oscillation frequency, w_{pl}, l_{pl}...width and length of load, T...oscillation period.

I_{DDA}	f	w_{pl}	l_{pl}	$\sigma(T)$	T
A	Hz	m	m	s	s
9.59071e-05	2.20225e06	1e-05	1e-05	1.7e-11	4.54080e-07
9.54438e-05	6.70461e05	1e-05	4e-05	3e-11	1.49151e-06
9.54438e-05	6.70461e05	4e-05	1e-05	3e-11	1.49151e-06
9.53120e-05	1.77277e05	4e-05	4e-05	1.9e-10	5.64088e-06

Several simulations with different geometries for the loads were performed until an adequate accuracy for the parameters was reached. It was found that the extraction process does not work very well with minimum size devices. Especially the structure to measure $\mathbf{T_{ox}}$ requires big devices, which disqualifies it as a monitoring structure. In order to reduce the size, the design is reduced to 23 stages instead of 41. The transistor dimensions used in the oscillator design can be seen in table 2.2a for the $\mathbf{T_{ox}}$ structure and in table 2.2b for the **cgds** structure. The **cgds** design pretty much has minimum size devices. The first layout was done with 41 stages, being just barely too big for a scribe line. Therefore, the number of stages for the **cgds** structure was reduced to 31 after the first test chip.

The first stage of each oscillator is made up of a NAND gate. With the NAND gate the oscillator can be enabled or disabled via a digital signal. An address circuitry is used to select each of the oscillators separately. It is a decoder made up of NOR gates that sets the targeted NAND gate high. Thereby, the respective circuit is put into its oscillating state. In case the selection input to the NAND gate is low, the ring oscillator is in a stable

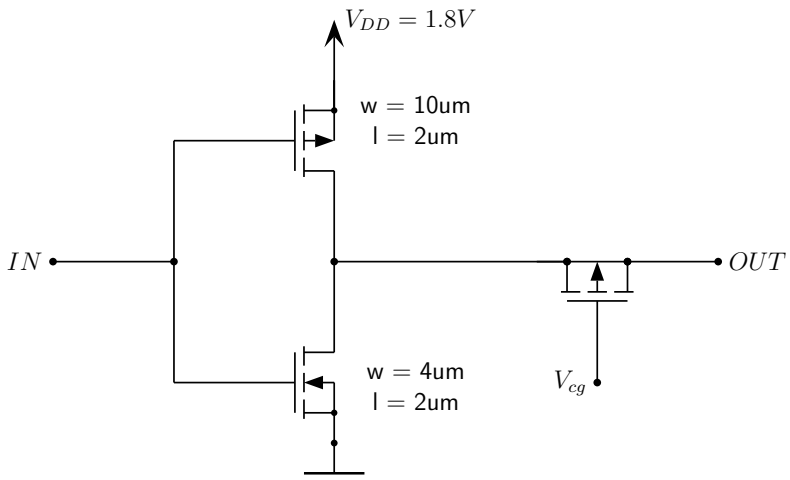


Figure 2.12: Single oscillator stage with a PMOS load. Source, bulk and drain are connected to OUT.

Table 2.2: Device dimensions for design 1 and 2.

(a) Dimensions of the final design for extraction of $\mathbf{T_{ox}}$. One oscillator has 23 stages. This design will be referenced as design 1.

RO structure	inverter length	inverter width (NMOS)	inverter width (PMOS)	load width	load length
	μm	μm	μm	μm	μm
1	2.0	4.0	10.0	10.0	1.0
2	2.0	4.0	10.0	10.0	3.0
3	2.0	4.0	10.0	20.0	1.0
4	2.0	4.0	10.0	20.0	3.0

(b) Dimensions of the final design for extraction of **cgds**. The oscillators on the first test chip have 41 stages, which are then reduced to 31 stages after that. This design will be referenced as design 2.

RO structure	inverter length	inverter width (NMOS)	inverter width (PMOS)	load width	load length
	μm	μm	μm	μm	μm
1	0.35	1.0	2.5	1.0	0.35
2	0.35	1.0	2.5	2.0	0.35

state with a constant high at its output. All of these gates are designed with minimum dimensions. An additional inverter stage of the same size as the oscillator's is used to decouple the signal from the oscillator. However, if this inverter runs on the same supply as the ring oscillator itself, then the total current will include the current required by that single inverter stage. This is undesired, as it is not part of the oscillator structure itself. In order to avoid this problem, the inverter stages after each oscillator are powered by the supply voltage of a currently deactivated oscillator.
After the inverters the signal passes through a Schmitt trigger, which is placed close to the logical gates of the multiplexer. Due to the long routing from the oscillators at the periphery the Schmitt trigger's input signal can be distorted. The Schmitt trigger has a fixed level at which it triggers and thus restores the edges of the signal without changing the frequency. Then all signals are multiplexed with NAND and NOR gates to the output. Only the oscillating signal will pass through. A large buffer is at the output to drive any capacitances that arise from the measurement devices. The size of each stage is increased in order to provide enough current for the next stage but not drastically increase the capacitance that the previous stage sees. Schematics of the designs can be seen in appendix A, figures A.1, A.2 and A.3.

2.3.3 Matching Analysis and Sensitivity Investigations

Matching Analysis

The accuracy with which the measurements can be expected to work is determined with the help of Monte Carlo mismatch simulations. To this end, the designs are simulated with around 200 Monte Carlo runs. The results are shown in figures 2.13 and 2.14. The supply voltage for design 1 is set at 1.8V to diminish the range over which the capacitance is averaged. The inverter supply voltage for design 2 had to be raised to higher values than in design 1, otherwise the results from the analysis are too inaccurate due to mismatch. With 1.8V an accuracy of μerror = 28% is reached for the mean value of design 2, compared to the μerror = 4.5% shown in figure 2.14.

The maximum errors that are given in the plots are calculated with nominal values from the simulation models. For the overlap capacitance parameter, the value averaged over the voltage range as pointed out in figures 2.10a and 2.10b is used as reference value. Especially the oxide capacitance measurement can be performed with high accuracy.

Sensitivity Analysis

In order to derive a mathematical model for an unknown function of which the results are known, the criterion to minimize the least square error is generally used. This means that the deviations of the results calculated with the model are minimized with respect to the actual outcomes. Those outcomes can be for example measurement results or simulation results. Different approaches exist to achieve this goal, for example non-linear fitting algorithms or also linear algorithms. The motivation for deriving such a model in this particular case is to investigate the parameters that have the most influence on the

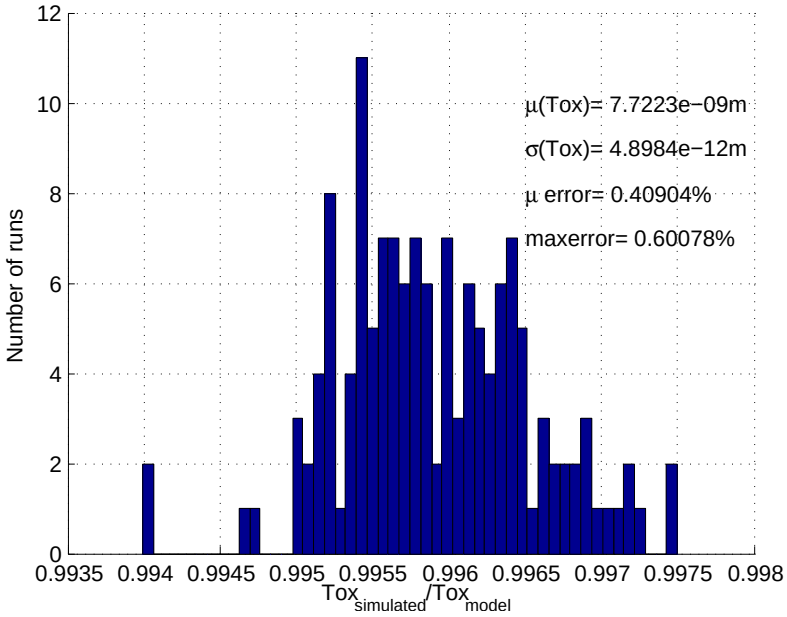


Figure 2.13: Matching simulation, result for oxide thickness $\mathbf{T_{ox}}$. Simulation design 1. The deviation of the average value from the model value is denoted as μ error. The maximal occurring deviation as maxerror. $V_S = 1.8V$.

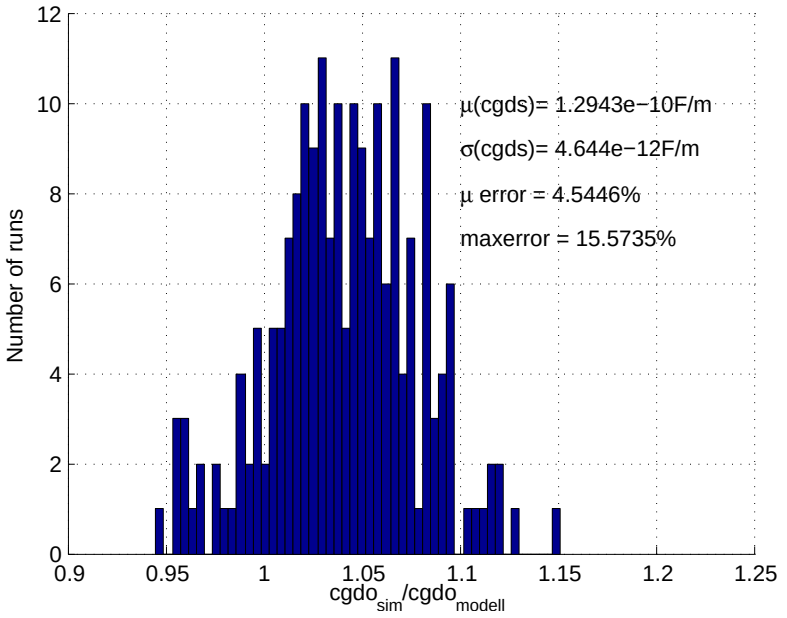


Figure 2.14: Matching simulation, result for overlap capacitance parameter **cgds**. Simulation design 2. The deviation of the average value from the model value is denoted as μ error. The maximal occurring deviation as maxerror. $V_S = 3.3V$.

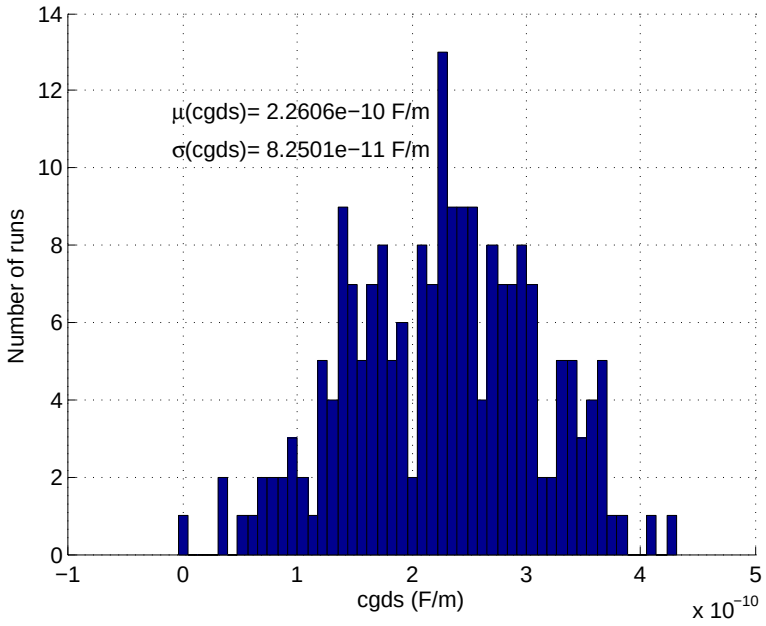


Figure 2.15: Distribution of the simulated overlap capacitance parameter **cgds** with process and mismatch variation for design 2 with a PMOS load. $V_S = 3.3V$.

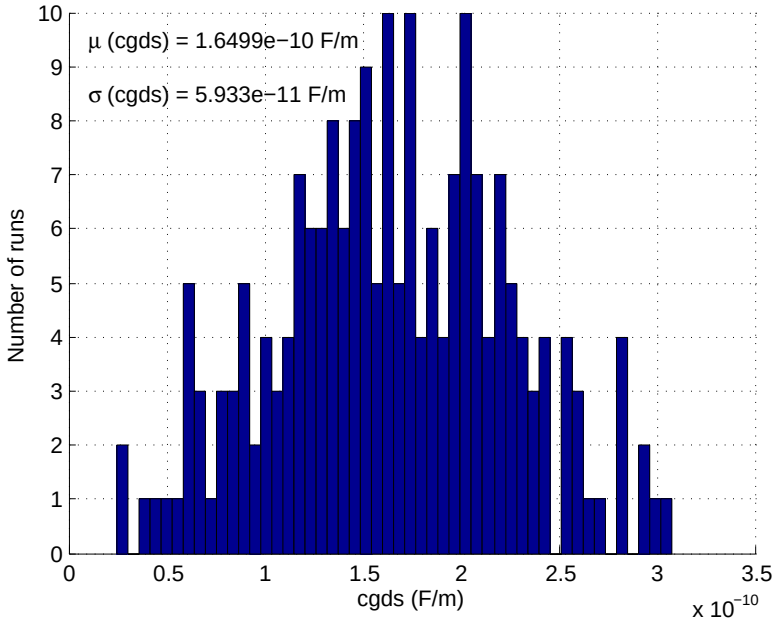


Figure 2.16: Distribution of the simulated overlap capacitance parameter **cgds** with process and mismatch variation for design 2 with a NMOS load. $V_S = 3.3V$.

outcome. That is to say that the goal is to find out whether the above introduced designs are especially sensitive toward the parameters that they are intended to measure, or if there are other influences that need to be considered. Therefore, a general least square fit approach is adapted to the problem at hand.
Using numerical techniques as described in [6], especially the methods found in chapter 15.4, a sensitivity analysis with regard to parameters that are varied during a Monte Carlo simulation can be performed. Spectre offers the option for a process Monte Carlo simulation to store each input parameter and its value in separate files. As this is done for each run, the complete parameter variation as it occurs during the simulation is available. The goal is to calculate the sensitivity of the oscillation period toward these parameters. It is hereby assumed that the simulation results for the oscillation period t have a linear dependency on the varied parameters.
The mathematical expression with which the period t is modeled as a function of the Monte Carlo parameters has the following form:

$$t(i) = t_0 + \sum_{j=1}^{M} \mathrm{a}_j \cdot \Delta p_j(i) \quad i = 1...N \tag{2.24}$$

where N is the number of Monte Carlo runs and M the number of varied parameters. The sensitivity of the period $t(i)$ with respect to parameter p_j is defined as a_j. t_0 is hereby the value that results when the parameters p_j take on their mean value, i.e. $\Delta p_j = 0$.With the mean values and the distribution around them, which are both gained from simulations, matrix $\mathbf{A}$ and vector $\mathbf{b}$ can be formed.

$$\begin{aligned} A_{ij} &= \frac{\Delta p_j(i)}{\sigma_i} \\ b_i &= \frac{t(i) - t_0}{\sigma_i} = \frac{\Delta t(i)}{\sigma_i} \end{aligned} \tag{2.25}$$

with σ_i being the standard deviations of the measurement error of the i^{th} data point. These can be set to the constant value $\sigma_i = 1$ if they are not known according to [6]. This will be done for the following equations. The solution to equation (2.24) can be found by minimizing the merit function χ^2, which is defined as

$$\chi^2 = \sum_{i=1}^{N} \left[\Delta t(i) - \sum_{j=1}^{M} \mathrm{a}_j \cdot \Delta p_j(i) \right]^2 . \tag{2.26}$$

The minimum occurs for a set of parameters $\mathbf{a}$ for which the derivative of χ^2 with respect to the parameters a_j vanishes.

$$0 = \sum_{i=1}^{N} \left[\Delta t(i) - \sum_{k=1}^{M} \mathrm{a}_k \cdot \Delta p_k(i) \right] \cdot \Delta p_j(i) \quad \text{for } j = 1...M \tag{2.27}$$

Using matrix **A** and vector **b** the calculations are:

$$\begin{aligned} [\alpha] &= \mathbf{A}^T \cdot \mathbf{A} \\ [\beta] &= \mathbf{A}^T \cdot \mathbf{b} \\ \mathbf{a} &= [\alpha]^{-1} \cdot [\beta]\,. \end{aligned} \tag{2.28}$$

Inverting singular or badly conditioned matrices can be problematic. Therefore it is suggested in [6] to use singular value decomposition to solve the problem. The Matlab function *svd(**A**)* computes three matrices **U**, **S** and **V**, that return the matrix **A** when multiplied.

$$\mathbf{A} = \mathbf{U} \cdot \mathbf{S} \cdot \mathbf{V'} \tag{2.29}$$

U and **V** are unitary matrices and **S** has a diagonal structure. Solving equations (2.28) yields

$$\mathbf{a} = \sum_{i=1}^{M} \frac{\mathbf{U}_i \cdot \mathbf{b}}{w_i} \cdot \mathbf{V}_i \tag{2.30}$$

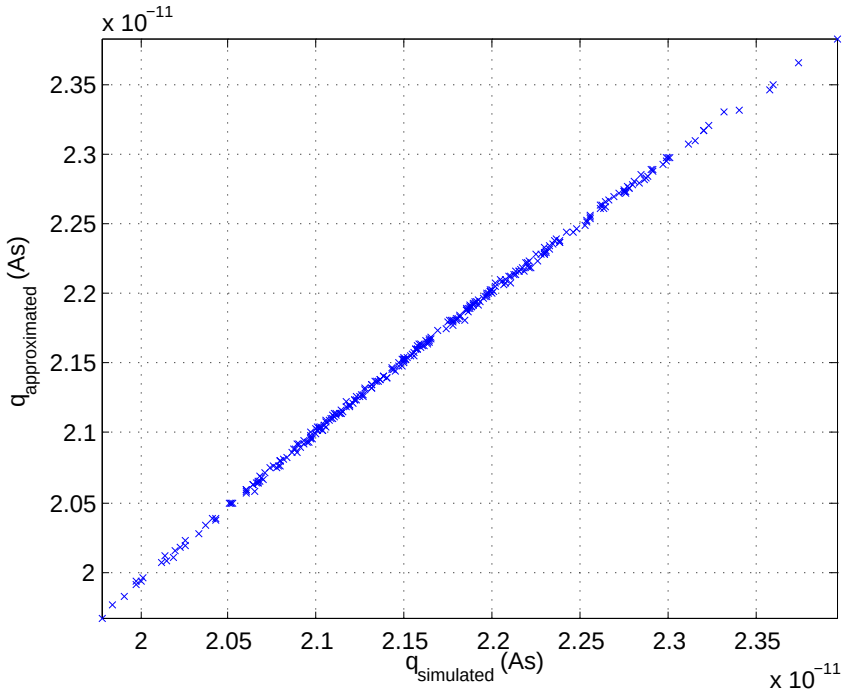
with w_i being the diagonal elements of **S**. In case a w_i is zero, the reciprocal value is set to zero, thereby eliminating the discontinuity.
In order to get a better feeling for the impact that different parameters have, a relative sensitivity is defined as

$$\frac{\Delta t(i)}{\bar{t}} = \sum_{j=1}^{M} \left(\mathrm{a}_j \cdot \frac{\bar{p_j}}{\bar{t}} \right) \cdot \frac{\Delta p_j(i)}{\bar{p_j}} \tag{2.31}$$

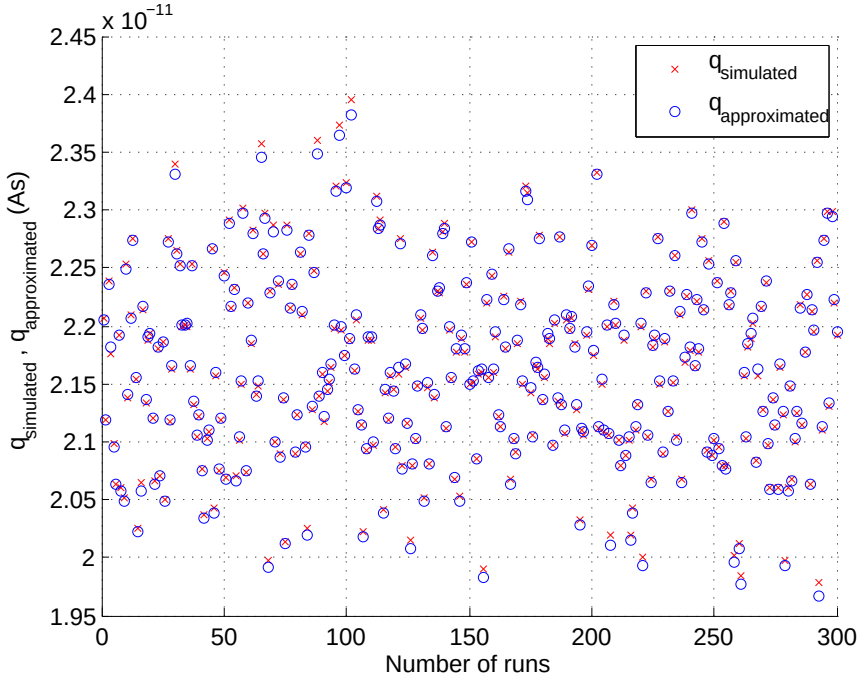
where $\mathrm{a}_j \cdot \frac{\bar{p_j}}{\bar{t}}$ is the relative sensitivity. $\bar{p_j}$ is hereby the average value of one parameter across the range of Monte Carlo runs and $\bar{t}$ the average value of the fitted result.

The following table 2.3 gives the parameters that are varied for the Monte Carlo process simulation. In addition to the parameters below, four other parameters are also varied, i.e. npeak1, npeak5, drdiffn and drdiffp, which vary the channel doping concentration and the source/drain diffusion sheet resistance of the NMOS and PMOS devices. These are not included in the least squares fit as they tend to worsen the fit.

Applying this method to the current I and the oscillation period t yields the results shown in figures 2.17, 2.18 and 2.19, and tables 2.4, 2.5 and 2.6. The simulations are performed for three different structures: first with an unloaded ring oscillator, then with design 1 oscillator structures which extract the oxide thickness, and finally with design 2 oscillators used to extract the overlap capacitance.
The sensitivity analysis is performed for the oxide thickness $\mathbf{T_{ox}}$, the gate to drain and gate to source overlap capacitance, and the product of the mean current times the oscillation period of the unloaded ring oscillator.

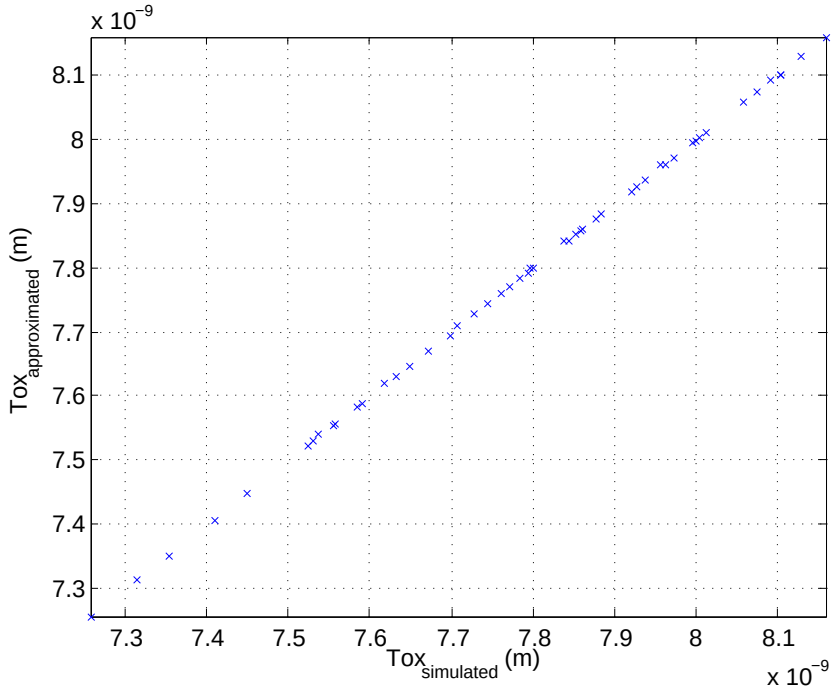


(a) Least squares approximation applied to an unloaded oscillator. Plotted are the charges $q = I \cdot t$ calculated with the approximation against the simulated charge values ($q_{\text{simulated}}$ vs $q_{\text{approximated}}$).

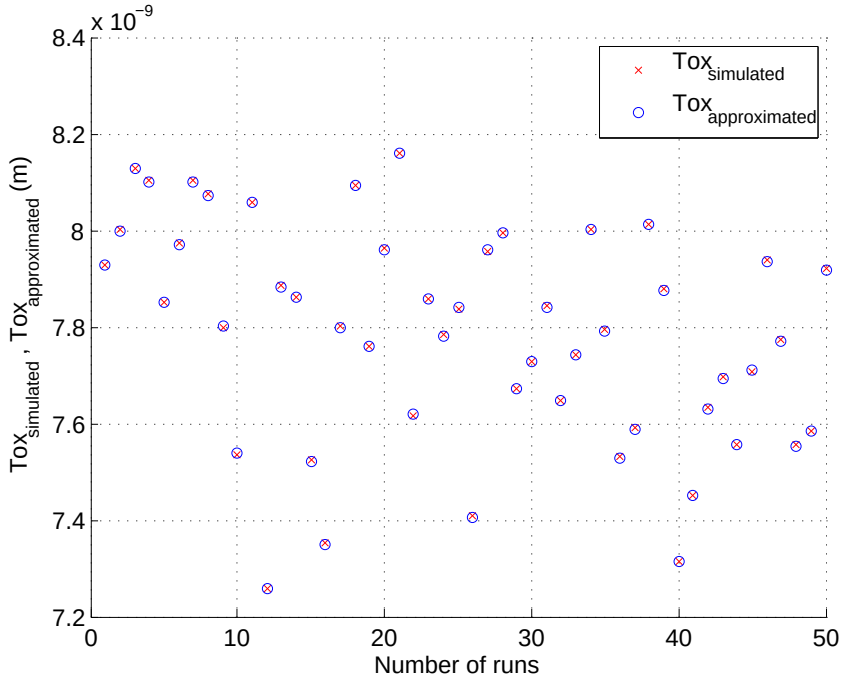


(b) Least squares approximation applied to an unloaded oscillator. Plotted are the simulated and approximated charge values for each Monte Carlo run.

Figure 2.17: Plots of the least squares approximation for an unloaded oscillator.

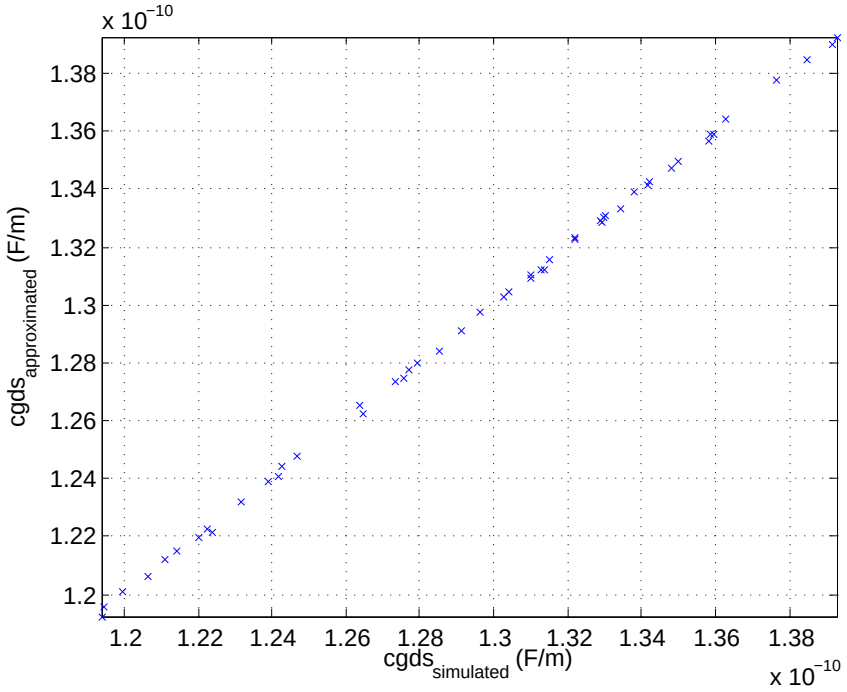


(a) Least squares approximation applied to design 1. Plotted are the oxide thickness values calculated with the approximation against the simulated values.

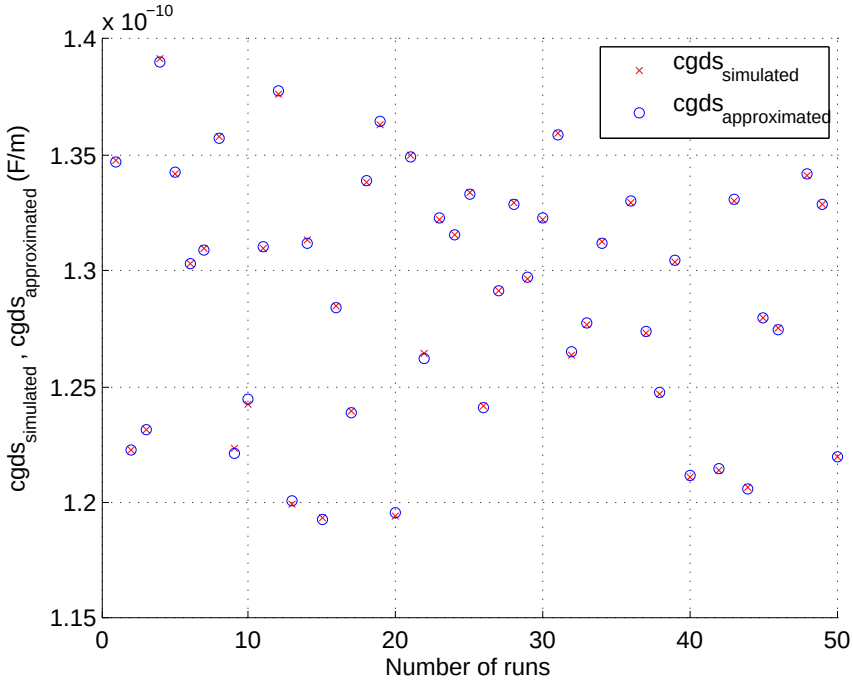


(b) Least squares approximation applied to design 1. Plotted are the approximated parameter values for $\mathbf{T_{ox}}$ and the simulated values for each Monte Carlo run.

Figure 2.18: Plots of the least squares approximation for design 1.



(a) Least squares approximation applied to design 2. Plotted are the overlap capacitance parameters **cgds** calculated with the approximation against the actually simulated parameter values.



(b) Least squares approximation applied to design 2. Plotted are the approximated overlap parameter values and the simulated values for each Monte Carlo run.

Figure 2.19: Plots of the least squares approximation for design 2.

Table 2.3: Model parameters which are varied for a Monte Carlo process simulation.

Input parameters to the least square fit	Dimension	Model parameters influenced by these variations
Δcgsdop	$\frac{F}{m}$	PMOS model parameter for the gate to drain and gate to source overlap capacitance
Δcgbop	$\frac{F}{m}$	PMOS model parameter for the gate to bulk overlap capacitance
Δcj5	$\frac{F}{m^2}$	p diffusion area capacitance parameter
Δcjsw5	$\frac{F}{m}$	p diffusion perimeter capacitance parameter
Δdeluop	$\frac{m^2}{Vs}$	PMOS mobility parameter
Δdelvtop	V	PMOS threshold parameter
Δcgsdon	$\frac{F}{m}$	NMOS gate to drain and gate to source overlap parameter
Δcgbon	$\frac{F}{m}$	NMOS gate to bulk overlap parameter
Δcj1	$\frac{F}{m^2}$	n diffusion area capacitance parameter
Δcjsw1	$\frac{F}{m}$	n diffusion perimeter capacitance parameter
Δdeluon	$\frac{m^2}{Vs}$	NMOS mobility parameter
Δdelvton	V	NMOS threshold parameter
Δdeltox	m	Oxide thickness parameter
Δdell	m	length offset parameter
Δdelw	m	width offset parameter

As the results show, sensitivities are found which closely fit the set of varied model parameters to the actual change of the simulation outcome. Therefore, the assumptions regarding the linear dependency on the model parameters (2.24) hold.
Closer inspection of the resulting parameter sets **a** given in tables 2.5 and 2.6 for the oxide thickness and overlap capacitance extraction further confirms the validity of the designs. The extracted oxide thickness is very sensitive toward changes of the oxide thickness parameter Δdeltox, which is as expected. The overlap capacitance is very sensitive toward changes of the overlap capacitance parameter for the PMOS. As the load is a PMOS device, this is also straightforward. The sensitivity in this case is not 100% as it is for the oxide thickness, however. The reason for this is that the overlap capacitance depends on two parameters **CGDO** and **CGDL**. Here only **CGDO** is varied. Thus, increasing **CGDO** by for example one hundred percent does not mean that the overall overlap capacitance increases by the same amount, but only by 69%.
Moreover, these results also show that the extraction method works as intended: by comparing the loaded with the unloaded ring oscillators the desired parameters can be isolated and extracted almost regardless of how other parameters vary, as long as the variation occurs for the unloaded and loaded structures equally. Thus, by placing them close together, the influence of process variation on the parameter of interest can be investigated.

Table 2.4: Sensitivities a_j resulting from the least square fit for the product $I \cdot t$ of the unloaded oscillator.

Varied parameters	Sensitivities a_j	Relative Sensitivities
Δcgsdop	$6.5199 \cdot 10^{-03}$ Vm	2.6%
Δcgbop	$6.2986 \cdot 10^{-04}$ Vm	0.32%
Δcj5	$7.7978 \cdot 10^{-10}$ Vm^2	4.9%
Δcjsw5	$1.3311 \cdot 10^{-03}$ Vm	1.9%
Δdeluop	$-1.3394 \cdot 10^{-15}$ $\frac{\mathrm{VAs}^2}{\mathrm{m}^2}$	−1.1%
Δdelvtop	$4.3942 \cdot 10^{-12}$ $\frac{\mathrm{As}}{\mathrm{V}}$	−15%
Δcgsdon	$2.2048 \cdot 10^{-03}$ Vm	1.2%
Δcgbon	$-2.5874 \cdot 10^{-04}$ Vm	−0.13%
Δcj1	$2.4879 \cdot 10^{-10}$ Vm^2	1.1%
Δcjsw1	$6.3936 \cdot 10^{-04}$ Vm	0.73%
Δdeluon	$4.2196 \cdot 10^{-16}$ $\frac{\mathrm{VAs}^2}{\mathrm{m}^2}$	0.93%
Δdelvton	$-3.0202 \cdot 10^{-12}$ $\frac{\mathrm{As}}{\mathrm{V}}$	−7.0%
Δdeltox	$-2.3936 \cdot 10^{-03}$ $\frac{\mathrm{As}}{\mathrm{m}}$	−86%
Δdell	$9.3334 \cdot 10^{-06}$ $\frac{\mathrm{As}}{\mathrm{m}}$	−0.061%
Δdelw	$2.9886 \cdot 10^{-06}$ $\frac{\mathrm{As}}{\mathrm{m}}$	0.051%

Table 2.5: Sensitivities a_j resulting from the least square fit for the oxide thickness $\mathbf{T_{ox}}$. (Design 1)

Varied parameters	Sensitivities a_j	Relative Sensitivities
Δcgsdop	$1.1984 \cdot 10^{-01}$ $\frac{\mathrm{m}^2}{\mathrm{F}}$	0.13%
Δcgbop	$-6.1771 \cdot 10^{-02}$ $\frac{\mathrm{m}^2}{\mathrm{F}}$	−0.087%
Δcj5	$-5.6545 \cdot 10^{-09}$ $\frac{\mathrm{m}^3}{\mathrm{F}}$	−0.099%
Δcjsw5	$1.7208 \cdot 10^{-03}$ $\frac{\mathrm{m}^2}{\mathrm{F}}$	0.0072%
Δdeluop	$1.5917 \cdot 10^{-13}$ $\frac{\mathrm{Vs}}{\mathrm{m}}$	0.35%
Δdelvtop	$-1.1292 \cdot 10^{-10}$ $\frac{\mathrm{m}}{\mathrm{V}}$	1.1%
Δcgsdon	$-1.1109 \cdot 10^{-02}$ $\frac{\mathrm{m}^2}{\mathrm{F}}$	−0.017%
Δcgbon	$-1.8973 \cdot 10^{-02}$ $\frac{\mathrm{m}^2}{\mathrm{F}}$	−0.027%
Δcj1	$-7.4415 \cdot 10^{-09}$ $\frac{\mathrm{m}^3}{\mathrm{F}}$	−0.089%
Δcjsw1	$1.5314 \cdot 10^{-02}$ $\frac{\mathrm{m}^2}{\mathrm{F}}$	0.049%
Δdeluon	$4.9362 \cdot 10^{-14}$ $\frac{\mathrm{Vs}}{\mathrm{m}}$	0.30%
Δdelvton	$1.3647 \cdot 10^{-10}$ $\frac{\mathrm{m}}{\mathrm{V}}$	0.88%
Δdeltox	$9.9696 \cdot 10^{-01}$	100%
Δdell	$-2.6148 \cdot 10^{-05}$	0.0012%
Δdelw	$8.5151 \cdot 10^{-06}$	−0.00042%

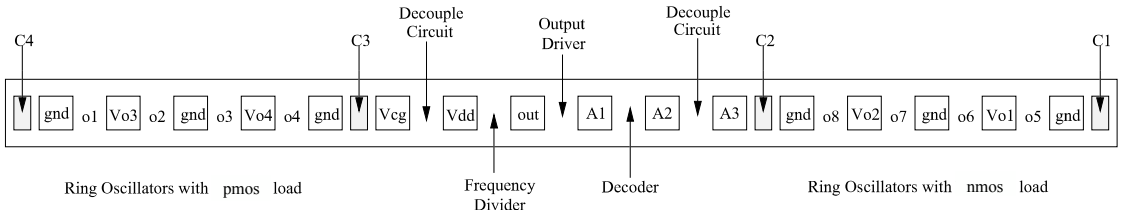
Table 2.6: Sensitivities a_j resulting from the least square fit for the overlap capacitance parameter **cgds**. (Design 2)

Varied parameters	Sensitivities a_j	Relative Sensitivities
Δcgsdop	1.0394	69%
Δcgbop	$-4.1097 \cdot 10^{-04}$	-0.035%
Δcj5	$-1.1349 \cdot 10^{-10}$ m	-0.12%
Δcjsw5	$8.6542 \cdot 10^{-05}$	0.021%
Δdeluop	$6.8595 \cdot 10^{-15}$ $\frac{\mathrm{As}^2}{\mathrm{m}^3}$	0.91%
Δdelvtop	$1.1238 \cdot 10^{-11}$ $\frac{\mathrm{As}}{\mathrm{V}^2\mathrm{m}}$	-6.4%
Δcgsdon	$1.6834 \cdot 10^{-03}$	0.16%
Δcgbon	$-4.1434 \cdot 10^{-04}$	-0.035%
Δcj1	$4.7497 \cdot 10^{-10}$ m	0.34%
Δcjsw1	$-1.8866 \cdot 10^{-03}$	-0.37%
Δdeluon	$4.3887 \cdot 10^{-15}$ $\frac{\mathrm{As}^2}{\mathrm{m}^3}$	1.62%
Δdelvton	$-8.5186 \cdot 10^{-12}$ $\frac{\mathrm{As}}{\mathrm{V}^2\mathrm{m}}$	-3.3%
Δdeltox	$1.5181 \cdot 10^{-05}$ $\frac{\mathrm{As}}{\mathrm{Vm}^2}$	0.092%
Δdell	$-8.4107 \cdot 10^{-06}$ $\frac{\mathrm{As}}{\mathrm{Vm}^2}$	-0.017%
Δdelw	$1.5028 \cdot 10^{-06}$ $\frac{\mathrm{As}}{\mathrm{Vm}^2}$	-0.0091%

The biggest impact on the frequency of the unloaded ring oscillator show the threshold voltage variation Δdelvtop of the PMOS and the oxide thickness. The oxide thickness affects the biggest capacitances in the structure, and therefore is the most influential. Other parameters that directly affect the capacitances also show a relatively big influence on the simulation outcomes.

2.4 Ring Oscillator Circuit Layout

As stated before in section 2.1.3 the frequency of the oscillator is very sensitive to its layout. Two different designs have been presented in the previous section, the first one to determine the oxide thickness and the second one to determine the overlap capacitance. If the different parts of the characterization structures do not match, it will not be possible to measure the desired properties. There are two different aspects that need to be considered here. First, the stages of a single oscillator should be ideally identical to each other with the same length of routing and surrounding. Second, not only should the inverters be the same in the loaded and reference oscillator, but also all parasitics that are introduced through the routing and diffusions. Basically the reference is then the same circuit as its respective loaded oscillator without the load transistors' gates. A correct layout can achieve a frequency mismatch of smaller than one percent, as described in section 2.1.3. As the layout of the overlap characterization design, which has been introduced as design 2, was completed earlier than design 1, the first test chip is made up of structures from



(a) Schematic layout of test chip 1 to monitor the NMOS and PMOS overlap capacitance parameters. The oscillator structures are placed between their respective supply pads. The test structures are from design 2.

(b) Pin description for the first test chip

PAD	Description
gnd	Ground connection; the separate pads are not connected on the chip itself
V_{o1}	Supply pad for oscillators o5 and o6
V_{o2}	Supply pad for oscillators o7 and o8
V_{o3}	Supply pad for oscillators o1 and o2
V_{o4}	Supply pad for oscillators o3 and o4
V_{CG}	Connection to the gates of the load transistors
V_{DD}	Supply pad for address and output circuit
out	Output pad at which frequency can be measured
A1	Address pad, msb
A2	Address pad
A3	Address pad, lsb

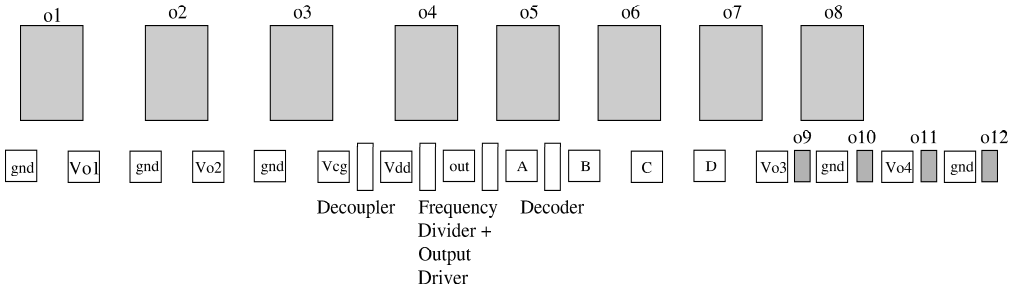
Figure 2.20: Schematic layout and pin description of test chip 1.

design 2. The second test chip comprises design 1 and a revision of design 2.

2.4.1 Schematic Layout

Almost minimum size devices are used for the characterization design 2. It is therefore possible to place it in a standard scribe line. The schematic layout for this SLM test structure can be seen in figure 2.20a and a description of the pins is given in table 2.20b. Oscillators one to four are intended to measure the PMOS overlap capacitance parameter; the other four oscillators to measure the NMOS overlap capacitance parameter. A separate supply pad is given for each ring oscillator and its reference oscillator. Thus, the ring oscillators are not powered by the same supply as the digital components, which could otherwise introduce jitter in the frequency. Furthermore, this is a straightforward way to measure the mean current that the ring oscillator consumes. The quiescent current of the disabled oscillator is assumed to be negligible as discussed before.

Design 1 is bigger and therefore not suitable for SLM structures. Yet, using a different pad arrangement than in a SLM would require a different measurement setup for the second



(a) Schematic layout of test chip 2. The oxide thickness characterization structure design 1 is arranged around a standard scribe line. As there is still some empty space an improved version of design 2 with 31 stages is also implemented.

(b) Pin description for the second test chip

PAD	Description
gnd	Ground connection; the separate pads are not connected on the chip itself
V_{o1}	Supply pad for oscillators o1, o2 and o9
V_{o2}	Supply pad for oscillators o3, o4 and o10
V_{o3}	Supply pad for oscillators o5, o6 and o11
V_{o4}	Supply pad for oscillators o7, o8 and o12
V_{CG}	Connection to the gates of the load transistors
V_{DD}	Supply pad for address and output circuit
out	Output pad at which frequency can be measured
A	Address pad, msb
B	Address pad
C	Address pad
D	Address pad, lsb

Figure 2.21: Schematic layout and pin description of test chip 2.

test chip compared to the first. Thus, the scribe line is taken as a centerpiece for the second test chip, around which the other oscillators are arranged as illustrated in figure 2.21a. Some of the extra space available in between the probe pads is used to place some test structures from the first test chip, to be specific the overlap characterization structures for PMOS transistors. For this second test chip the number of stages for this structure are reduced to 31 as stated in section 2.3.2. A description of the pins is given in table 2.21b.

2.4.2 Layout

Pictures of the actual layout will be presented in this section. The general layout of the overlap test structure can be seen in figure 2.23a. The components are placed as shown in the schematic layout in figure 2.20a. As it turns out, the forty-one stage design is just slightly too big to fit into a standard scribe line with routing above and below. The dimensions of a standard scribe line are 80 μm by 2000 μm and the space needed for the

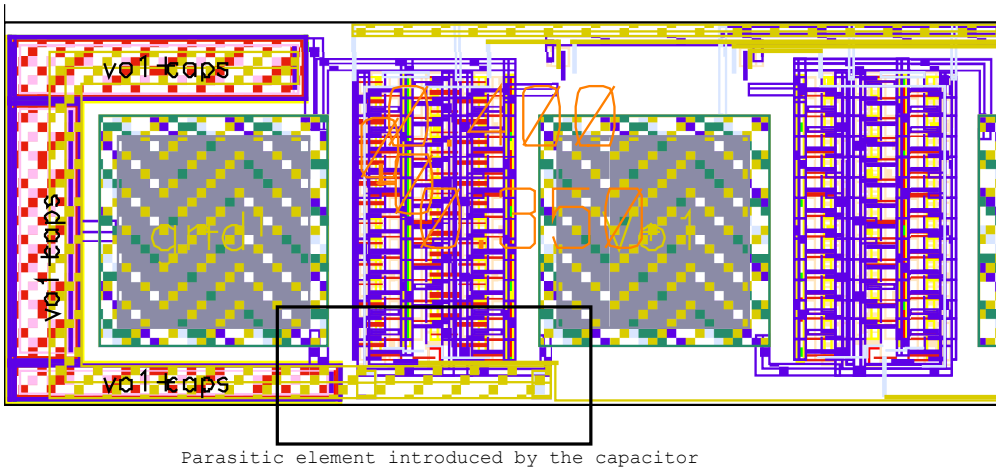
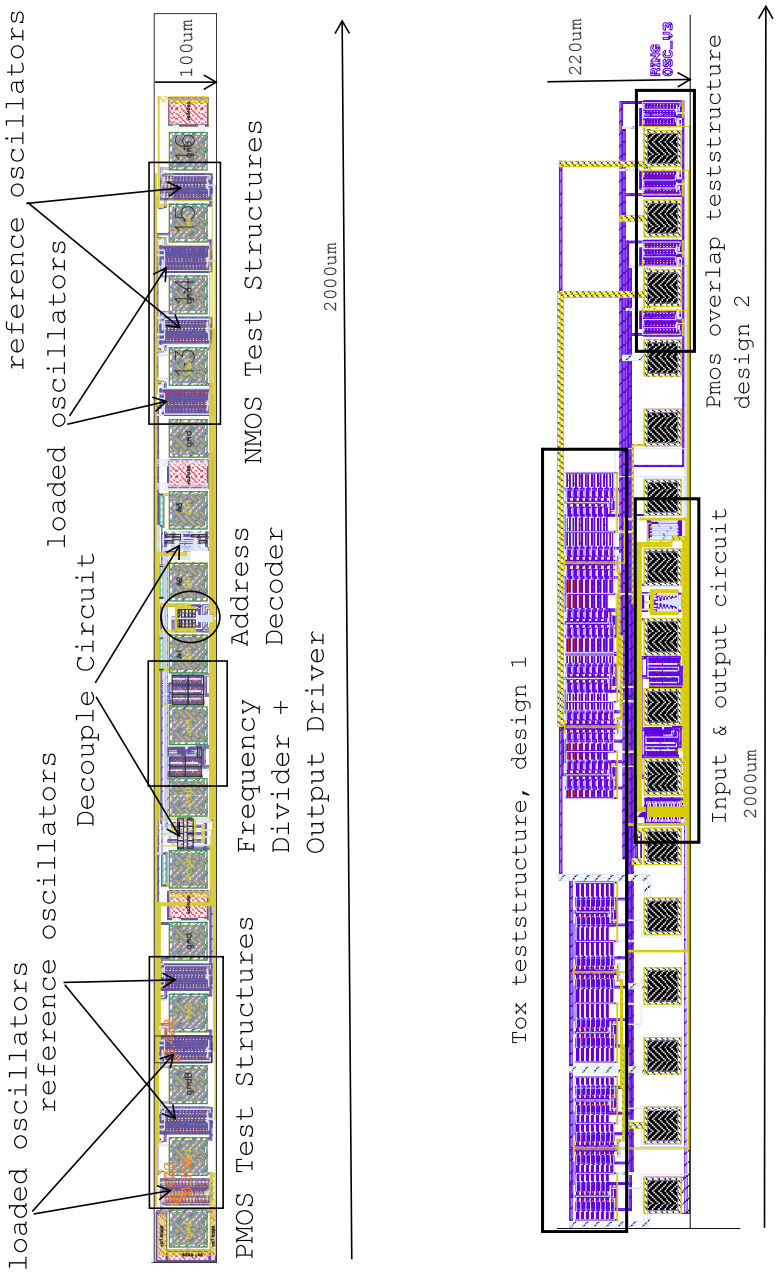


Figure 2.22: The space at the end of the scribe line is not enough to place the capacitor. Fitting it around the pad introduces an additional asymmetry between the loaded and the reference oscillator.

forty-one stage design is 100 μm by 2000 μm. In this case, where a special test chip is being built, this poses no problem as there are no space requirements. However, the oscillator designs need to be reduced to 31 stages if these structures are used for monitoring the overlap capacitance. This is done for the design placed on the second test chip.

Capacitors C1 to C4 from figure 2.20a were intended to buffer the oscillator's supply voltage. Yet, with a capacitance of only a couple of picofarad they are not really suited for this task and therefore are not placed on the second test chip. Besides, placing the capacitors disrupts the symmetry of the PMOS overlap test design. The space available on the one end of the scribe line is much less than that on the other because the pads are not centered in the scribe line. To fit the capacitor into that space it needs to be placed around the first connection pad. Part of the structures then overlap with the first ring oscillator of the PMOS design, which will introduce parasitic elements that are not present in the other oscillators. This problem is shown in figure 2.22. Alternatively external buffer capacitors could be placed directly on the probe card if the need should arise.

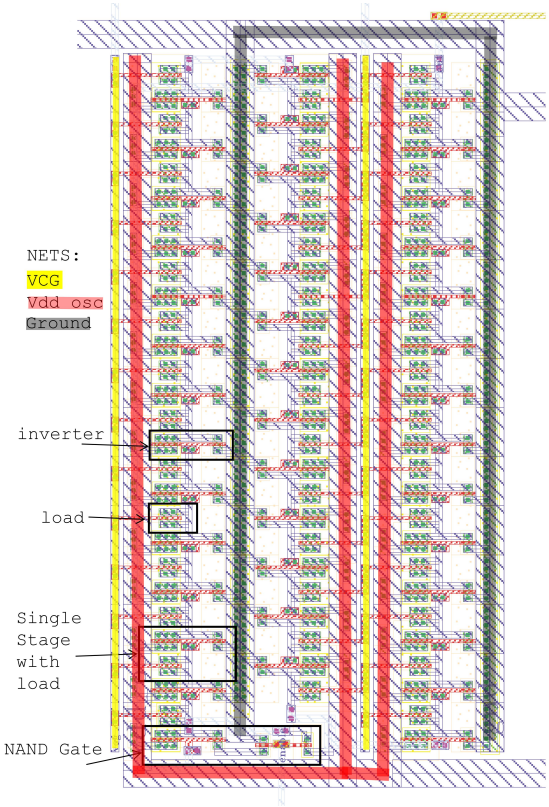
Figure 2.24a shows one complete ring oscillator from the first test chip, in this case with a PMOS load. The same framework, i.e. the routing of the different supply and control voltages, is used for every oscillator. The only difference between an oscillator and its reference is the missing gate of the load transistor. This can be seen in more detail in figures 2.24b and 2.24c. This way systematic offsets are avoided.
The forty oscillator stages are placed in three rows with a NAND gate at the bottom. The equivalent oscillators that are placed on the second test chip pictured in figure 2.23b are reduced to 31 stages because an uneven number of stages is needed and a prime number of stages suppress harmonics.



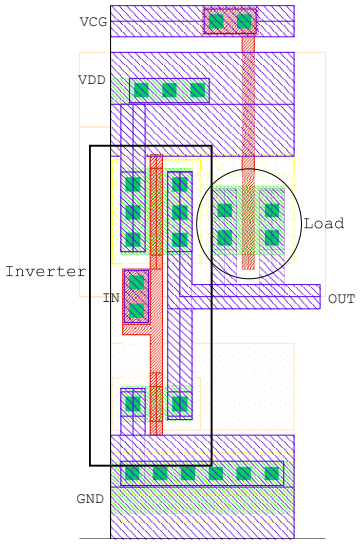
(a) Final layout of the **cgds** test chip with structures from design 2.

(b) Final layout of the $\mathbf{T_{ox}}$ test chip with structures from design 1 and design 2.

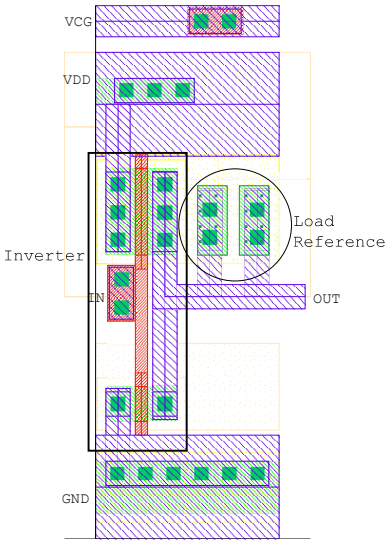
Figure 2.23: Layout of test chip 1 and 2



(a) Layout for one oscillator structure from design 2. The same frame is used for all ring oscillators in this design to ensure symmetry between the different oscillators.



(b) Layout of a single oscillator stage with PMOS load, design 2.



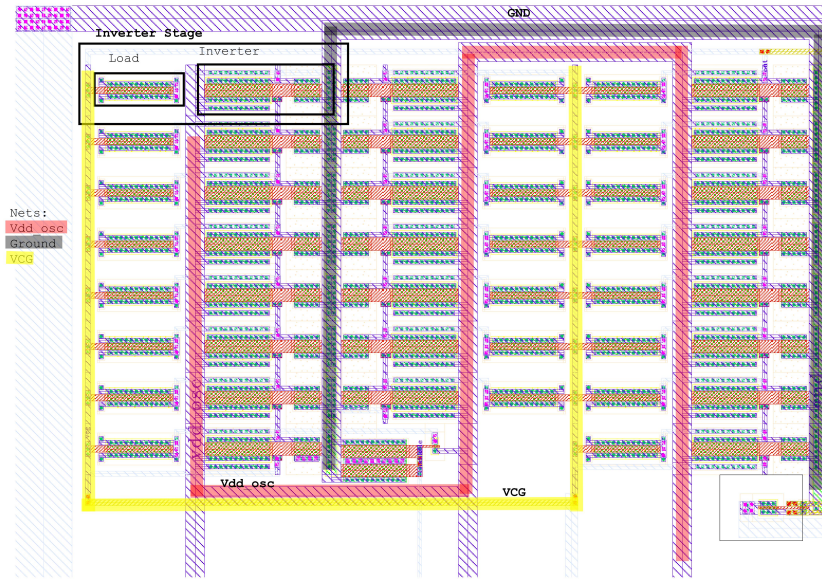
(c) Layout of a single reference oscillator stage for a PMOS load, design 2.

Figure 2.24: Layout details of design 2

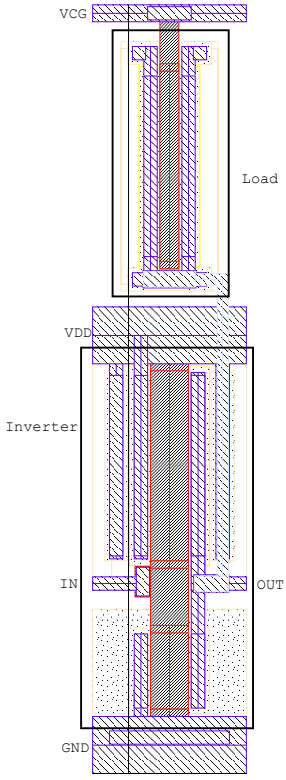
The size difference between designs 1 and 2 is nicely shown in figure 2.23b. The eight oscillators from design 1 clearly cannot fit between the standard pad placement that is used although the number of stages has already been reduced to $n = 23$. In figure 2.25a the layout for the smallest oscillator of that design is shown and details of the loaded and reference stage in figures 2.25b and 2.25c. The loads are now placed outside of the inverter stage. This is necessary as the bulk of each load is shorted with its drain and source, and therefore each load transistor needs its separate well. Unfortunately, this increases the size of the oscillator considerably. Again the only difference between loaded and reference oscillator is the missing gate of the load transistor.

2.4.3 Verification of the Layout

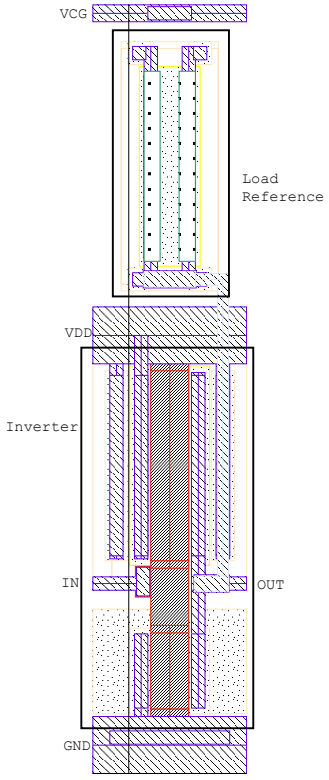
With a complete layout parasitic elements like routing capacitances or resistances can be extracted. These parasitic elements are not included in the nominal simulations that are described in section 2.3 and might have an impact on the accuracy or introduce an offset. It is therefore necessary to extract the parasitic elements and re-simulate the extracted view.
As previously described the desired capacitance is isolated by comparing the oscillators to their references. In the schematic design, diodes that represent the drain and source to bulk junctions are placed between each inverter stage of the reference. Their dimensions are determined with the same equations as they are for the MOSFET models. This is done to eliminate the junction capacitance from the capacitance measurement. This approach does not work with the layout. As it turns out, only three sides of the sidewall of the junction capacitance are modeled in these MOSFET models, the side facing the gate being neglected. However, when the diodes are placed, i.e. the same transistor only without a gate, all four sides of the sidewall contribute to the junction capacitance. This makes it impossible to extract the overlap capacitance with the developed method, as the reference now has a bigger capacitance than the respective loaded ring oscillator. Consequently, simulations with the layout cannot be compared to the simulations which have been presented up to now. In order to get some idea of how the schematic simulations compare with the layout, the frequencies of some oscillators are compared in tables 2.7a and 2.7b. These are from test chip 1 a PMOS and NMOS oscillator with one micron load width and their respective reference oscillators in table 2.7a. From test chip 2 the oscillator with the smallest load and its reference from the $\mathbf{T_{ox}}$ test structure are shown in table 2.7b. Additionally, the equivalent PMOS structure as already placed on test chip 1 to measure the overlap capacitance parameter is given here again. Worst power and worst speed simulations are performed with the layout extract. Actual measurements are also included.
The frequency difference between the loaded oscillators and their references is given because for the measurement it is more important how the oscillators vary relative to each other than their absolute value. For the schematic and layout simulations of design 2 the references have a slightly bigger capacitance due to the capacitance of the fourth diode sidewall. Thus, their frequency is smaller than that of their respective loaded oscillators. This can also be seen for measurements on the PMOS structure which are shown in the last column of table 2.7a. Here, however, this is not due to a bigger capacitance in the



(a) Layout for one oscillator structure of the $\mathbf{T_{ox}}$ design from design 1.



(b) Layout of a single oscillator stage with PMOS load, design 1.



(c) Layout of a single reference oscillator stage for PMOS load, design 1.

Figure 2.25: Layout details of the $\mathbf{T_{ox}}$ test structure, design 1

Table 2.7: Simulation and measurement results for test chip 1 and 2. f_l ... frequency of loaded oscillator; f_r ... frequency of reference oscillator; $\Delta f = f_r - f_l$; ws ... worst case speed; tm ... typical mean; wp ... worst case power.

(a) Test chip 1. Shown are the results for the loaded oscillators f_l with 1 micron load width and their references f_r from design 2. NMOS and PMOS refer to the type of load transistor in the oscillators.

		Simulation								Measurement	
		Schematic		Extracted View							
	Unit	NMOS	PMOS	NMOS			PMOS			NMOS	PMOS
		tm	tm	ws	tm	wp	ws	tm	wp		
f_l	MHz	171.0	163.2	79.4	125.2	176.8	80.5	124.1	181.1	136.4	137.3
f_r	MHz	169.9	160.5	77.6	123.8	173.1	79.4	122.8	179.3	138.6	136.9
Δf	MHz	1.1	2.7	1.8	1.4	3.7	1.1	1.3	1.8	-2.2	0.4

(b) Test chip 2. Shown are the results for the smallest oscillator of design 1 and its reference, and the oscillators with one micron load width of design 2. D1 ... Design 1; D2 ... Design 2.

		Simulation								Measurement	
		Schematic		Extracted View							
	Unit	D1	D2	D1			D2			D1	D2
		tm	tm	ws	tm	wp	ws	tm	wp		
f_l	MHz	24.4	216.5	17.2	21.0	26.6	108.6	157.0	246.0	23.0	164.4
f_r	MHz	30.8	212.9	21.2	25.9	32.5	107.8	156.1	245.7	28.7	163.8
Δf	MHz	-6.4	3.6	-3.9	-4.9	-5.9	0.8	0.9	0.3	-5.7	0.6

reference but to a slightly bigger current consumption of the loaded oscillator.
It can be seen that the parasitic elements have a big influence on the frequency for the smaller oscillators. The difference between the schematic and extracted view simulations goes up to almost 60MHz in table 2.7b. Compared to that the bigger structures of design 1 are barely influenced at all.
Although the measurement results will be further discussed in section 2.6.2 they are given here to show that the simulation results with parasitics approximate the measurement quite well. Furthermore, the results lie in the process variation interval given by the worst case simulations.

2.5 Measurement Setup

Two different designs with two different applications are being presented. The overlap capacitance test structure is intended to monitor the overlap capacitance during fabrication and is therefore built into a standard scribe line. The second design is too big for a monitoring structure and more relevant for device characterization. These measurements are done in the laboratory with probe stations and parameter analyzers. However, both test chips will be evaluated in the laboratory under the same conditions. Therefore the laboratory setup as indicated in the diagram 2.26 will be described in this section.

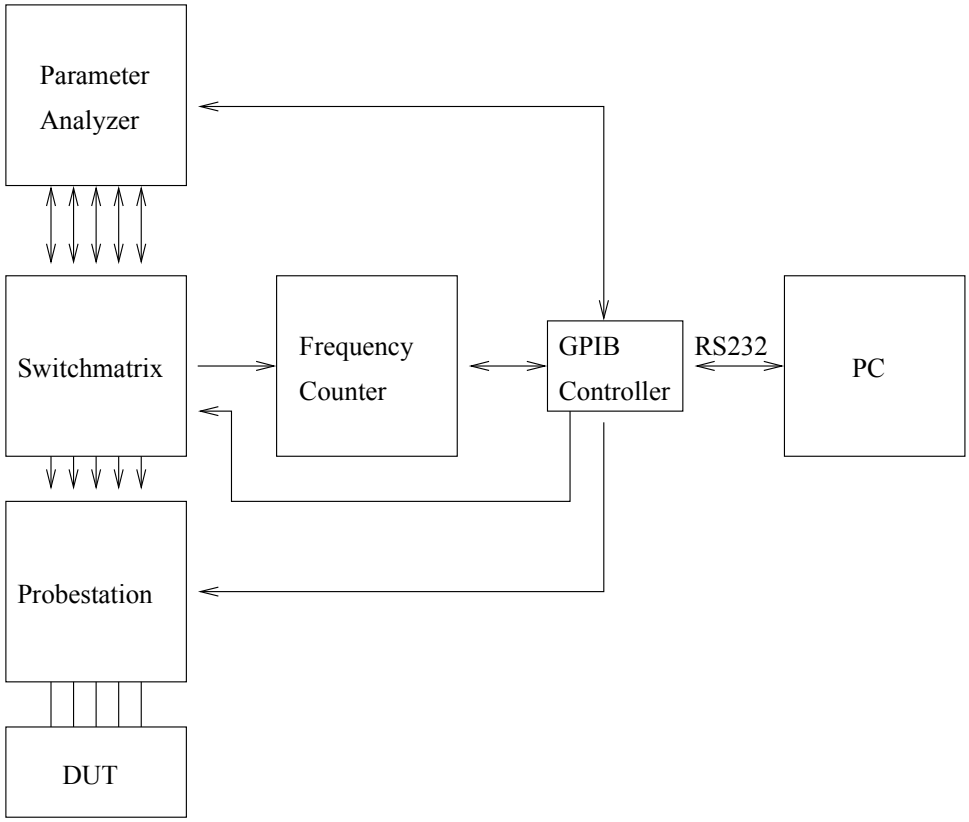


Figure 2.26: Schematic Measurement Setup. The different components are controlled with Matlab using a GPIB controller.

2.5.1 Measurement Equipment

The basic setup consists of a probe station, a parameter analyzer, a switch matrix and a frequency counter. All of these instruments are controlled through Matlab via GPIB. With the switch matrix signals can be dynamically assigned to the different needles of the probe card without the need to reconnect. The probe station that is used can move the contact needles from site to site and reconnect automatically once the wafer has been aligned and the die size specified. In the following sections these instruments will be introduced in more detail.

Parameter Analyzer

The parameter analyzer used for this setup is the Agilent 4155C Semiconductor Parameter Analyzer. It provides four source/monitor units (SMU) in addition to two voltage source units (VSU), two voltage measurement units (VMU) and a ground unit [7]. The units are assigned in the following way: SMU1 through SMU4 supply the eight ring oscillators, VSU1 supplies all the rest of the circuitry, i.e. decoder and read out circuitry, VSU2 provides the gate voltage V_{CG}, and the Ground Unit is used as common reference. Thus

Range	Measurement Value [a]	Measurement Resolutions [b]			
		Integration Time			High Speed Sampling Measurement [c]
		1PLC or Longer	640 µs to 1.92 ms	80 µs to 560 µs	
1 nA	0 ≤ |I| ≤ 1.15 nA	10 fA	10 fA	100 fA	1 pA
10 nA	0 ≤ |I| ≤ 11.5 nA	10 fA	100 fA	1 pA	10 pA
100 nA	0 ≤ |I| ≤ 115 nA	100 fA	1 pA	10 pA	100 pA
1 µA	0 ≤ |I| ≤ 1.15 µA	1 pA	10 pA	100 pA	1 nA
10 µA	0 ≤ |I| ≤ 11.5 µA	10 pA	100 pA	1 nA	10 nA
100 µA	0 ≤ |I| ≤ 115 µA	100 pA	1 nA	10 nA	100 nA
1 mA	0 ≤ |I| ≤ 1.15 mA	1 nA	10 nA	100 nA	1 µA
10 mA	0 ≤ |I| ≤ 11.5 mA	10 nA	100 nA	1 µA	10 µA
100 mA	0 ≤ |I| ≤ 100 mA	100 nA	1 µA	10 µA	100 µA

a. This column is applied to the auto ranging or the limited auto ranging. For fixed ranging, maximum measurement value is **Range** column value.
b. Measurement resolution depends on the integration time setting. For Knob sweep measurement, see the column of Integration Time 80 µs to 560 µs.
c. This column is applied to the sampling measurement that *initial interval* is set to 480 µs or shorter.

Figure 2.27: Current measurement resolution of the Medium Power SMUs as given in [8].

the average current of the ring oscillators in their oscillating states can be measured by the same units that supply them. As each supply pad is connected to both the loaded oscillator and its respective reference, the quiescent current that is measured is the sum of both of them. The current average in the oscillating state is in the range of milliamperes, for which the current resolution is given as one nanoampere as can be seen in figure 2.27 for integration time 1PLC or longer. Hereby 1PLC is defined as one power line cycle and equals 1PLC=20ms. In the quiescent state the average current is in the range of 100 nanoamperes for which a resolution of 100 fA is given. This is at least four orders of magnitudes smaller than the current consumption in the oscillating state.
The measurement sequence is a linear sampling measurement with two sampling points. The integration time is set to medium, which is equal to one PLC in this measurement range ([8] page 7-34). The integration time defines the number of measurement samples the SMUs take and average over to obtain a measurement value. In this fashion, errors caused by line frequency noise and other environmental noise sources are reduced [8]. Although a medium integration time increases the measurement time, the measurement accuracy was observed to be significantly better compared to measurements with short integration time. With a long integration time, however, no major improvement could be seen. In addition, to obtain the final measurement value, the resulting two measurements from the two sampling points are averaged.

Frequency Counter

The Agilent 5334A Universal Counter is used for the frequency measurements. The user manual is given in [9]. The circuit output is directed to the input A of the counter and

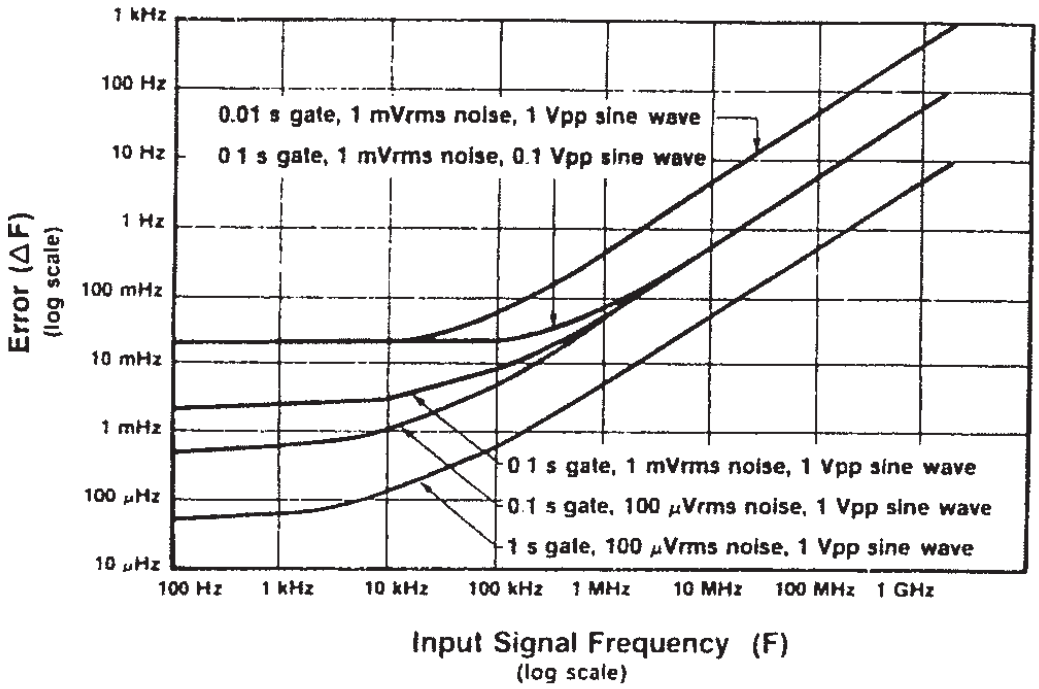


Figure 2.28: Frequency resolution error as function of gate time taken from [9].

the frequency is measured. The gate time is set to ten seconds, which is the time that the counter measures the signal. It averages all of the measured periods to calculate the frequency. Therefore, the gate time determines the measurement resolution and the frequency resolution error as shown in figure 2.28. In this graph the maximum gate time shown is one second, which is therefore used to determine the error. The accuracy of the frequency measurement is given by [9] on page 1-2 as

$$\text{Accuracy} = \pm\text{Resolution} \pm \text{Timebase Error} . \tag{2.32}$$

If all the worst case errors are taken at around 150kHz input frequency, the timebase error is dominant with an error of 10Hz. This error is taken from the graphic in figure 2.29. Even the worst error in graphic 2.28, which is around 200mHz for $f = 150\text{kHz}$, is still significantly smaller than the error introduced by the timebase.
Further settings for the counter are the input attenuation (a), which is set to an attenuation of a=10, and the trigger level. The output signal is always in the range of zero and $V_{DD} = 3.3V$. Therefore, with an attenuation of a=10, the trigger level V_{trigger} is set to $V_{\text{trigger}} = 0.15V$, to place the trigger level around the center of the incoming signal.

Probe Station

The probe station is Cascade Microtech's Summit 12k semi-automatic prober with Nucleus 3.1 control software. Probe cards specifically designed for the device under test (DUT) can be used with this probe station. As the probe needles cannot be adjusted separately,

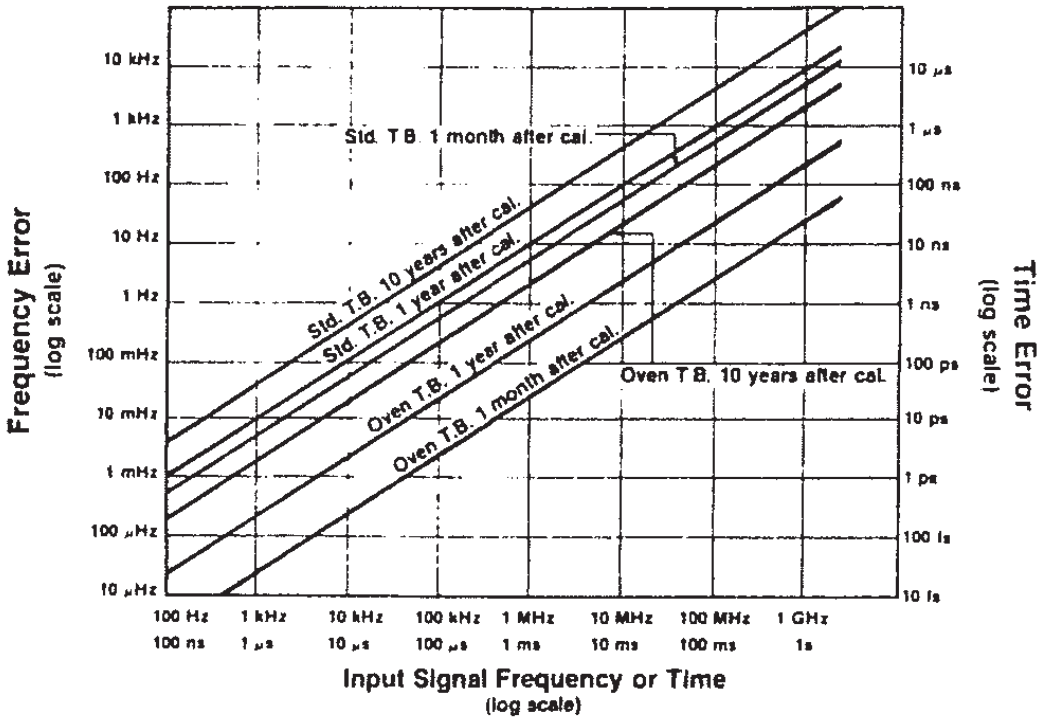


Figure 2.29: Timebase error for the Agilent 5334A Universal Counter shown in [9]. The timebase error is determined by the crystal environment and aging effects.

the wafer needs to be aligned to the probe card. This is done by adjusting the orientation of the chuck, which is the platform on which the wafer is placed in the prober. After that, the die size needs to be specified. This is necessary for automatic measurements, where the control software moves the chuck in a predefined pattern. If the die size is not specified correctly, the chuck will not move to the correct location for the following measurements. With an accurate setup, the dies that are to be measured can be selected with the software and several measurements performed without any further supervision from the operator necessary.

Switch Matrix

All inputs to the probe station are routed via a switch matrix. The supply voltages provided by the parameter analyzer are dynamically assigned to the respective probe needles. Therefore, when an assignment is applied to the switch matrix, all supply voltages are turned off. This way the addresses needed to select each of the oscillators can be applied by simply switching the respective probe needles either to 3.3V or ground. The probe card can thus remain connected to the DUT, reducing the wear on the probe pads.

2.5.2 Measurement Error Estimation

In order to estimate the measurement error the equation to determine the capacitance per stage is used

$$C_s(f, I) = \frac{\frac{1}{n \cdot f} \cdot I}{V_{DD}} \tag{2.33}$$

where n is the number of stages, f the measured frequency, I the measured average current and V_{DD} the oscillator supply voltage. Approximating the capacitance with a Taylor series aborted after the first derivative yields

$$C_s(f, I) = C_s(f_0, I_0) + \frac{\partial C_s(f, I)}{\partial f} \cdot (f - f_0) + \frac{\partial C_s(f, I)}{\partial I} \cdot (I - I_0) \tag{2.34}$$

with f_0 and I_0 denoting the measurement values without error and f and I the actually measured values. If the partial derivatives are calculated,

$$\frac{\partial C_s(f, I)}{\partial f} = -\frac{I}{f^2 \cdot n \cdot V_{DD}} \tag{2.35}$$

$$\frac{\partial C_s(f, I)}{\partial I} = \frac{1}{f \cdot n \cdot V_{DD}} \tag{2.36}$$

and with $\Delta f = (f - f_0)$ and $\Delta I = (I - I_0)$ given as the measurement accuracies of the test equipment, the error can be approximated as

$$\Delta C_s = \sqrt{\left(\frac{\Delta I}{f \cdot n \cdot V_{DD}}\right)^2 + \left(\frac{I \cdot \Delta f}{f^2 \cdot n \cdot V_{DD}}\right)^2}. \tag{2.37}$$

For measurements on the first test chip, which comprises the oscillators from design 2, Δf and ΔI are given as $\Delta f = 10\text{Hz}$ and $\Delta I = 100\text{nA}$ respectively. The error is calculated for a frequency of $f = 135\text{kHz}$ and $I = 0.5\text{mA}$ current, which is the representative range of the measured values. $n = 41$ is the number of oscillator stages and $\text{V}_{\text{DD}} = 3.3\text{V}$ the oscillator's supply voltage. As the ring oscillator frequency is divided by 1024, the frequency error and the frequency itself need to be multiplied by that factor to get the error for the actual capacitance measurement.

$$\Delta C_s \approx 6 \cdot 10^{-18}\text{F} \tag{2.38}$$

Multiplying this error with $\sqrt{2}$ to take the comparison of the loaded and the reference oscillator into account, dividing by two – the overlap capacitance is half of the measured value – and dividing by $\text{W}_{\text{min}} = 1\mu\text{m}$, which is the smallest load width, yields the capacitance per width error.

$$\mathbf{\Delta cgds} = \frac{\Delta C_s \cdot \sqrt{2}}{2 \cdot \mathrm{W_{min}}} \approx 4.3 \cdot 10^{-12} \frac{\mathrm{F}}{\mathrm{m}} \tag{2.39}$$

This error is in the percentage region of the parameter of interest, which is expected to be around $\mathbf{cgds} \approx 10^{-10} \frac{\mathrm{F}}{\mathrm{m}}$.
Repeating the same procedure for the design 1 test structures yields an error of

$$\Delta C_s = \sqrt{\left(\frac{10^{-7}\mathrm{A}}{20 \cdot 10^3 \cdot 1024\mathrm{Hz} \cdot 23 \cdot 3.3\mathrm{V}}\right)^2 + \left(\frac{0.5 \cdot 10^{-3}\mathrm{A} \cdot 1 \cdot 1024\mathrm{Hz}}{(20 \cdot 10^3 \cdot 1024\mathrm{Hz})^2 \cdot 23 \cdot 3.3\mathrm{V}}\right)^2} \tag{2.40}$$

$$\Delta C_s \approx 7 \cdot 10^{-17}\mathrm{F}. \tag{2.41}$$

The frequency of these oscillators from design 1 is smaller compared to the oscillators from design 2 due to their bigger size. Thus, a value of $f = 20\mathrm{kHz}$ is chosen, which is in the range of the measured values. For this frequency the error is taken as $\Delta f = 1\mathrm{Hz}$ from figure 2.29. The supply voltage $\mathrm{V_{DD}} = 3.3V$ and the average current I is equal to that of design 2. The number of stages is $n = 23$ in this case.
The oxide thickness error $\mathbf{\Delta T_{ox}}$ for the smallest structure is found to be

$$\mathbf{T_{ox}} = \frac{\epsilon}{C_s} \cdot W \cdot L \tag{2.42}$$

$$\mathbf{\Delta T_{ox}} = \sqrt{2} \cdot \left|\frac{\partial \mathbf{T_{ox}}}{\partial C_s}\right| \cdot \Delta C_s \tag{2.43}$$

$$\mathbf{\Delta T_{ox}} = \frac{\epsilon \cdot \sqrt{2}}{(\frac{C_s}{W \cdot L})^2} \cdot \frac{\Delta C_s}{W \cdot L} \tag{2.44}$$

$$\mathbf{\Delta T_{ox}} = \sqrt{2} \cdot \mathbf{T_{ox}}^2 \cdot \frac{\Delta C_s}{\epsilon \cdot W \cdot L} \tag{2.45}$$

$$\mathbf{\Delta T_{ox}} = 1.8 \cdot 10^{-11}\mathrm{m}. \tag{2.46}$$

For $\mathbf{T_{ox}}$, W, and L nominal values are used. The calculated error for $\mathbf{T_{ox}}$ is also in the percentage region of the expected parameter value $\mathbf{T_{ox}} = 7.754 \cdot 10^{-9}\mathrm{m}$.

2.6 Measurements, Results and Discussion

This section should give an overview over the measurement results and the parameter extraction. Furthermore, shortcomings of the design will be discussed.

2.6.1 Measurement Results

Measurements are performed on 49 sites across the wafer for the first test chip and on 84 sites for the second test chip. Each site is measured five times in a row, whereby after

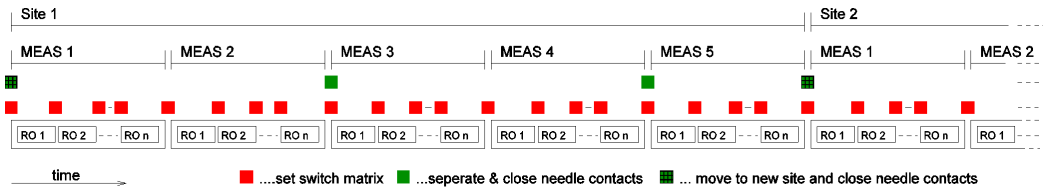


Figure 2.30: Measurement principle to determine measurement reproducibility. Each site is measured five times, where after the second and fourth measurement the probe card is reconnected.

the second and fourth time the probe card is reconnected as shown schematically in figure 2.30. To sort out outliers, the interquartile range criterion is used. A graphical description of the interquartile range can be seen in figure 2.31. For discrete measurement values, the quartiles can be obtained by ordering the measurement values according to their size and dividing the resulting set into four parts. Each part of the set contains an equal amount of measurement results. The lower quartile Q1 and upper quartile Q3 are equal to the values at 25% and 75% of the set. The interquartile range IQR is the difference between the mesurement values at Q3 and Q1. All measurement results that are 1.5 times IQR above the upper quartile Q3 or 1.5 times IQR below the lower quartile Q1 are excluded. The mean and the standard deviation of the measurement are calculated from the remaining values.

The errors estimated from the considerations of the previous section seem overly pessimistic. By measuring each site five times in a row, the actual error for the measurement is determined as follows. The differences between the measurement results are calculated for two situations: between the first and second, and third and fourth measurement the probe card remains connected; and between the second and third, and fourth and fifth measurement the probe card is reconnected. Therefore, by taking the differences between the results where the probe card remains connected and calculating the standard deviation, the statistical deviations that the switch matrix and other measurement equipment introduce can be calculated. The second error that can be calculated also includes the probe card as an error source. This error is bigger than the first one as it includes all previous error sources in addition to the needle to contact error. Therefore, this is the error given in table 2.8 in the column titled "Reproducibility". These errors are a magnitude smaller than the errors estimated in the previous section. Although systematic errors are not included in this calculation, the result is still excellent, as the variation of the parameter can be determined accurately.
Histograms of the measurement results and their discussion are given in the next section and in the appendix A.3.

2.6.2 Discussion

First the PMOS overlap test structure will be discussed. The value obtained for the gate to source/drain overlap capacitance parameter is about half as big as the expected value from figure 2.10a. Yet, as this occurs for both measurements on test chip one and two –

Table 2.8: Measurement Results and Comparison with Manufacturing Acceptance Parameters (MAP)

	Test chip 1			Test chip 2				
	Mean Value	Standard Deviation	Reproducibility	Mean Value	Standard Deviation	Reproducibility	MAP	
PMOS **cgds**	$6.65 \cdot 10^{-11}$	$7.1 \cdot 10^{-12}$	$3 \cdot 10^{-13}$	$5.54 \cdot 10^{-11}$	$8.9 \cdot 10^{-12}$	$2 \cdot 10^{-13}$		$\frac{\mathrm{F}}{\mathrm{m}}$
NMOS **cgds**	$2.635 \cdot 10^{-10}$	$5.6 \cdot 10^{-12}$	$6 \cdot 10^{-13}$					$\frac{\mathrm{F}}{\mathrm{m}}$
$\mathbf{T_{ox}}$				$7.9931 \cdot 10^{-9}$	$2.62 \cdot 10^{-11}$	$5 \cdot 10^{-13}$	$7.6259 \cdot 10^{-9}$	m
NWELL $C_{\mathrm{sidewall0}}$				$5.04 \cdot 10^{-10}$	$1.4 \cdot 10^{-11}$	$1 \cdot 10^{-12}$	$4.76 \cdot 10^{-10}$	$\frac{\mathrm{F}}{\mathrm{m}}$
NWELL C_{area0}				$7.27 \cdot 10^{-5}$	$4.9 \cdot 10^{-6}$	$1 \cdot 10^{-7}$	$10.2 \cdot 10^{-5}$	$\frac{\mathrm{F}}{\mathrm{m}^2}$

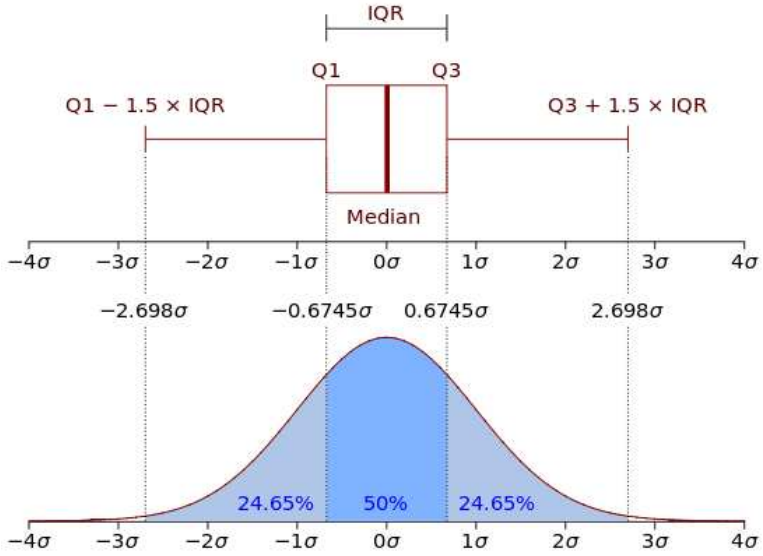


Figure 2.31: Graphical description of the interquartile range criterion taken from [10]. IQR is the interquartile range and σ the standard deviation. Q1 is obtained by integrating the probability density function pdf from $\int_{-\infty}^{Q1} \text{pdf}\, dx = 0.25$, and Q3 from $\int_{-\infty}^{Q3} \text{pdf}\, dx = 0.75$. The interquartile range criterion is approximately equal to the 3σ criterion yet without previous knowledge of σ.

the results can be seen in table 2.8 – with two slightly different layouts, this cannot be considered a measurement error.

Figures 2.34, 2.35 and 2.36 present data, where the overlap test design on the second test chip was measured for different gate voltages V_{CG} and oscillator supply voltages V_{DD}. Figure 2.34 shows the measurement results from the two loaded oscillators, figure 2.36 from the reference oscillators and 2.35 the difference. All results are capacitances per width, i.e. the same extraction procedure as introduced to measure **cgds** is used for each value of V_{CG}. As can be seen the curves in figure 2.34 obtained with higher supply voltages show a smooth transition from the inversion region to the accumulation region of the transistor. For $V_{DD} = 2.0V$, on the other hand, bumps can be seen in the graph. The slopes are different as a result of the averaging that occurs due to the voltage swing at the source and drain. At higher gate voltages, when the transistor is in the accumulation region, the overlap capacitance does not change very drastically as function of voltage anymore, as can be seen in figure 2.10a. Thus the capacitance levels out in that region. When looking at the results from the reference oscillators, it is obvious that something is amiss; there is a very big difference for the measurements with $V_{DD} = 2.5$V and $V_{DD} = 3.3$V compared to the measurement for $V_{DD} = 2.0$V. Although the capacitance of a *pn* junction is expected to increase with smaller reverse bias voltages – this can be seen for $V_{DD} = 2.5$V and $V_{DD} = 3.3$V in figure 2.36 – for $V_{DD} = 2.0$V it is considerably smaller. This unexpected behavior and the results from mismatch simulations in section 2.3.3 indicate that there is a lower limit for the reduction of the supply voltage for the overlap capacitance parameter test structure design 2. In section 2.3.3 the test structure was shown to be too inaccurate

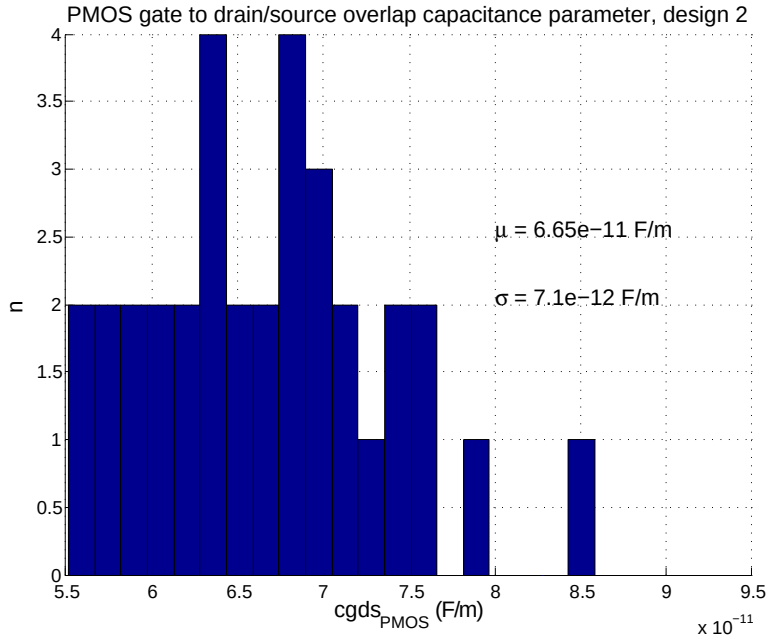


Figure 2.32: $\mathbf{cgds}_{\mathrm{PMOS}}$ measurement results from test chip 1.

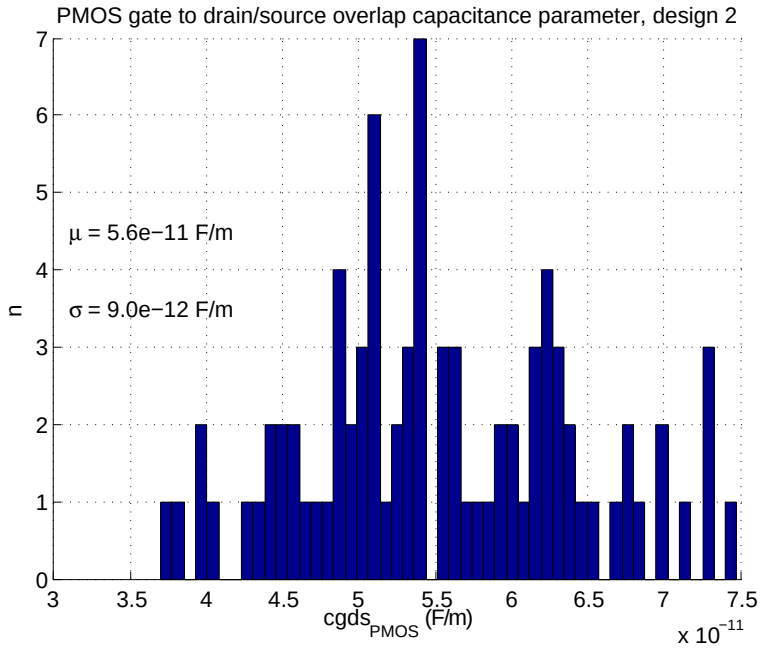


Figure 2.33: $\mathbf{cgds}_{\mathrm{PMOS}}$ measurement results from test chip 2.

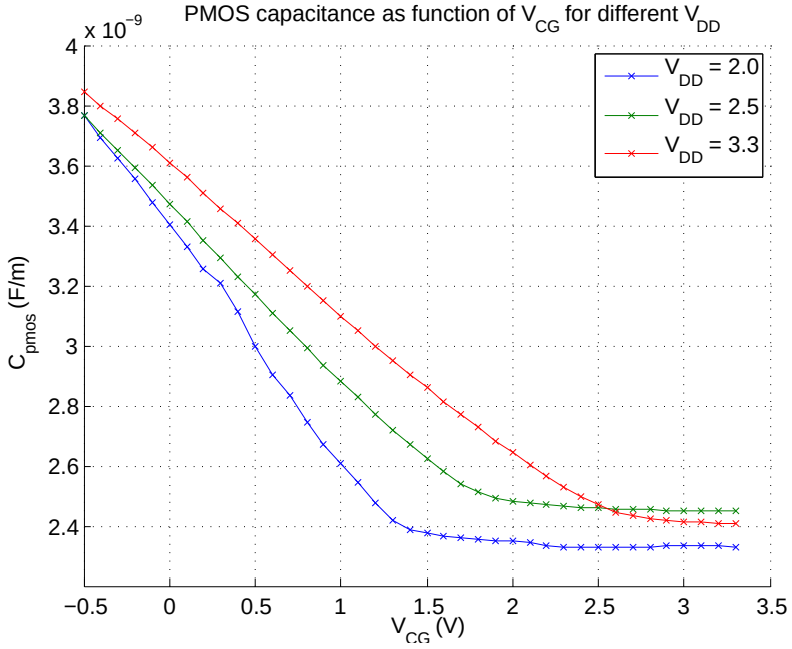


Figure 2.34: C_{PMOS} results from test chip 2. The shown capacitance is a capacitance per width. It is obtained with the **cgds** extraction method applied to the loaded oscillators. The gate voltage is sweeped from $-0.5V \leq V_{CG} \leq 3.3V$. The measurements are performed for three different oscillator supply voltages V_{DD}.

for lower voltages V_{DD}. Actions to improve the mismatch would be to increase the number of stages or the size of the devices. Both changes would disqualify the design for the intended purpose for MAP measurements. The rough transition of the curve in figure 2.34 compared to the smooth course of the other two characteristics is also assumed to be the product of mismatch effects.
The reason for the parameter value being smaller than the result from the simulations is that the sidewalls toward the gate of the transistor are different from the respective sidewalls in the reference. The differences are the lightly doped drain (LDD) region in the transistor and the different doping profile in the reference. Simulating the capacitance for one diode sidewall at $V_{\text{reverse voltage}} = -1.65V$, subtracting that value from the measured diffusion capacitance and repeating the overlap extract, yields a result much closer to the expected value. Making this adjustment yields a mean value of $\mathbf{cgds} = 1.72 \cdot 10^{-10} \frac{\mathrm{F}}{\mathrm{m}}$ compared to the expected $\mathbf{cgds} = 1.398 \cdot 10^{-10} \frac{\mathrm{F}}{\mathrm{m}}$ from figure 2.10a. Due to parasitics such as the metal 1 to gate capacitance, which are also included in the measured value, it is now slightly bigger. These cannot be distinguished from the overlap capacitance because they also scale with the width. To address this problem the drain and source contacts for the different geometries should all be made the same length. Then, the metal 1 to gate capacitance introduces a constant offset which cancels out with the extraction process.

The results for the NMOS test structure from figure 2.37 yield slightly bigger values than obtained from the simulation fig.2.10b. Part of this is due to the comparison with the diffusions of the reference oscillators. When diffusions are placed as close together as

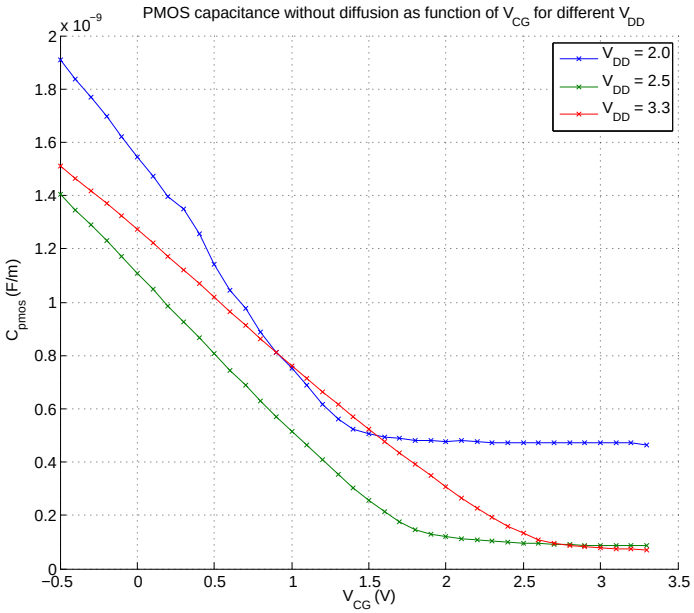


Figure 2.35: C_{PMOS} results from test chip 2. The shown capacitance per width is obtained with the **cgds** extraction method applied to the difference of the loaded and reference oscillators. The gate voltage is sweeped from $-0.5V \leq V_{CG} \leq 3.3V$. The measurements are performed for three different oscillator supply voltages V_{DD}.

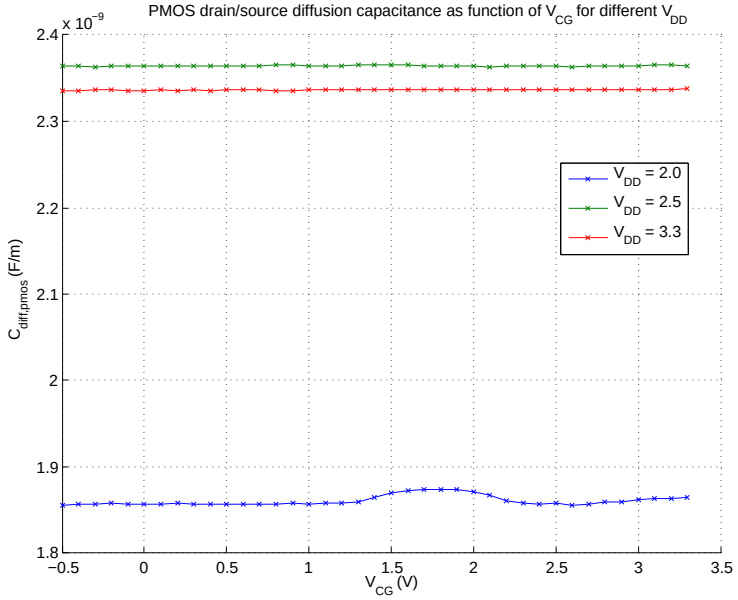


Figure 2.36: C_{pdiff} results from test chip 2. The shown capacitance is a capacitance per width which is obtained with the **cgds** extraction method applied to the reference oscillators.

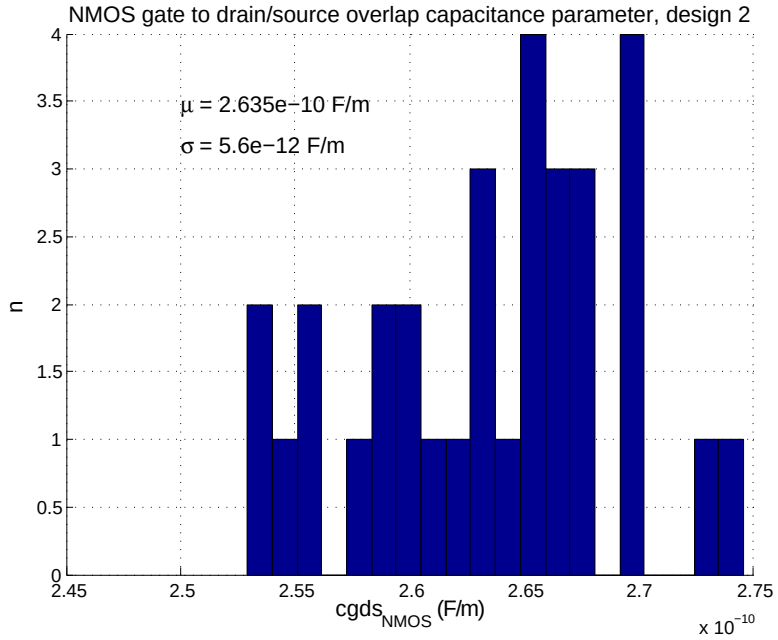


Figure 2.37: $\mathbf{cgds}_{\mathrm{NMOS}}$ results from test chip 1.

in this design, it is possible that the two different areas connect during the fabrication process. The design rule for minimum distance $d_{\min}$ of two diffusions of the same kind is $d_{\min} = 0.6\mu$m. Simulating the two geometries – diodes separated and diodes connected – with capacitance values obtained from monitoring measurements, and comparing that to the measurement results yields figure 2.38. It can be seen that the measured value shown as blue circles is closer to the bottom blue line, which is the value obtained for a geometry where the diffusions are connected. Thus, the difference of the loaded and the reference oscillator is slightly too big in this case.
However, if the deviation from the expected value $\mathbf{cgds} = 2.64 \cdot 10^{-10} \frac{\mathrm{F}}{\mathrm{m}}$ instead of $\mathbf{cgds} = 1.92 \cdot 10^{-10} \frac{\mathrm{F}}{\mathrm{m}}$ is compared to the result for the PMOS devices, it is expected that one big diode more closely resembles the diffusion capacitances than two separate ones. The bigger part of the deviation is assumed to come from the gate polysilicon. As the same framework is used for the NMOS devices as it is used for the PMOS structure (fig. 2.24b), the gate needs to be routed across the whole inverter cell. In the reference it is omitted completely. Thus there will be an extra offset on the result.

The best results are obtained with the bigger tox test structure from design 2. The oxide thickness is calculated for a voltage swing of $V_{DD} = 3.3V$. Yet, due to the large voltage swing, the oxide thickness value at that point – the gate voltage V_{CG} at which the oxide thickness in table 2.8 is determined is referenced as 'Bias point of measurement' in figure 2.40– has not yet reached the point where it can be measured accurately. The deviation can be seen when the measurement value is compared to the value obtained from MAP measurements. Therefore, a gate voltage sweep was performed for different supply voltages. The results can be seen in figure 2.40. These curves represent an equivalent oxide thickness because the oxide thickness does not change as shown. The total capacitance, however,

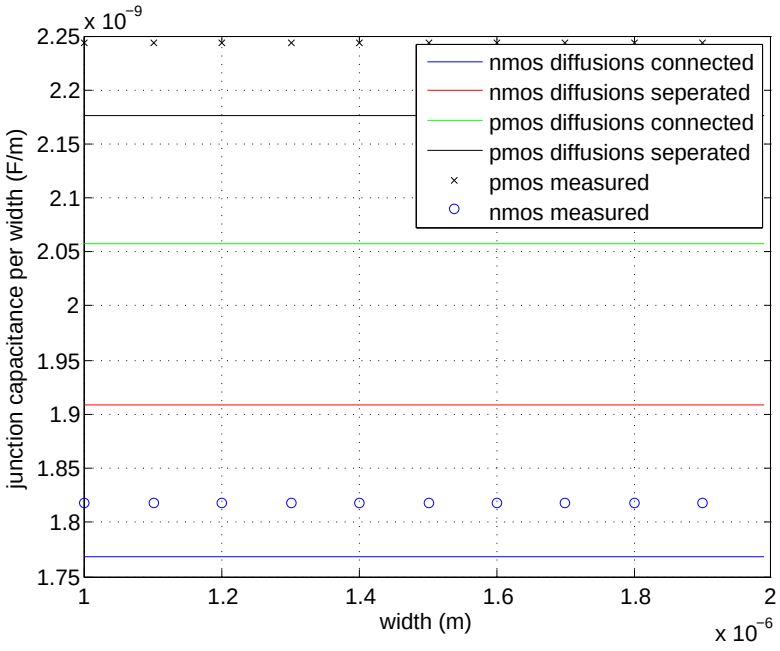


Figure 2.38: Simulated and measured capacitance values per width for n^+ and p^+ diffusions.

does change. The actual oxide thickness can be determined for high gate voltages VCG. For smaller voltage swings at the source and drain this value approaches faster the desired value, which can be seen for both 2V and 2.5V voltage swing. The mismatch in this case is not as dominant as with the overlap test structure, as the transistors are much bigger.

As this design is made up of eight oscillators and their references, a nice side effect is that the nwell parameters can also be determined. These can be seen in the appendix in figures A.9 and A.10. Both the sidewall and area coefficients can be determined and are given in table 2.8. As the measured values are average values around $\frac{V_{DD}}{2}$, the following equations are used to determine the values at zero volts:

$$C_{\text{area}}(V) = C_{\text{area0}} \cdot (1 - \frac{V}{\mathbf{vj}})^{\mathbf{mj}} \tag{2.47}$$

$$C_{\text{sidewall}}(V) = C_{\text{sidewall0}} \cdot (1 - \frac{V}{\mathbf{vjsw}})^{\mathbf{mjsw}} \tag{2.48}$$

These equations to determine the capacitance are valid if the diode is in reverse bias conditions, which is the case here. The parameters **vj**, **mj**, **vjsw** and **mjsw** are BSIM3v3 model parameters, and C_{area0} and $C_{\text{sidewall0}}$ the junction capacitance parameters for zero volts bias voltage. A more detailed description and the values used for the calculation can be seen in table 2.9. In table 2.8 the values for C_{area0} and $\text{C}_{\text{sidewall0}}$ are given to be able to compare them against the MAP results.
The sidewall parameter can be determined in to different ways: either by the side that

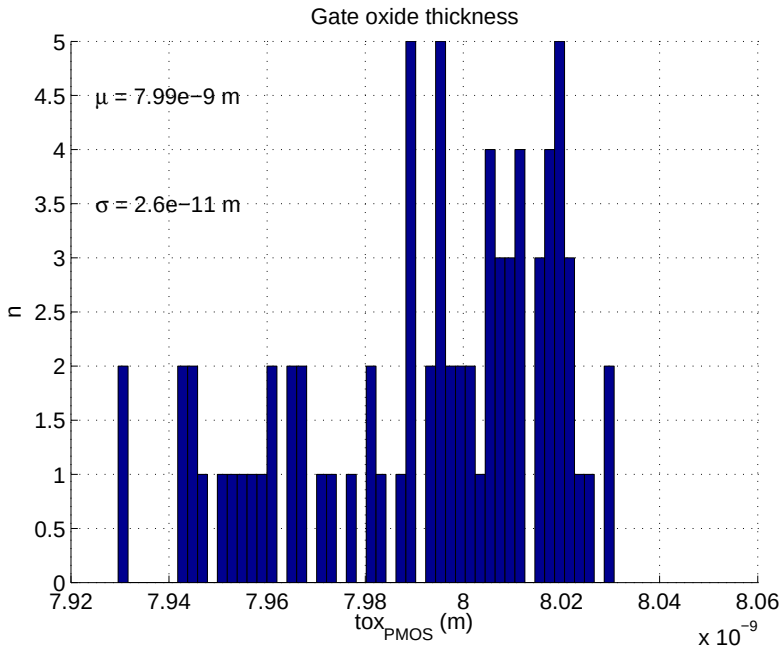


Figure 2.39: $\mathbf{T_{ox}}$ measurement results from test chip 2.

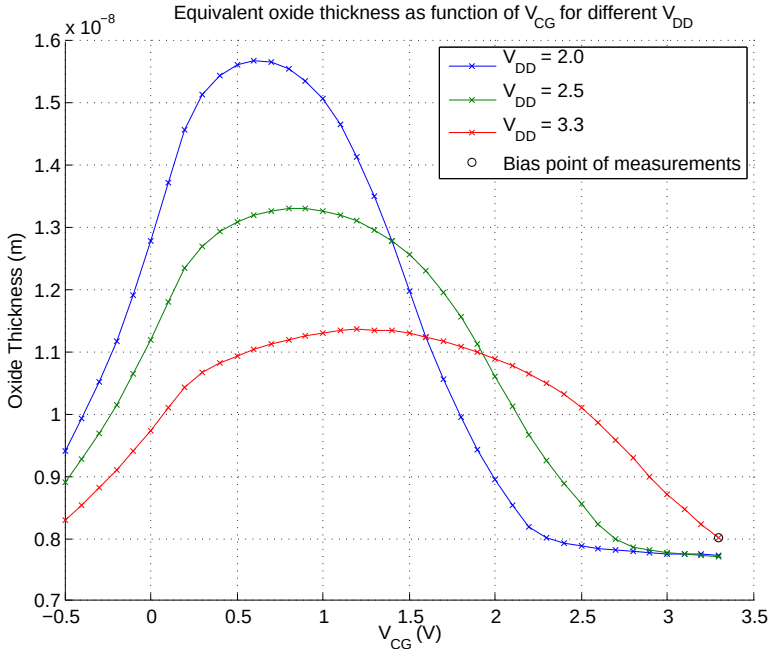


Figure 2.40: $\mathbf{T_{ox}}$ measurement results from test chip 2. The gate voltage is sweeped and the measurement performed for different oscillator supply voltages.

Table 2.9: MOS diode model parameters as given in [4].

Parameter	BSIM3v3 manual	Value	Unit	Description
vj	**Pb**	0.69	V	Bottom junction built-in potential
vjsw	**Pbsw**	0.69	V	Source/drain sidewall junction built-in potential
mj	**Mj**	0.34		Bottom junction capacitance grading coefficient
mjsw	**Mjsw**	0.23		Source/drain sidewall junction capacitance grading coefficient
C_{area}	C_j	$4.80 \cdot 10^{-5}$	$\frac{F}{m^2}$	Bottom junction capacitance per unit area
$C_{sidewall}$	C_{jsw}	$3.80 \cdot 10^{-10}$	$\frac{F}{m}$	Source/drain sidewall junction capacitance grading coefficient per unit length

scales with the length of the transistor or the side that scales with the width. A slight difference exists for these two values. Yet, the extraction with regard to the width is regarded as more accurate, as the widths are bigger than the lengths of the load transistors. Using the sidewall that scales with length yields $C_{\text{sidewall}} = 6.22 \cdot 10^{-10} \frac{F}{m}$ compared to $C_{\text{sidewall}} = 5.04 \cdot 10^{-10} \frac{F}{m}$, which is obtained from the sidewall that scales with width.

2.7 Conclusion

This chapter dealt with extracting the overlap capacitance parameters for NMOS and PMOS devices and the oxide thickness for PMOS devices from measurements on ring oscillators. These are dynamic measurements with voltage swings at the source and drain equal to the supply voltage of the ring oscillators. The extracted parameters are values averaged over the range of operation defined by the voltage swing. As mismatch variations are reduced by using many stages, the variation measured represents the process variation of the respective parameter.
A proposed improvement for the oxide thickness test structure from design 1 is that the Schmitt triggers are replaced by comparators, for which the reference level can be adjusted according to the supply voltage of the oscillators. Then the measurements to determine the oxide thickness $\mathbf{T_{ox}}$ can be performed down to the lowest voltages for which the transistors in the inverter still work as intended. Thereby, the range over which the measured values are averaged is reduced and the accuracy improved.
Regarding the overlap capacitance parameter test structures from design 2, the reference oscillators need to be better matched to the loaded oscillators to filter out the remaining systematic parasitic capacitances. Thus, the gate of the load transistor should not be completely omitted in the reference but cut only shortly before the transistor. In addition, the metal connection to the source and drain should be made the same length for all

load transistors. Finally, the diodes that are placed in the reference as loads should be made one big diode instead of two separate. This more closely resembles the parasitic capacitances in the transistor than using two separate diodes, as the measurement results for the NMOS design show.
Regardless of the improvements that need to be made to the designs, the measurements so far have shown promising results that proof the validity of the methods.

Chapter 3

Variability Characterization

The second objective of this thesis is to investigate ring oscillator circuits designed to measure the threshold voltage variability. Increasing the delay per stage by introducing an additional capacitive load is the method used in the previous chapter. Many stages are used per oscillator to cancel out statistical variations from the measured values. Now the goal is to measure statistical characteristics of the load devices. Therefore, instead of using many stages only a minimum number of stages are implemented. In addition, the load is not intended as a dominating capacitance to increase the delay. Yet, the delay should be very sensitive toward variations of the load. The basic layout of this chapter is the same as for the previous chapter. First, available literature is introduced in section 3.1. This work is based again on research conducted by IBM [11]. Then the circuit design and layout are discussed in sections 3.2 and 3.3.

3.1 Literature Studies

A method utilizing frequency measurements with ring oscillators to determine the threshold variability is described in [11]. Instead of designing oscillators with many stages as in chapter 2, here only a minimum number of stages are required. With many stages in the oscillator random fluctuations, for example in the threshold voltage, are averaged over the number of stages. But the focus of these investigations is precisely local random fluctuations. Thus, the ring oscillators are implemented with only five stages.
The design described in [11] is shown in figure 3.1. The PFET keeper and additional load are not necessarily required for the measurement.

The threshold voltage variability measurement is based on the assumption that it is equivalent whether the threshold voltage is reduced by a little bit or the passgate voltage raised by the same amount. The effect is the same for the mathematical equations. The following equations illustrate this thought process for the drain source current I_{DS}. This is done for a transistor in saturation but can also be shown for the transistor in the triode region.

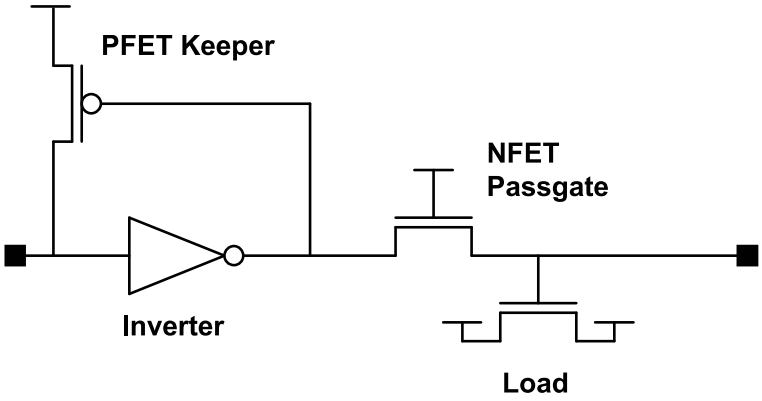


Figure 3.1: Schematic of a ring oscillator stage for threshold variability monitoring as given in [11]. The passgate dimensions should be significantly smaller than the rest of the circuit to make the delay sensitive to the passgate.

$$I_{DS} = \kappa \cdot \frac{W}{L} \cdot \left[\underbrace{V_G - V_S}_{=V_{GS}} - (V_t - \Delta V_t) \right]^2 \tag{3.1}$$

$$I_{DS} = \kappa \cdot \frac{W}{L} \cdot \left[(V_G + \Delta V_t) - V_S - V_t \right]^2 \tag{3.2}$$

κ is hereby a technology constant, W and L the transistor's dimension, V_t the threshold voltage, and V_G and V_S the gate and source potential, respectively. Thus, if the frequency characteristic as a function of the passgate voltage is known, the standard deviation in the frequency measurements $\sigma(f)$ can be directly related to the threshold voltage standard deviation $\sigma(t)$.

$$\sigma(V_t) = \frac{k \cdot \sqrt{n} \cdot \sigma(f)}{\frac{df}{dV_{DD}}} \tag{3.3}$$

where $\frac{df}{dV_{DD}}$ is the frequency characteristic as a function of the supply voltage linearized around the mean passgate gate voltage, the factor $\sqrt{n}$ takes the number of passgates in the oscillator into account, and k should ideally be equal to negative one.

$$k = -\frac{\frac{df}{dV_{DD}}}{\frac{df}{dV_t}} \tag{3.4}$$

Equation (3.4) is the mathematical expression for the assumption this method is based on. However, having the passgate gate voltage tied to the supply voltage is not optimal for measurements. In their investigations Bhushan *et al.* [11] simulated the dependency from

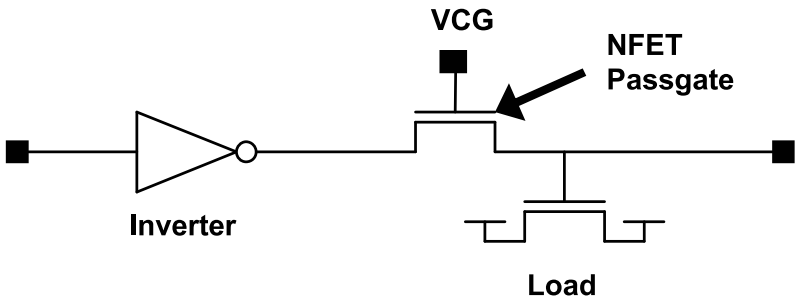


Figure 3.2: Instead of tying the passgate gate to V_{DD} as in figure 3.1, it can be controlled directly via V_{CG} in this circuit shown in [11]

equation (3.4) and discovered that $k = -0.72$ instead of $k = -1$. Thus, they enhanced their design with an extra terminal V_{CG} to directly control the passgate gate voltage (see figure 3.2).

The factor k can now be determined as

$$k = -\frac{\frac{df}{dV_{CG}}}{\frac{df}{dV_t}}. \tag{3.5}$$

Numerous oscillators are then arranged in a matrix configuration with a total of 63 oscillators as illustrated in figure 3.3. To address the oscillators a clock signal is created with one additional ring oscillator. This clock signal is used to drive a counter to create the 64 addresses. The one address where no oscillator is enabled is used as reference point in the matrix. The outputs of the oscillators are then multiplexed to a frequency divider and from there to the output pad. The schematics for the described circuit can be seen in figure 3.4.

3.2 Ring Oscillator Circuit Design

Two different circuits are designed: one circuit with a PMOS passgate and one with a NMOS passgate. Due to the fast oscillation, the ring oscillator's output signal does not go from rail to rail. The voltage swing depends on the kind of passgate used. For the PMOS passgate the waveform is located at higher voltages between about 1.5V to 2.5V. With the NMOS passgate it is between ground to around 2V. Therefore the circuit blocks following the oscillators are different. The circuit as it is for the PMOS passgates will be presented here and the equivalent circuit for the NMOS passgate is shown in the appendix in section B.1.

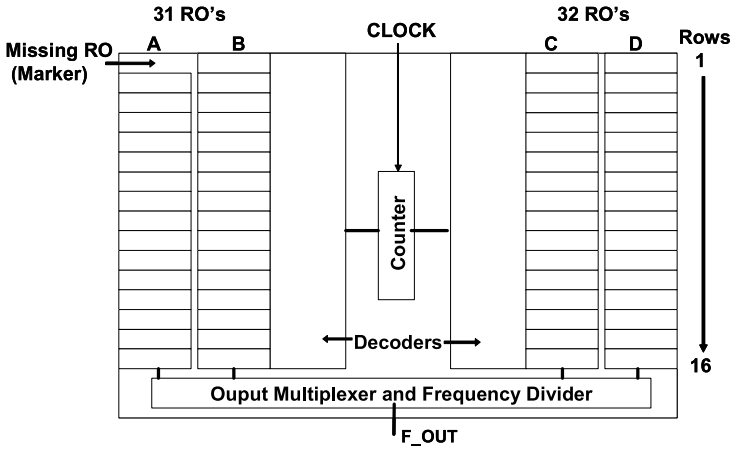


Figure 3.3: Circuit schematic for the ring oscillator matrix with 63 oscillators taken from [11].

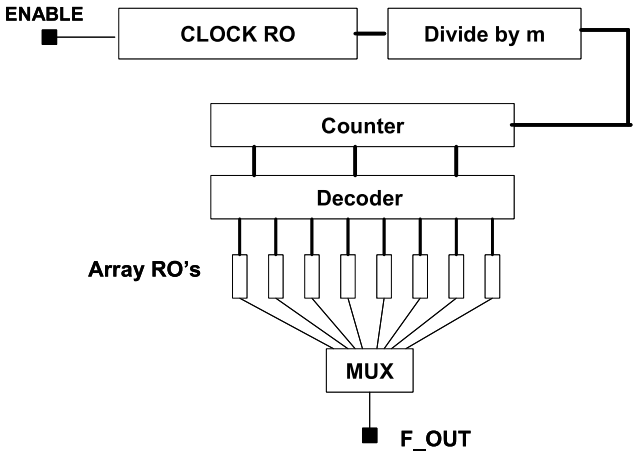


Figure 3.4: Complete Circuit for variability measurements by [11].

The circuit begins with a clock input pad. The clock signal is not created directly on the chip due to space restrictions. Connection pads are in abundance, however, and by using an external clock the duration each oscillator is enabled can be adjusted easily. This clock drives an addressing circuit to enable one oscillator at a time. The addresses are created with a 5 bit counter shown in figure 3.5. A decoder then enables each oscillator in turn.

The oscillator is designed according to the recommendations given in [11]: five inverter stages with an additional passgate load, whereas the inverter stages are dimensioned at least six times as big as the passgate load. Thus, using minimum devices as passgate the dimensions are as in table 3.1. The schematic for an oscillator with PMOS passgate can be seen in figure 3.6.

The additional MOSFET load in figure 3.1 is not included in this design. Its purpose is to decrease the oscillator frequency, which is already quite high for such a small number of stages. If the frequency gets too high, it can cause problems for comparators or similar

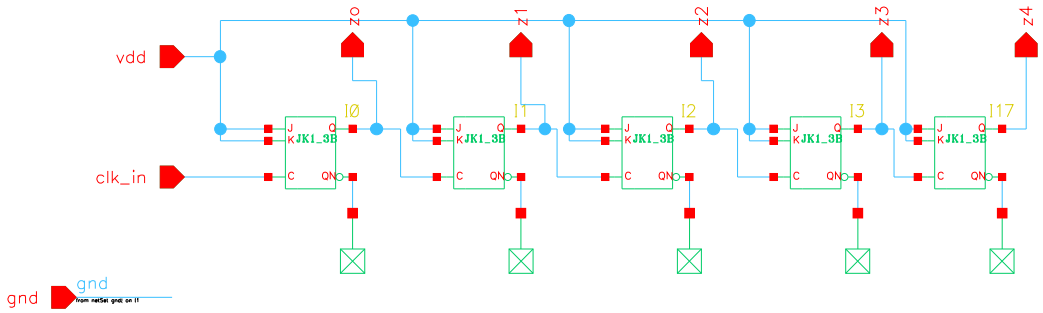


Figure 3.5: Schematic of the implemented 5 bit counter.

Table 3.1: Inverter dimensions for both PMOS and NMOS passgate oscillators.

Oscillator	PMOS		NMOS		passgate	
	width	length	width	length	width	length
	μm	μm	μm	μm	μm	μm
PMOS	6	0.35	3	0.35	0.4	0.35
NMOS	6	0.35	3	0.35	0.4	0.35

circuit blocks. Yet, with five stages and unavoidable parasitic capacitances, the resulting frequency is just within the reach of the implemented comparator.
The first stage is implemented as NAND gate to enable the oscillator. The oscillator outputs are decoupled with a source follower circuit, part of which is shown in figure 3.7. NMOS source followers are used in this case since the oscillation is located in the upper voltage range. Correspondingly, PMOS source followers are used with the NMOS passgate oscillators. An additional switch is placed in each source follower to enable the respective path belonging to the momentarily active oscillator. The enable signal is the same one that enables the oscillator when PMOS source followers are used, and the inverted signal for NMOS source followers. The number of source followers depends on the size of one oscillator and thus the number of oscillators that fit onto one scribe line. As will be shown in the next section, this number is 28. The bias current ibias required for the decouple circuit is provided by an external source. The same bias current is used for the source follower and the comparator.

Two different designs are implemented for the comparator: one with a PMOS differential pair and one with a NMOS differential pair. The schematic of the comparator with PMOS input stage can be seen in figure 3.8, and the corresponding schematic with NMOS input stage in figure B.3. Through the NMOS source follower the signal is again pushed down toward the lower voltage range. Therefore, a comparator with a PMOS input stage is used. The requirements for the comparator are to be small and fast. Thus, a topology with positive feedback is used. With the feedback transistors it is also possible to introduce some hysteresis into the circuit. However, this feature is not required here.

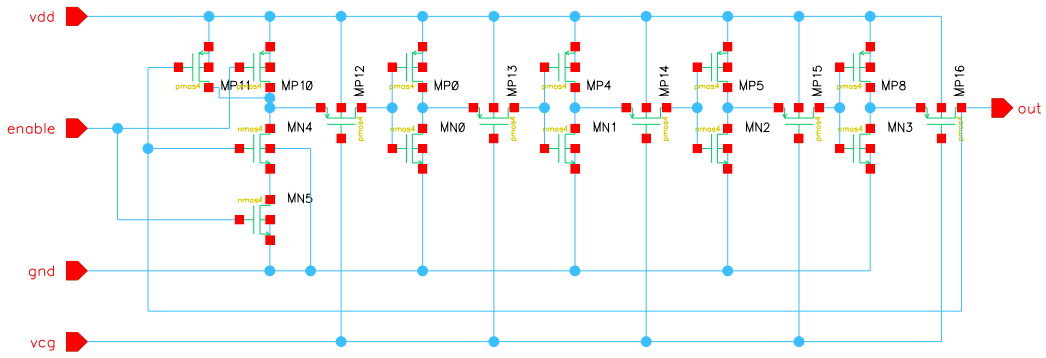


Figure 3.6: Schematic of the PMOS passgate oscillator.

Finally, after the comparator the signal is fed to a frequency divider and then to the output. Schematics of the complete circuit for the PMOS passgate can be seen in figure 3.9 and for the NMOS passgate in the appendix on page 102. The pin description is given in table 3.2.

3.2.1 Simulation Results

As a first step the assumption that the proportionality k from equation (3.4) is equal to minus one is investigated. Therefore, the circuit as shown in figure 3.6 is simulated twice. For the first run a variable offset is added to the threshold voltage of the passgate. The value of this offset is varied linearly from -50 mV to 50 mV. Thus, the oscillation frequency is determined as function of the passgate's threshold voltage. The second run is basically the same, only now, instead of varying the threshold voltage the gate voltage V_{CG} is varied. This is done for both the PMOS oscillators and NMOS oscillators. The gate voltage is nominally $V_{CG} = 0V$ for the PMOS loads and $V_{CG} = 3V$ for the NMOS loads around which it is then varied again linearly from $-50\text{mV} + V_{CG} \leq V_{CG} \leq 50\text{mV} + V_{CG}$. The results in figures 3.10a and 3.10b show that the proportionality factor k in this investigation is significantly different from $k = -1$. It is determined to be $k = -0.874$ for the NMOS passgate oscillator and $k = -0.909$ for the PMOS passgate.

After determining k, the PMOS passgate oscillator is used to validate the methods described in the previous section. Therefore, Monte Carlo simulations are performed for three different gate voltages $V_{CG1} = -0.05V$, $V_{CG2} = 0V$, and $V_{CG3} = 0.05V$. This region is chosen such that it encompasses the threshold voltage variability – the model value is $\sigma(V_{t,\text{model}}) = 27.5mV$ for minimum size devices – but is not too wide to cause significant nonlinearities in the function $f(V_t)$. Two hundred runs are simulated for V_{CG1} and V_{CG3}, and five hundred for V_{CG2}. Only mismatch variations are included in this simulation. With the average values at V_{CG1} and V_{CG3} the slope $\frac{df}{dV_{CG}}$ is determined. Then, setting k in equation (3.3) to $k = -0.909$ and $\sigma(f)$ as the standard deviation calculated from the data points at V_{CG2}, the threshold variability is estimated as $\sigma(V_t) = 27.4mV$. This result

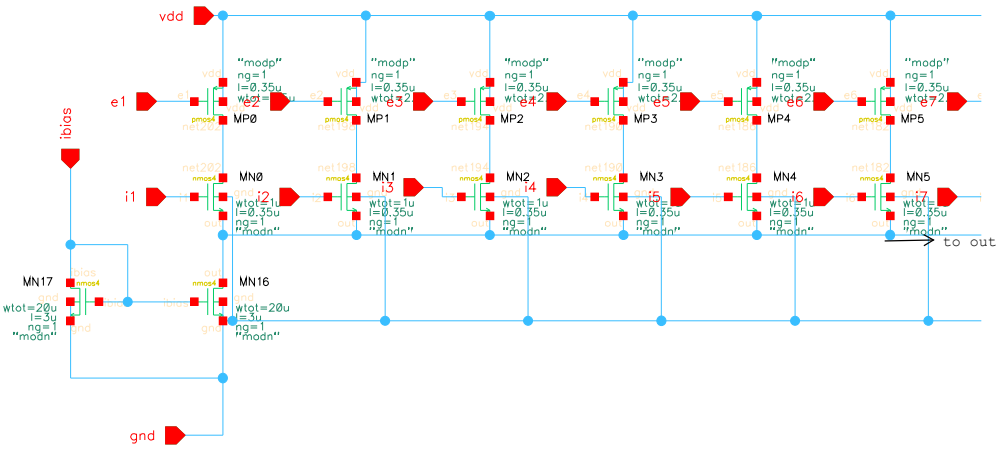


Figure 3.7: Schematic of the NMOS source follower used to decouple the signal from the oscillator. The signals i1, i2... are the signals coming from the oscillators, and e1, e2... from the addressing circuit. The bias current ibias is supplied by an external source.

is quite close to the model value of $\sigma(V_{t,\text{model}}) = 27.5mV$. With the uncertainty u of the standard deviation in equation (3.7) due to the finite amount of samples m

$$u(\sigma(V_t)) = \sigma(V_t) \cdot \frac{1}{\sqrt{2(m-1)}} \tag{3.6}$$

$$u(\sigma(V_t)) = \pm 0.9 \text{ mV}, \quad m = 500 \tag{3.7}$$

the model value is reached. This result, however, is only useful to show that it is indeed possible to extract the threshold voltage variability from these simulations. For the test chip there is not enough space in one scribe line to place 200 oscillators, and the additional circuit elements might also introduce deviations.
Including all the circuit elements and simulating $m = 32$ oscillators with the same conditions as above yields

$$\sigma(V_t) = 32.5 \text{ mV} \tag{3.8}$$

$$u(\sigma(V_t)) = \pm 4.1 \text{ mV}. \tag{3.9}$$

Each oscillator runs for 400ns which is determined by the period of the clock signal. The frequency is then extracted by shifting the output signal down to about the center of its oscillation and finding the time instants where the shifted signal crosses the zero line. With these indices, the period is calculated. An additional uncertainty is introduced this way since the simulated data points are not always spaced equally around the zero crossings. For the measurement, the oscillators will each run longer and therefore the frequency will be determined more accurately. Moreover, the slope $\frac{df}{dV_{CG}}$ also introduces an uncertainty

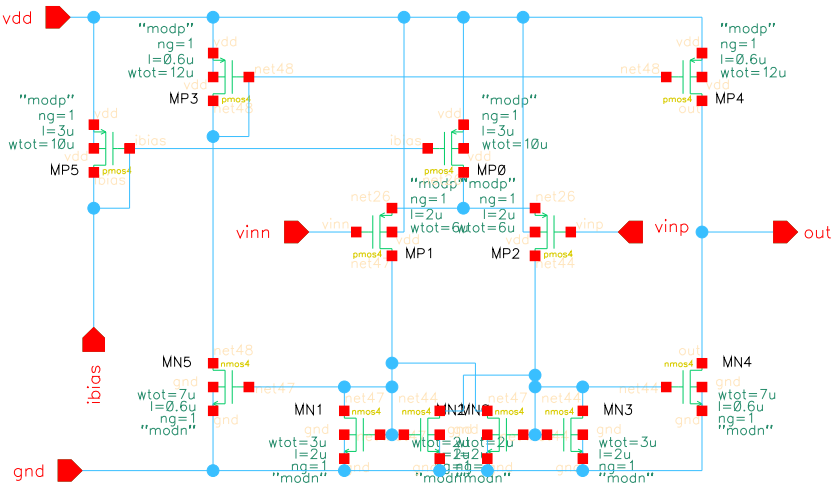


Figure 3.8: Comparator with PMOS differential pair [12].

into the simulation because the mean values at V_{CG1} and V_{CG2} are calculated with a finite number of data points. When measured on the test chip, the frequencies for V_{CG1}, V_{CG2} and V_{CG3} are all measured with the same oscillators. Therefore, if only mismatch variations are of significance, this error is expected to be small since the measurement values will be correlated. This will need to be investigated once measurements are possible. Due to these reasons the measurement value is expected to be closer to the parameter than the result in (3.9).

3.3 Ring Oscillator Circuit Layout

In this section the layout of the variability test chips will be discussed. The layout is basically the same for the NMOS and PMOS test chips. Thus, only the PMOS version is shown here.
All in all 28 ring oscillators are placed on the test chip. Each oscillator is built up identically as illustrated in figure 3.11.

Four oscillators can be placed in between each pad. Although there is still some free space – the complete layout can be seen in figure 3.12a – the limiting factor is the routing of the address lines. It takes up all the space on the top of the scribe line. The oscillator blocks are placed in between ground and supply pads, which are separated from the supply pads of the rest of the circuit. This is done so that variations on the digital supply do not introduce extra jitter in the oscillators. As the 28 oscillators are spread over the length of the scribe line, the procedure to determine the threshold variation needs to be performed for each set of four oscillators separately, and the results averaged. Otherwise, process variations will also have an impact on the outcome.

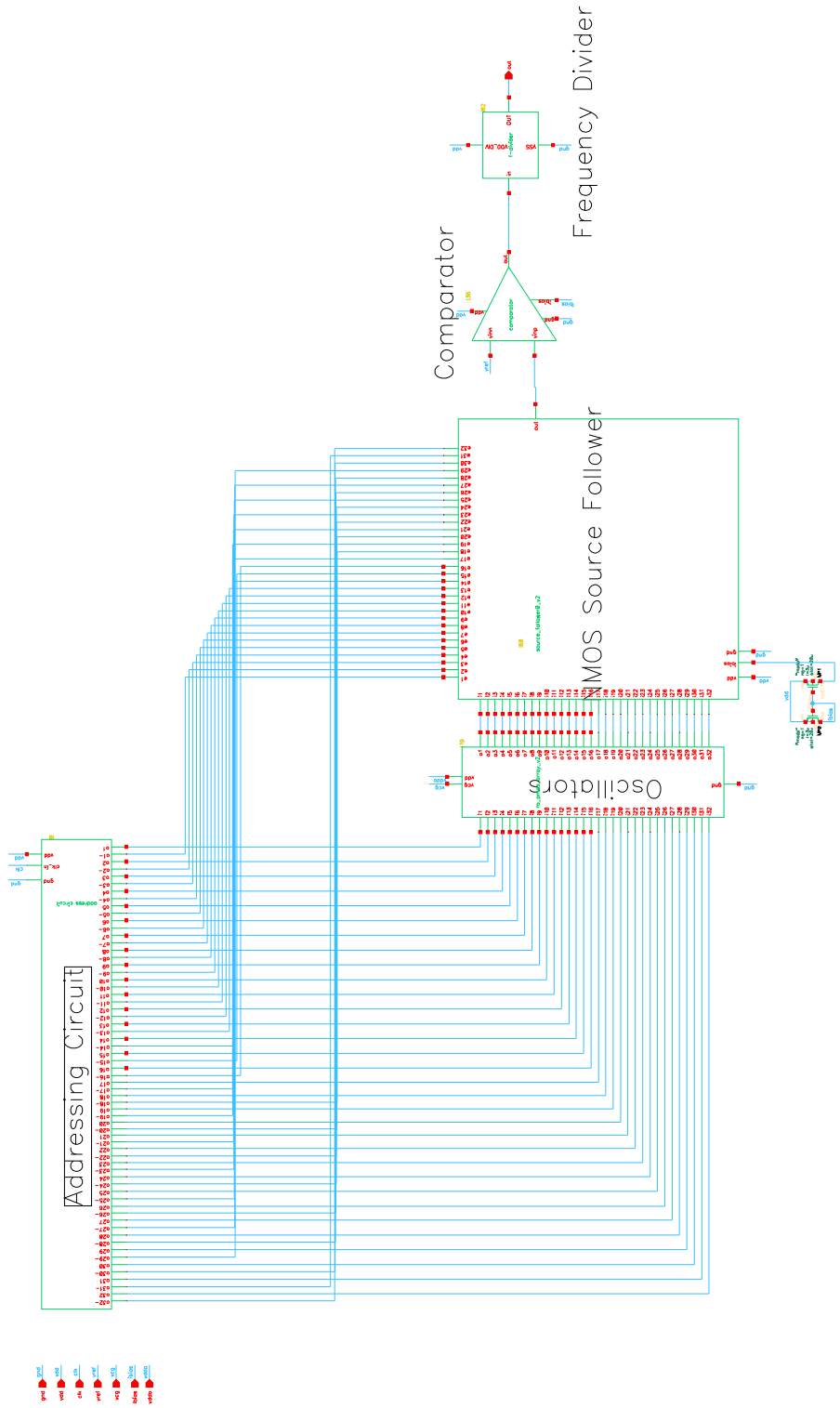
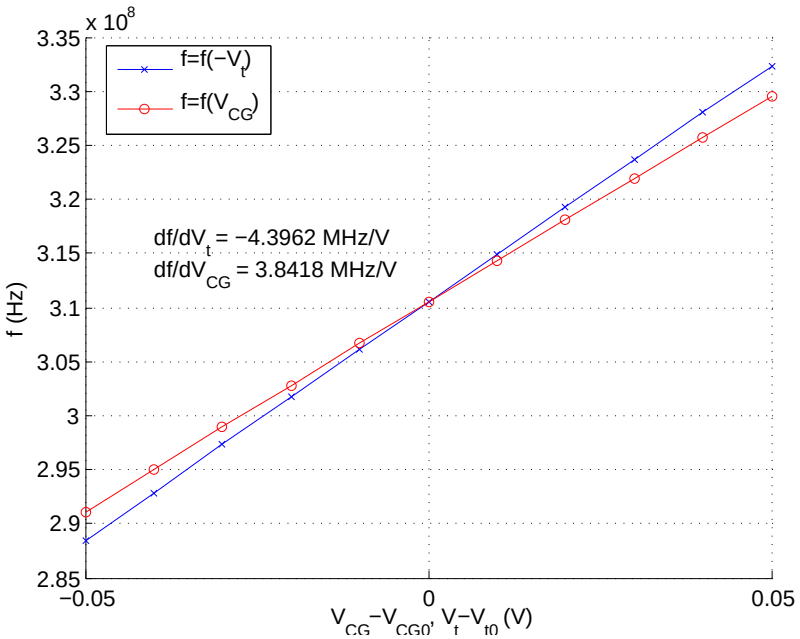
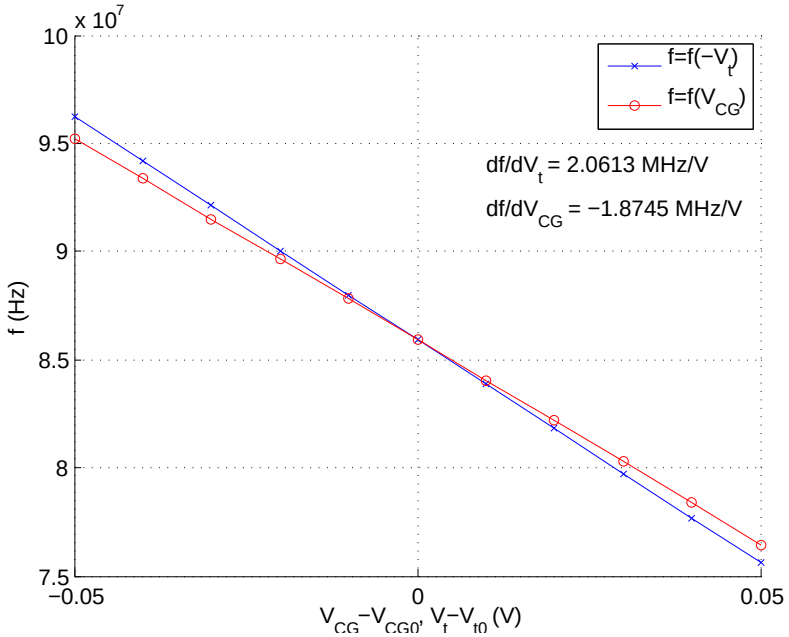


Figure 3.9: Complete circuit for measurement of PMOS threshold voltage variability.



(a) The frequency f is plotted as functions of V_{CG} and V_t for NMOS passgates. The proportionality factor k is $k = -0.874$.



(b) The frequency f is plotted as functions of V_{CG} and V_t for PMOS passgates. The proportionality factor k is $k = -0.909$.

Figure 3.10: Simulation results to determine k for PMOS and NMOS passgate.

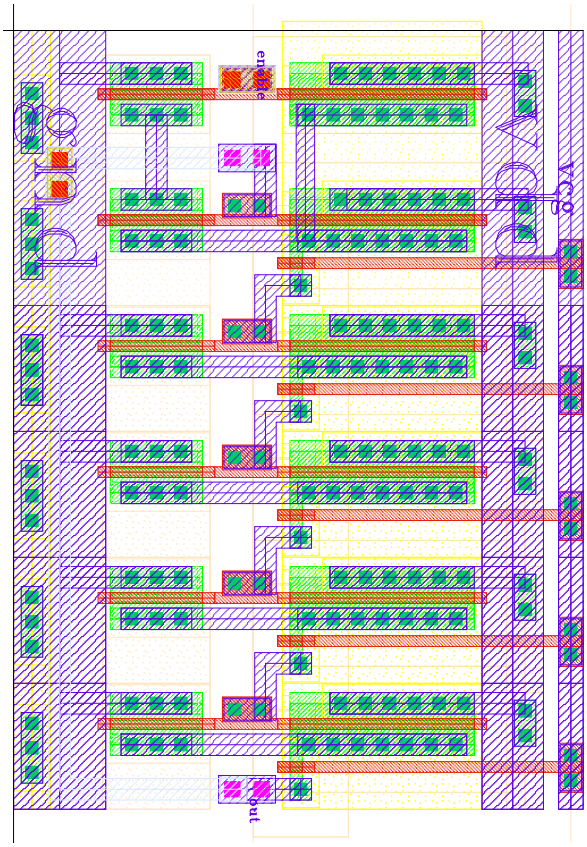
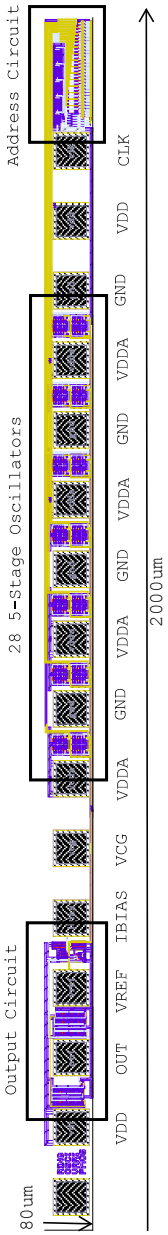


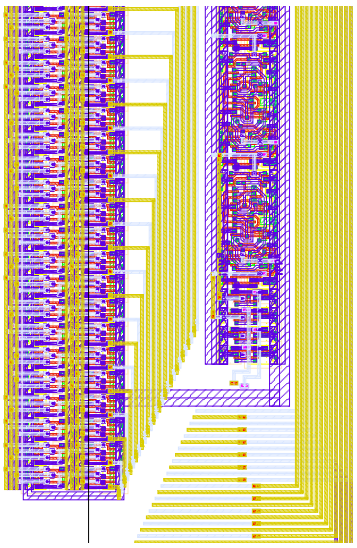
Figure 3.11: Layout of the ring oscillator with PMOS passgate.

Table 3.2: Pin description for the variability test chip

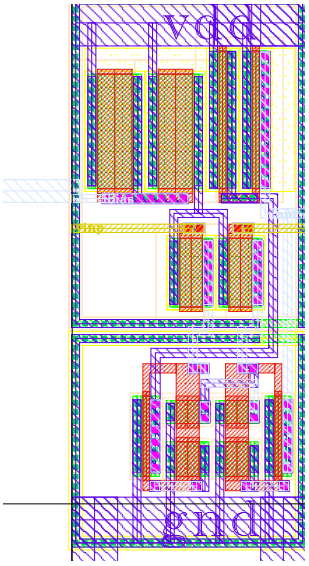
PAD	Description
GND	Ground connection; the separate pads are not connected on the chip itself
V_{DDA}	Supply pad for oscillators
V_{DD}	Supply pad for addressing and output circuit
V_{REF}	reference voltage for comparator
CLK	Clock signal used for addressing
V_{CG}	Connection to the gates of the load transistors
IBIAS	Bias current for source follower and comparator
OUT	Output pad at which frequency can be measured



(a) Layout of the test chip to measure PMOS threshold voltage variability.



(b) Layout of the address circuitry.



(c) Comparator with PMOS differential pair, layout.

Figure 3.12: Layout details of variability test chip

The clock input and the addressing circuit are placed all the way to the right of the layout structure to shield the oscillator stages from the digital input. Furthermore, the addressing circuit is quite big and the biggest space on the macro is on that side. Figure 3.12b shows the counter and the logic gates that decode the addresses. The space required for the routing of the 28 addresses can also be seen in this figure. The signal is decoupled with a source follower and fed to a comparator after the oscillators as illustrated in figure 3.12c. The frequency divider after that is the same one which is used for the CV measurement test chips.

3.4 Conclusion

The focus of chapter 3 was the feasibility of measuring the threshold voltage variability with ring oscillator circuits. A test chip was introduced and the methods described in the literature were analyzed. Only a relatively small number of oscillators could be placed on the test chip due to space restrictions posed by the scribe line. Even so, simulations predict a good agreement with the expected value. Measurements on the presented test chip are not included because at this point in time the wafers are still in production.

Chapter 4

High-Voltage Ring Oscillator Investigations

Ring oscillators are most commonly used to benchmark FET spice models. Therefore, the inverter stages are arranged in a ring structure without any additional loads. The resulting frequency is simulated and compared to measurements. Although two different devices influence the results – both PMOS and NMOS transistors in each inverter stage – this test is a good validation for the models. For the case that the simulation results fit closely to the measurement results conclusions are straightforward: the models correctly reproduce the actual behavior of the devices. The other case, where the simulation results differ from the measured values, is more complicated since there are different devices involved in the process. However, they indicate where problems exist and additional work needs to be done. As previously, the main advantage to other measurement methods is that the measurement is dynamic and more closely resembles operation on a product.
This chapter deals specifically with validating high voltage transistors. The difference compared to standard transistor devices is that the gate to drain region can withstand a much greater voltage than the gate to source region. Thus, the operating regions of the transistors in the oscillator will be determined by the maximum possible gate to source voltage. To start with, an investigation is conducted in section 4.1 to find out what the oscillation frequency is most sensitive to. In section 4.2 oscillators with different high voltage devices are introduced. The designs are simulated with both the BSIM3v3 [4] and HiSIM_HV [13] SPICE models to compare simulation results. These results are then compared to measurements on silicon.

4.1 Frequency Investigations

The following investigations are conducted with a device for which fairly significant deviations were found between BSIM3v3 subcircuit [14] and HiSIM_HV simulations. The results that preceded this investigation can be seen in figure 4.1. The difference between the two frequencies is around thirty percent.

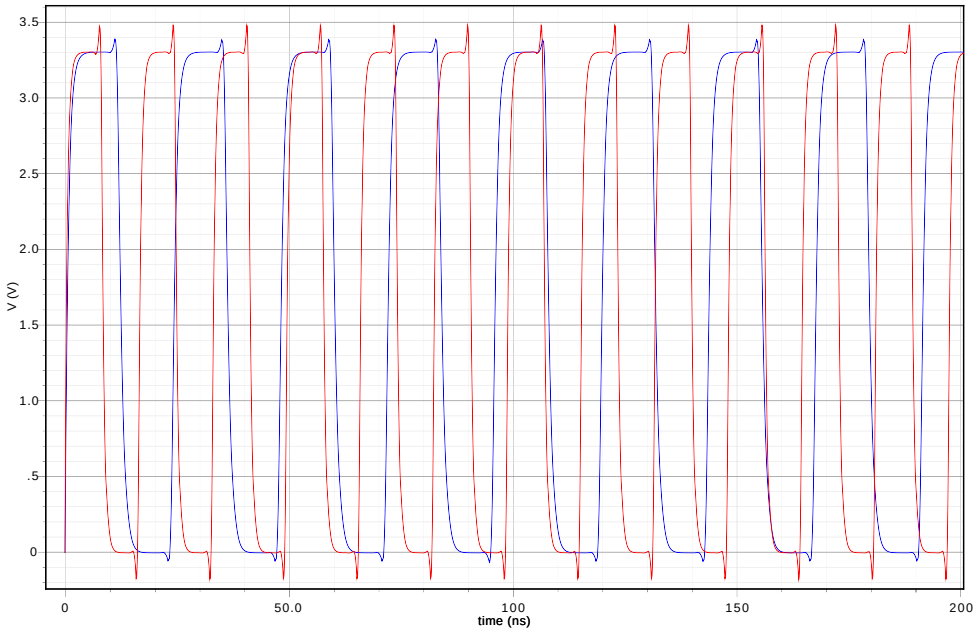


Figure 4.1: Comparison of the resulting waveform for a ring oscillator with NMOS50m devices for BSIM3v3 subcircuit and HiSIM_HV model. red...BSIM3v3; blue...HiSIM_HV.

To begin with, the gate capacitance and the overlap capacitance of the models are compared. As it turns out, there is a problem for the gate capacitance of the NMOS device: the BSIM3v3 subcircuit simulation yields a cgg which is about forty percent smaller than the HiSIM_HV model result as shown in figure 4.2. The overlap capacitance and the capacitance values for the PMOS device are in an acceptable range as can be seen in figures C.1, C.2, and C.3 on pages 103 to 104).
Due to this deviation, two parameters that influence the gate capacitance are investigated, namely **dlc** – the length offset parameter which influences the intrinsic capacitance – and **cgdx** – a capacitance that is added in parallel to the gate to drain region in the subcircuit. The change of the gate capacitance with these two parameters can be seen in figures 4.3 and 4.4. Although both parameters influence the overlap capacitance in a different way, as illustrated in figures C.4 and C.5, the change is almost the same in the region of interest ($0 < V_{\mathrm{GS}} < 3.3V$). Furthermore, separate simulations with a 10% bigger **ron** of the BSIM3v3 subcircuit are performed for each parameter set. **ron** is the resistance of the device when it is turned on. The result, however, is only a minimal decrease of the frequency. Figure 4.5 shows the resulting waveforms. The curve pairs that lie close together have the same capacitance parameters but different **ron**.

Compared to the original set, increasing **dlc** equalizes the overlap capacitance of the two models, which can be found in the regions where the capacitance changes little in the cgg plots. Yet, the characteristic around zero volt gate voltage in figure 4.3 is only slightly increased to the characteristic in figure 4.2. Since the voltage at the gate oscillates between zero and three volts, this region still has a major impact on the frequency. Re-simulating the ring oscillator with the two models shows that the BSIM3v3 subcircuit result is still

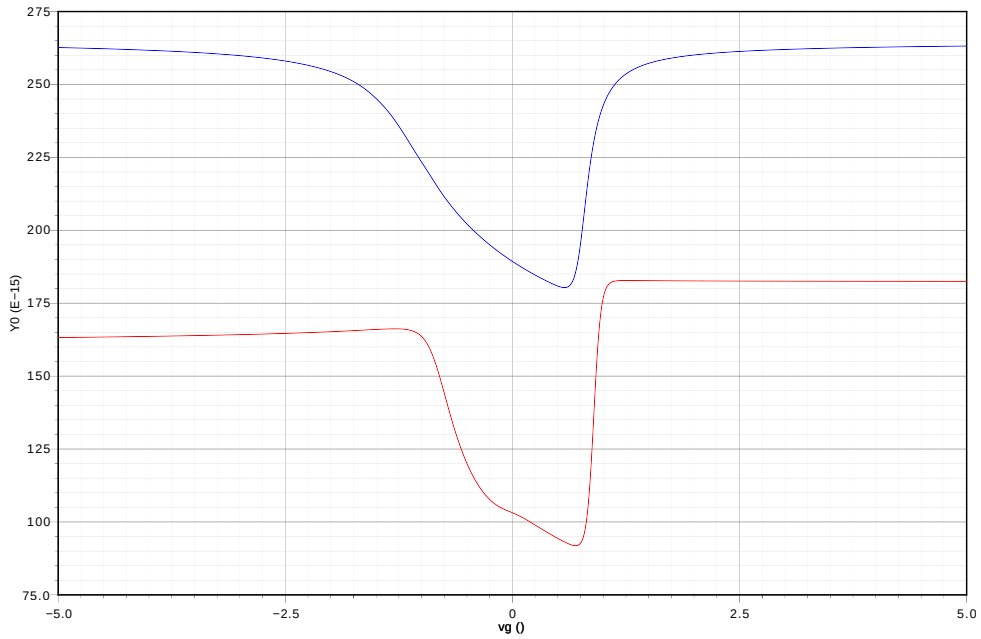


Figure 4.2: Comparison of the total gate capacitance of the NMOS50m for BSIM3v3 subcircuit and HiSIM_HV model. red...BSIM3v3; blue...HiSIM_HV; ordinate Y0...Capacitance (F).

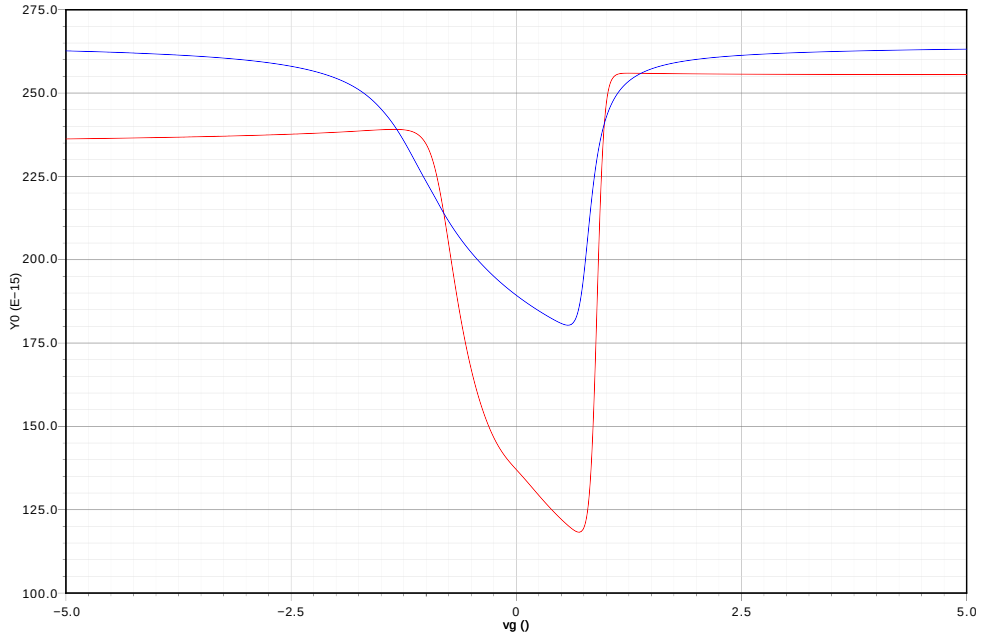


Figure 4.3: Comparison of the total gate capacitance of the NMOS50m for BSIM3v3 subcircuit and HiSIM_HV model. The parameter **dlc** of the BSIM3v3 subcircuit is adjusted. red...BSIM3v3dlc; blue...HiSIM_HV; ordinate Y0...Capacitance (F).

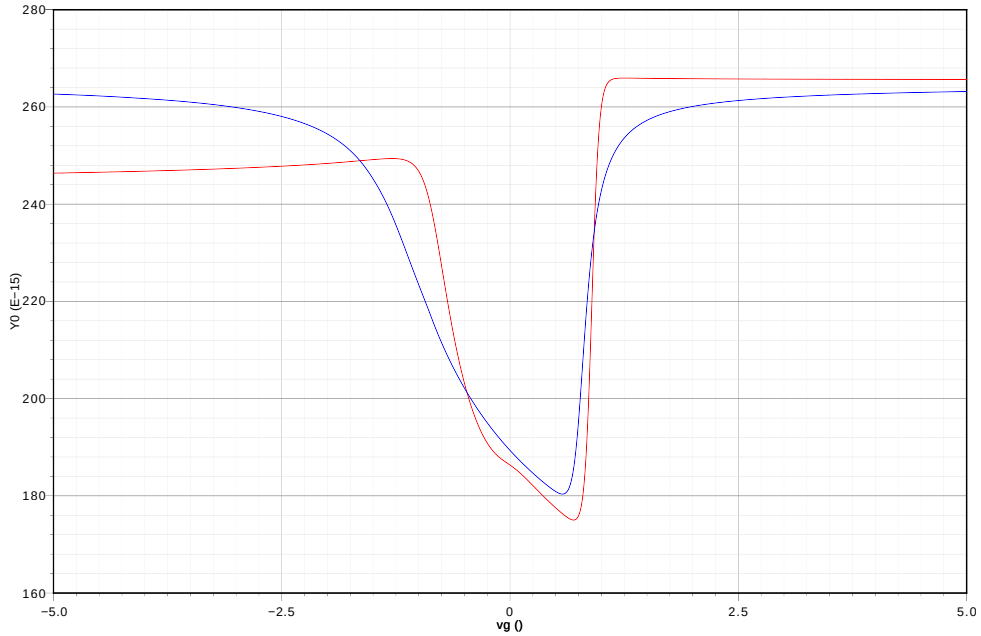


Figure 4.4: Comparison of the total gate capacitance of the NMOS50m for BSIM3v3 subcircuit and HiSIM_HV model. The parameter **cgdx** of the BSIM3v3 subcircuit is adjusted. red...BSIM3v3cgdx; blue...HiSIM_HV; ordinate Y0...Capacitance (F).

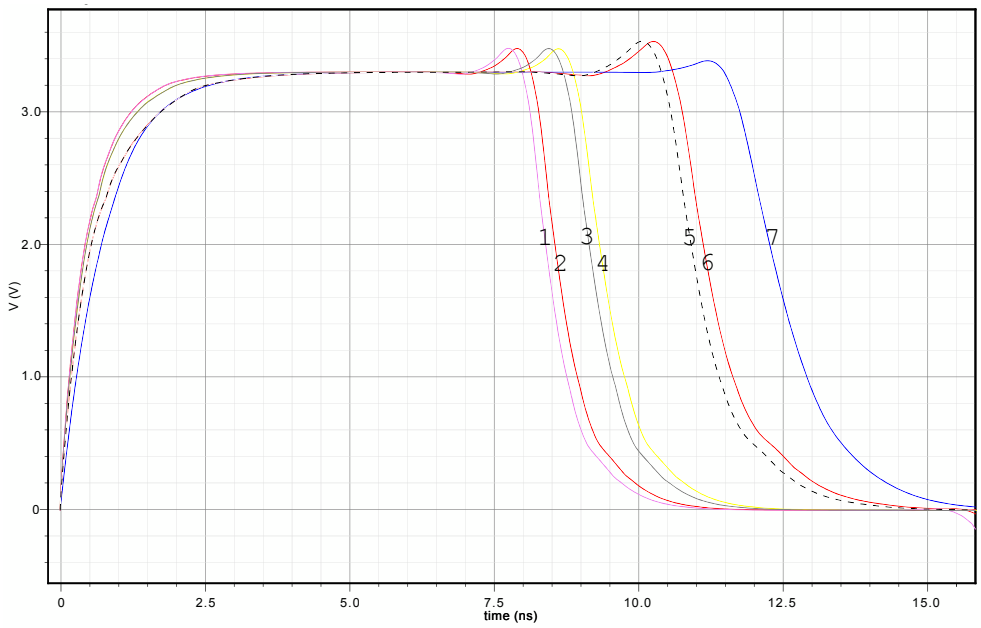


Figure 4.5: Comparison of the influence of different parameters on the frequency. Additionally **ron** is changed for each parameter set of the BSIM3v3 subcircuit. **ron** has only a minor influence on the frequency in this case. The results lie very close to the curves obtained with the original **ron**. 1...BSIM3v3; 2...BSIM3v3**ron**; 3...BSIM3v3dlc; 4...BSIM3v3dlc**ron**; 5...BSIM3v3cgdx; 6...BSIM3v3cgdx**ron**; 7...HiSIM_HV.

Table 4.1: Ring oscillator dimensions.

Device	Description	width	length	Designator
		μm	μm	
NMOSi50t	50V transistor with a thin oxide (7nm)	20	1	i50t
PMOS50t	50V transistor with a thin oxide (7nm)	40	1	
NMOSi50t	50V transistor with a thin oxide (7nm)	10	0.5	i50tmin
PMOS50t	50V transistor with a thin oxide (7nm)	10	1	
NMOS50m	50V transistor with a mid oxide (15nm)	20	1	50m
PMOS50m	50V transistor with a mid oxide (15nm)	40	1	
NMOSi20t	20V transistor with a thin oxide (7nm)	20	0.7	i20t
PMOS20t	20V transistor with a thin oxide (7nm)	40	0.7	

far from the HiSIM_HV model result. **cgdx**, on the other hand, raises the complete curve so that the two gate capacitance simulations basically overlap. This moves the BSIM3v3 subcircuit result quite close to the HiSIM_HV model result: the difference is now only about 10 percent. These results are shown in figure 4.5. 10% would be an acceptable difference between the two models. Although **cgdx** also changes cgd and other values, it happens in an operating region that is not traversed in the simulation.
As conclusion of this investigation, it can be said that the most significant parameter for the frequency is the gate capacitance. Such is the case for the high voltage transistors, which do not traverse through all of their operating regions due to the fact that the gate voltage cannot go to such high values as the drain would permit. And as each inverter pulls the next gate up or down to the respective supply, the maximum allowed voltage is determined by the gate. These investigations were performed without assuming that one or the other model more accurately resembles measured values.

4.2 Simulation and Measurement Results

In this section simulation results for four different ring oscillators will be presented and the BSIM3v3 subcircuit and HiSIM_HV model compared. The oscillators are built up of only eleven stages as high voltage transistors by themselves occupy a large area. Table 4.1 shows the used devices and their dimensions. Two oscillators are built with the same transistors yet with different dimensions. For the first one, the PMOS width is twice the width of the NMOS device to make their driving capabilities similar. For the second one, minimum sized devices are used.

The layout of of the 50m oscillator is shown in figure 4.6. The oscillator's eleven stages and the frequency divider can be seen. Furthermore, the pad arrangement is given. The pad arrangement and frequency divider are the same for all oscillators, even though the oscillator's transistors are placed in slightly different ways. The size of all oscillator test structures, however, is approximately the same.

Table 4.2 shows the simulation and measurement results. The simulations were performed with schematics and additionally with parasitics extracted from the layouts. First of

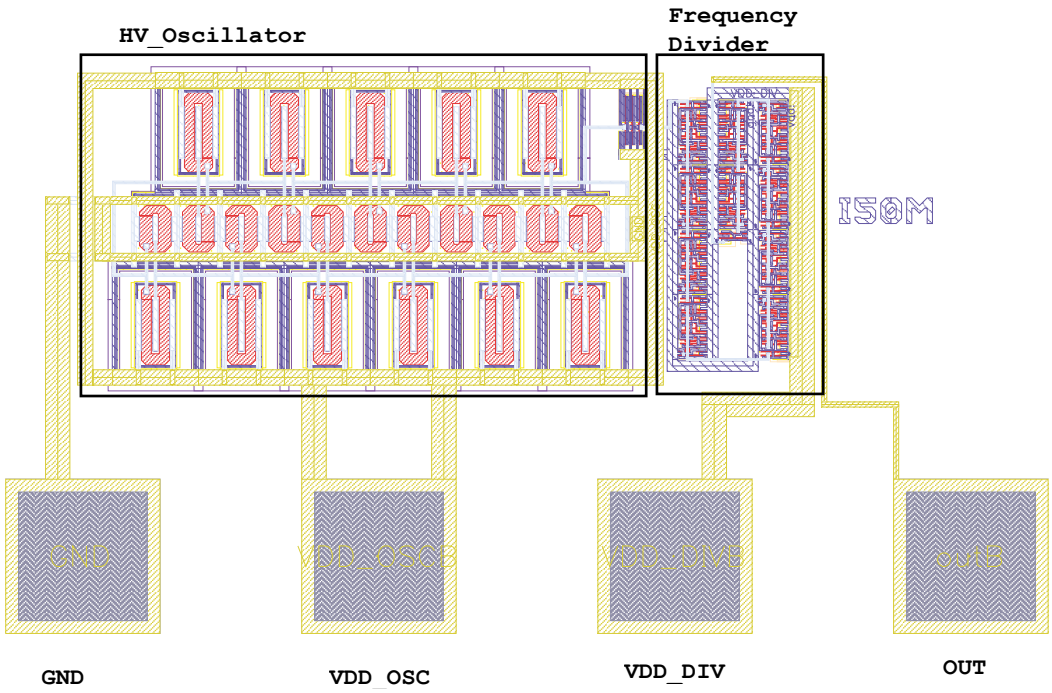


Figure 4.6: Layout of HV oscillator with NMOS50m and PMOS50m transistors. GND ... ground pad; VDD_{DIV} ... supply voltage for divider; VDD_{OSC} ... supply voltage for oscillator; OUT ... output pad.

all, HiSIM_HV simulations yield generally smaller frequencies than the BSIM3v3 models. Furthermore, the results for the i50t and i20t structures fit very well. Both frequencies for BSIM3v3 and HiSIM_HV are not too far apart, and in case of the parasitic extract, fairly close to the measured values. However, here the first problem arises: looking at the i50tmin structure, one would expect the measured frequency to increase as the overall capacitances decrease. Yet the measurement goes in the opposite direction and yields a much smaller frequency compared to the i50t oscillator. Basically two steps need to be taken here: first the measurement must be repeated to verify that this is indeed the correct result. Then the output characteristic needs to be investigated for minimum devices. The PMOS in this case is a lot weaker than the NMOS and might slow the whole structure down. As the i50t structure is pretty close to the measurement, the capacitance model is assumed to be correct. For the 50m structure the thirty percent difference between BSIM3v3 and HiSIM_HV that has been observed before can be seen. The BSIM3v3 model lies closer to the measurement in this case.

4.3 Conclusion

Chapter 4 gave a quick overview of how ring oscillator structures can be used to benchmark models and highlight potential problems. Although one cannot easily deduce where these

Table 4.2: Simulation and measurement results.

Designator	BSIM3v3	HiSIM_HV	BSIM3v3	HiSIM_HV	Measurement
	Schematic	Schematic	Layout	Layout	
	MHz	MHz	MHz	MHz	MHz
i50t	51.0	50.05	48.6	48.0	42.5
i50tmin	62.7	56.74	56.7	52.7	39.4
50m	60.5	41.46	56.9	39.9	51.1
i20t	118	111	110	104	113

problems lie, it is then possible to focus on specific models for improvement. Compared to the first two measurement methods described in this thesis, here simply the frequency is measured. No additional loads or reference oscillators are required. Therefore, the design and layout are fairly straightforward. As in chapter 2 the optimum would be a high number of oscillator stages to smooth over random variations that occur from device to device. Yet, high voltage transistors are relatively big compared to standard devices and thus these oscillators comprise only eleven stages. Nonetheless, useful results were obtained.

Chapter 5

Summary

The focus of this thesis was measurements on ring oscillator structures. In Chapter 2 their application for parameter measurements was investigated. Based on available literature, measurement methods to extract specifically the overlap capacitance and oxide thickness were introduced and the required test structures designed and evaluated. Good agreement was found between measurements and simulation.
The topic of Chapter 3 was to measure the variation of parameters, particularly the variation of the threshold voltage. Existing literature was researched and its suitability for the available technology investigated with the help of simulations. A circuit implementation and layout were presented.
Finally, Chapter 4 described the use of ring oscillators as benchmark structures, in this particular case for high voltage transistors. Four ring oscillators were introduced for which simulations with two compact models were performed and compared to measurement data. Therefore, special test structures were designed and realized on silicon.
It was shown that ring oscillators can indeed be used to extract specific device properties by measuring frequencies and currents with standard measurement equipment.

Bibliography

[1] M. Bhushan, A. Gattiker, M. Ketchen, and K. Das, "Ring oscillators for cmos process tuning and variability control," *Semiconductor Manufacturing, IEEE Transactions on*, vol. 19, no. 1, pp. 10 – 18, feb. 2006.

[2] M. Ketchen, M. Bhushan, and D. Pearson, "High speed test structures for in-line process monitoring and model calibration [cmos applications]," in *Microelectronic Test Structures, 2005. ICMTS 2005. Proceedings of the 2005 International Conference on*, april 2005, pp. 33 – 38.

[3] M. Bhushan, M. Ketchen, M. Cai, and C. Kim, "Ring oscillator technique for mosfet cv characterization," *Semiconductor Manufacturing, IEEE Transactions on*, vol. 21, no. 2, pp. 180 –185, may 2008.

[4] Y. Cheng *et al.*, *BSIM3v3 Manual*, University of California, Berkeley, CA94720, 1996.

[5] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design.* Oxford University Press, 2002.

[6] W. Press, S. Teukolsky, W. Vetterling, and B. Flannery, *Numerical Recipes in C.* Cambridge University Press, 1992.

[7] *Agilent 4155C Semiconductor Parameter Analyzer, Agilent 4156C Precision Semiconductor Parameter Analyzer, User's Guide*, 11th ed., Agilent Technologies, Inc., 5301 Stevens Creek Blvd, Santa Clara, CA 95051 USA, July 2009.

[8] *User's Guide Volume 2, Measurement and Analysis, Agilent 4155C Semiconductor Parameter Analyzer, Agilent 4156C Precision Semiconductor Parameter Analyzer*, 5th ed., Agilent Technologies, Inc., 5301 Stevens Creek Blvd, Santa Clara, CA 95051 USA, August 2003.

[9] *5334A/B Universal Counter Operating and Programming Manual*, Agilent Technologies, Inc., 5301 Stevens Creek Blvd, Santa Clara, CA 95051 USA, December 1993.

[10] Wikipedia. (2012) Interquartile range — wikipedia, the free encyclopedia. [accessed 17-July-2012]. [Online]. Available: http://en.wikipedia.org/w/index.php?title=Interquartile_range&oldid=500614503

[11] M. Bhushan, M. Ketchen, S. Polonsky, and A. Gattiker, "Ring oscillator based technique for measuring variability statistics," in *Microelectronic Test Structures, 2006. ICMTS 2006. IEEE International Conference on*, march 2006, pp. 87 – 92.

[12] R. Gregorian, *Introduction to CMOS OP-AMPs and comparators*, ser. A Wiley-Interscience publication. Wiley, 1999.

[13] N. Sadachika *et al.*, *HiSIM_HV 1.0.2, Version 1.02 User's Manual*, Hiroshima University and STARC, 2008.

[14] P. Werner, "Measurement and modelling of high-voltage mos field effect transistors," Master's thesis, Institute of Solid-State Physics, Technical University Graz, 2002.

Appendix A

CV Characterization

A.1 Simulation Environment

```
function [] = writehead(fid);



s='//HEADER:   RO simulation for Spectre';
fprintf(fid,'%s\n',s);
s='simulator lang=spectre';
fprintf(fid,'%s\n',s);
s='global 0 psub! vss! vdd! vcg!';
fprintf(fid,'%s\n',s);
s='include
"/fsup04/prglnx/cds/IC5.1.41USR6ISR2/tools/dfII/samples/artist/ahdlLib/qu
antity.spectre"';
fprintf(fid,'%s\n',s);
s='include "/programs/ams_develop/spectre/c35/soac/C35B4C0.scs"';
fprintf(fid,'%s\n',s);
s='include "/programs/ams_develop/spectre/c35/soac/cap.scs"
section=capmc';
fprintf(fid,'%s\n',s);
s='include "/programs/ams_develop/spectre/c35/soac/res.scs"
section=resmc';
fprintf(fid,'%s\n',s);
s='include "/programs/ams_develop/spectre/c35/soac/bip.scs"
section=bipmc';
fprintf(fid,'%s\n',s);
s='include "./cmos53_ov.scs" section=cmosmc';
fprintf(fid,'%s\n',s);
s='//END HEADER';
fprintf(fid,'%s\n\n\n',s);
```

```
function [] = writeNet_ov_nand(fid,n);
%
% puts together a Netlist for the ring oscillator
% Includes enable NAND gate and a buffer Capacitance
%
C= 10e-6;
s='//Netlist for n RO stages';
fprintf(fid,'%s\n\n',s);
for j = 1 : n
       i = num2str(j);
       if j < 10
            i= ['0' i];
       end;
       ii= num2str(j+1);
       if j < 9
            ii = [ '0' ii ];
       end;
       if j == n
            ii='b';
       end;
       s= ['M' i ' (vdd! vss! psub! vcg! net' i ' net' ii ') invcell' ];
       fprintf(fid,'%s\n',s);
end;

s='V1 (vss!  0) vsource dc=vss type=dc';
fprintf(fid,'%s\n',s);
s='V2 (vdd!  0) vsource dc=vdd type=dc';
fprintf(fid,'%s\n',s);
s='V3 (psub! 0) vsource dc=psub type=dc';
fprintf(fid,'%s\n',s);
s='V4 (vcg! 0) vsource dc=vcg type=dc';
fprintf(fid,'%s\n',s);
s='V5 (a 0) vsource dc=vdd type=pwl wave=[0 0 1n 0 1.1n 3.3 1m 3.3]';
fprintf(fid,'%s\n',s);
s=['C1 (vdd! 0) capacitor c=' num2str(C) '  m=1'];
fprintf(fid,'%s\n',s);

s='M_subinst_nand_01 (net01 netb k psub!) modn \';
fprintf(fid,'%s\n',s);
s='w=wnu/1 l=lnu ng=1 \';
fprintf(fid,'%s\n',s);
s='as=(8.5e-07*wnu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wnu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ad=(8.5e-07*wnu/1*fmod(1,2)+int(1/2)*2*5e-07*wnu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ps=((2*8.5e-07+wnu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='pd=((2*8.5e-07+wnu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='nrd=5e-07/wnu/1 nrs=5e-07/wnu/1 mmvth=0 mmu0=0 \';
fprintf(fid,'%s\n\n',s);

s='M_subinst_nand_02 (k a vss! psub!) modn \';
fprintf(fid,'%s\n',s);
s='w=wnu/1 l=lnu ng=1 \';
fprintf(fid,'%s\n',s);
s='as=(8.5e-07*wnu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wnu/1)/1 \';
fprintf(fid,'%s\n',s);
```

```
s='ad=(8.5e-07*wnu/1*fmod(1,2)+int(1/2)*2*5e-07*wnu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ps=((2*8.5e-07+wnu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='pd=((2*8.5e-07+wnu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='nrd=5e-07/wnu/1 nrs=5e-07/wnu/1 mmvth=0 mmu0=0\';
fprintf(fid,'%s\n\n',s);

s='M_subinst_nand_03 (net01 a vdd! vdd! ) modp  \';
fprintf(fid,'%s\n',s);
s='w=0.4e-6/1 l=0.35e-6 \';
fprintf(fid,'%s\n',s);
s='ng=1 as=(8.5e-07*0.4e-6/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*0.4e-
6/1)/1 \';
fprintf(fid,'%s\n',s);
s='ad=(8.5e-07*0.4e-6/1*fmod(1,2)+int(1/2)*2*5e-07*0.4e-6/1)/1 \';
fprintf(fid,'%s\n',s);
s='ps=((2*8.5e-07+0.4e-6/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='pd=((2*8.5e-07+0.4e-6/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='nrd=5e-07/0.4e-6/1 nrs=5e-07/0.4e-6/1  mmvth=0 mmu0=0\';
fprintf(fid,'%s\n\n',s);

s='M_subinst_nand_04 (net01 netb vdd! vdd! ) modp  \';
fprintf(fid,'%s\n',s);
s='w=wpu/1 l=lpu \';
fprintf(fid,'%s\n',s);
s='ng=1 as=(8.5e-07*wpu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wpu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ad=(8.5e-07*wpu/1*fmod(1,2)+int(1/2)*2*5e-07*wpu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ps=((2*8.5e-07+wpu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='pd=((2*8.5e-07+wpu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='nrd=5e-07/wpu/1 nrs=5e-07/wpu/1  mmvth=0 mmu0=0\';
fprintf(fid,'%s\n\n',s);

s='M_subinst_nand_05 (net01 vcg! net01 vdd! psub!) modp_load  \';
fprintf(fid,'%s\n',s);
s='w=wplu/1 l=lplu \';
fprintf(fid,'%s\n',s);
s='ng=1 as=(8.5e-07*wplu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wplu/1)/1
\';
fprintf(fid,'%s\n',s);
s='ad=(8.5e-07*wplu/1*fmod(1,2)+int(1/2)*2*5e-07*wplu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ps=((2*8.5e-07+wplu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='pd=((2*8.5e-07+wplu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='nrd=5e-07/wplu/1 nrs=5e-07/wplu/1  mmvth=0 mmu0=0 extracted=1\';
fprintf(fid,'%s\n\n',s);

s='ic net01=3.3' ;
fprintf(fid,'%s\n\n',s);
```

```
function [] = writeStage1OV(fid,par1,par2);
%
% creates one inverter stage for the ring oscillator
%

vss = par1(1);
vdd = par1(2);
temp= par1(3);
wn  = par1(4);
ln  = par1(5);
wp  = par1(6);
lp  = par1(7);

wpl = par2(1);
lpl = par2(2);
vcg = par2(3);
psub = par2(4);

s='//SUBCIRCUIT for RO Stage';
fprintf(fid,'%s\n\n',s);

s=[ 'parameters wpu=' num2str(wp) ' lpu=' num2str(lp) ' wnu=' num2str(wn)
' lnu=' num2str(ln) ' vss=' num2str(vss) ' vdd=' num2str(vdd) ' wplu='
num2str(wpl) ' lplu=' num2str(lpl) ' vcg=' num2str(vcg) ' psub='
num2str(psub)];
fprintf(fid,'%s\n\n',s);
s='subckt invcell p n psub vcg in out';
fprintf(fid,'%s\n\n',s);
s='M_subinst_01 (out in p p ) modp  \';
fprintf(fid,'%s\n',s);
s='w=wpu/1 l=lpu \';
fprintf(fid,'%s\n',s);
s='ng=1 as=(8.5e-07*wpu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wpu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ad=(8.5e-07*wpu/1*fmod(1,2)+int(1/2)*2*5e-07*wpu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ps=((2*8.5e-07+wpu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='pd=((2*8.5e-07+wpu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='nrd=5e-07/wpu/1 nrs=5e-07/wpu/1  mmvth=0 mmu0=0 \';
fprintf(fid,'%s\n\n',s);


s='M_subinst_02 (out in n psub) modn \';
fprintf(fid,'%s\n',s);
s='w=wnu/1 l=lnu ng=1 \';
fprintf(fid,'%s\n',s);
s='as=(8.5e-07*wnu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wnu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ad=(8.5e-07*wnu/1*fmod(1,2)+int(1/2)*2*5e-07*wnu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ps=((2*8.5e-07+wnu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='pd=((2*8.5e-07+wnu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='nrd=5e-07/wnu/1 nrs=5e-07/wnu/1 mmvth=0 mmu0=0 \';
fprintf(fid,'%s\n\n',s);
```

```
s='M_subinst_03 (out vcg out p psub ) modp_load  \';
fprintf(fid,'%s\n',s);
s='w=wplu/1 l=lplu \';
fprintf(fid,'%s\n',s);
s='ng=1 as=(8.5e-07*wplu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wplu/1)/1
\';
fprintf(fid,'%s\n',s);
s='ad=(8.5e-07*wplu/1*fmod(1,2)+int(1/2)*2*5e-07*wplu/1)/1 \';
fprintf(fid,'%s\n',s);
s='ps=((2*8.5e-07+wplu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='pd=((2*8.5e-07+wplu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \';
fprintf(fid,'%s\n',s);
s='nrd=5e-07/wplu/1 nrs=5e-07/wplu/1  mmvth=0 mmu0=0 extracted=1\';
fprintf(fid,'%s\n\n',s);

s='ends invcell';
fprintf(fid,'%s\n\n\n',s);
```

```
function [] = writeOptions_ov(fid,parsim,pth, name);

tmp = parsim(1);
time= parsim(2);


s='//SIMULATOR OPTIONS ************************************';
fprintf(fid,'%s\n\n',s);
s='simulatorOptions options reltol=1e-6 vabstol=1.0e-6 iabstol=0.1e-12
\';
fprintf(fid,'%s\n',s);
s='tnom=27 homotopy=all limit=delta scalem=1.0 scale=1.0 \';
fprintf(fid,'%s\n',s);
s='compatible=spice2 gmin=1e-18 rforce=1.0 maxnotes=5 maxwarns=5 digits=5
\';
fprintf(fid,'%s\n',s);
s=' cols=80 pivrel=1e-3 sensfile="./sens.output" checklimitdest=psf \';
fprintf(fid,'%s\n',s);
s=['temp=' num2str(tmp)];
fprintf(fid,'%s\n',s);
s=['tran tran stop=' num2str(time) ' saveperiod=' num2str(time./10000) '
\'];
fprintf(fid,'%s\n',s);
s=['savefile="' pth name 'raw.raw" errpreset=conservative
write="spectre.ic" \'];
fprintf(fid,'%s\n',s);

s='writefinal="spectre.fc" annotate=status maxiters=50';
fprintf(fid,'%s\n',s);
s=['operatingpoint info what=oppoint where=file'];
fprintf(fid,'%s\n',s);
s=['deviceparameters info what=parameters where=file'];
fprintf(fid,'%s\n',s);
s=['netlist info what=netlist where=file'];
fprintf(fid,'%s\n\n',s);
```

```
function []= overlap_design()


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% filename /fsup04/fuxrdu/jry/diplomarbeit/spectre_ro/simulated_data;
% structure:
% vss vdd temp wn ln wp lp vsp i f [additional parameters specifying
% load
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

name1 = 'overlap_pmos_matching';
pth= ['./' name1 '/'];
evstr = ['! mkdir ' pth]';
eval(evstr);

fname_data = [pth name1 '.txt'];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% Definition of operating conditions and geometry of the ring oscillators
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

vss = 0.0;
vdd=3.3;
temp=27;
wn=1e-06;
ln=0.35e-06;
wp=2.5e-6;
lp=0.35e-06;

wpl = [1e-6 2e-6];
lpl = [0.35e-6];
vcg = [3.3];
psub=0.0;
n= 40;

par1=[vss, vdd, temp, wn, ln, wp, lp];
cd = [5e-13, 0.6e-12];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% loop in which the netlist for each ro is created and fed to spectre
% the results from spectre are read and analyzed
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

for iii= 1:length(vcg)
      for i = 1:length(wpl)
            for ii = 1:length(lpl)

%%%%%%% definition of the timeinterval to be simulated      %%%%%

      timeint= 0.025e7*cd(i);

%%%%%%% filename under which result will be saved           %%%%%
```

```
      name = [name1 '_' num2str(i)];

%%%%%%% name of netlist                                          %%%%%
      fname= [ pth name '.scs' ];

      par2=[wpl(i), lpl(ii), vcg(iii),psub];
      parsim=[ temp, timeint ];

%%%%%%% simulation of reference oscillator                       %%%%%

      ro_unloaded_ov(par1,par2,pth,name1,name,timeint,n);

%%%%%%% Netlist mos load                                         %%%%%

      fid = fopen(fname,'w');

      writehead_ov(fid);
      writeStage1OV(fid,par1,par2);
      writeNet_ov_nand(fid,n);
      writeOptions_ov_matching(fid,parsim,pth ,name);
      fclose(fid);

%%%%%%% handover to spectre                                     %%%%%

      evstr = [ '! spectre -format wsfascii +mt ' fname ];
      eval(evstr);


%%%%%%% parameter extraction from the simulated data            %%%%%

      getdataoverlap(pth, name,fname_data,par1,par2);


        end;
      end;
end;
```

```
//HEADER:   RO simulation for Spectre
simulator lang=spectre
global 0 psub! vss! vdd! vcg!
include
"/fsup04/prglnx/cds/IC5.1.41USR6ISR2/tools/dfII/samples/artist/ahdlLib/qu
antity.spectre"
include "/programs/ams_develop/spectre/c35/soac/C35B4C0.scs"
include "/programs/ams_develop/spectre/c35/soac/cap.scs" section=captm
include "/programs/ams_develop/spectre/c35/soac/res.scs" section=restm
include "/programs/ams_develop/spectre/c35/soac/bip.scs" section=biptm
include "./cmos53_ov.scs" section=cmostm
//END HEADER


//SUBCIRCUIT for RO Stage

parameters wpu=2.5e-06 lpu=3.5e-07 wnu=1e-06 lnu=3.5e-07 vss=0 vdd=3.3
wplu=1e-06 lplu=3.5e-07 vcg=3.3 psub=0

subckt invcell p n psub vcg in out

M_subinst_01 (out in p p ) modp  \
w=wpu/1 l=lpu \
ng=1 as=(8.5e-07*wpu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wpu/1)/1 \
ad=(8.5e-07*wpu/1*fmod(1,2)+int(1/2)*2*5e-07*wpu/1)/1 \
ps=((2*8.5e-07+wpu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \
pd=((2*8.5e-07+wpu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \
nrd=5e-07/wpu/1 nrs=5e-07/wpu/1  mmvth=0 mmu0=0 \

M_subinst_02 (out in n psub) modn \
w=wnu/1 l=lnu ng=1 \
as=(8.5e-07*wnu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wnu/1)/1 \
ad=(8.5e-07*wnu/1*fmod(1,2)+int(1/2)*2*5e-07*wnu/1)/1 \
ps=((2*8.5e-07+wnu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \
pd=((2*8.5e-07+wnu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \
nrd=5e-07/wnu/1 nrs=5e-07/wnu/1 mmvth=0 mmu0=0 \

M_subinst_03 (out vcg out p psub ) modp_load  \
w=wplu/1 l=lplu \
ng=1 as=(8.5e-07*wplu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wplu/1)/1 \
ad=(8.5e-07*wplu/1*fmod(1,2)+int(1/2)*2*5e-07*wplu/1)/1 \
ps=((2*8.5e-07+wplu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \
pd=((2*8.5e-07+wplu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \
nrd=5e-07/wplu/1 nrs=5e-07/wplu/1  mmvth=0 mmu0=0 extracted=1\

ends invcell


//Netlist for n RO stages

M01 (vdd! vss! psub! vcg! net01 net02) invcell
M02 (vdd! vss! psub! vcg! net02 net03) invcell
M03 (vdd! vss! psub! vcg! net03 net04) invcell
M04 (vdd! vss! psub! vcg! net04 net05) invcell
M05 (vdd! vss! psub! vcg! net05 net06) invcell
M06 (vdd! vss! psub! vcg! net06 net07) invcell
M07 (vdd! vss! psub! vcg! net07 net08) invcell
M08 (vdd! vss! psub! vcg! net08 net09) invcell
```

```
M09 (vdd! vss! psub! vcg! net09 net10) invcell
M10 (vdd! vss! psub! vcg! net10 net11) invcell
M11 (vdd! vss! psub! vcg! net11 net12) invcell
M12 (vdd! vss! psub! vcg! net12 net13) invcell
M13 (vdd! vss! psub! vcg! net13 net14) invcell
M14 (vdd! vss! psub! vcg! net14 net15) invcell
M15 (vdd! vss! psub! vcg! net15 net16) invcell
M16 (vdd! vss! psub! vcg! net16 net17) invcell
M17 (vdd! vss! psub! vcg! net17 net18) invcell
M18 (vdd! vss! psub! vcg! net18 net19) invcell
M19 (vdd! vss! psub! vcg! net19 net20) invcell
M20 (vdd! vss! psub! vcg! net20 net21) invcell
M21 (vdd! vss! psub! vcg! net21 net22) invcell
M22 (vdd! vss! psub! vcg! net22 net23) invcell
M23 (vdd! vss! psub! vcg! net23 net24) invcell
M24 (vdd! vss! psub! vcg! net24 net25) invcell
M25 (vdd! vss! psub! vcg! net25 net26) invcell
M26 (vdd! vss! psub! vcg! net26 net27) invcell
M27 (vdd! vss! psub! vcg! net27 net28) invcell
M28 (vdd! vss! psub! vcg! net28 net29) invcell
M29 (vdd! vss! psub! vcg! net29 net30) invcell
M30 (vdd! vss! psub! vcg! net30 net31) invcell
M31 (vdd! vss! psub! vcg! net31 net32) invcell
M32 (vdd! vss! psub! vcg! net32 net33) invcell
M33 (vdd! vss! psub! vcg! net33 net34) invcell
M34 (vdd! vss! psub! vcg! net34 net35) invcell
M35 (vdd! vss! psub! vcg! net35 net36) invcell
M36 (vdd! vss! psub! vcg! net36 net37) invcell
M37 (vdd! vss! psub! vcg! net37 net38) invcell
M38 (vdd! vss! psub! vcg! net38 net39) invcell
M39 (vdd! vss! psub! vcg! net39 net40) invcell
M40 (vdd! vss! psub! vcg! net40 netb) invcell
V1 (vss!  0) vsource dc=vss type=dc
V2 (vdd!  0) vsource dc=vdd type=dc
V3 (psub! 0) vsource dc=psub type=dc
V4 (vcg! 0) vsource dc=vcg type=dc
V5 (a 0) vsource dc=vdd type=pwl wave=[0 0 1n 0 1.1n 3.3 1m 3.3]
C1 (vdd! 0) capacitor c=1e-05  m=1
M_subinst_nand_01 (net01 netb k psub!) modn \
w=wnu/1 l=lnu ng=1 \
as=(8.5e-07*wnu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wnu/1)/1 \
ad=(8.5e-07*wnu/1*fmod(1,2)+int(1/2)*2*5e-07*wnu/1)/1 \
ps=((2*8.5e-07+wnu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \
pd=((2*8.5e-07+wnu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \
nrd=5e-07/wnu/1 nrs=5e-07/wnu/1 mmvth=0 mmu0=0 \

M_subinst_nand_02 (k a vss! psub!) modn \
w=wnu/1 l=lnu ng=1 \
as=(8.5e-07*wnu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wnu/1)/1 \
ad=(8.5e-07*wnu/1*fmod(1,2)+int(1/2)*2*5e-07*wnu/1)/1 \
ps=((2*8.5e-07+wnu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \
pd=((2*8.5e-07+wnu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \
nrd=5e-07/wnu/1 nrs=5e-07/wnu/1 mmvth=0 mmu0=0\

M_subinst_nand_03 (net01 a vdd! vdd! ) modp  \
w=0.4e-6/1 l=0.35e-6 \
ng=1 as=(8.5e-07*0.4e-6/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*0.4e-6/1)/1
\
```

```
ad=(8.5e-07*0.4e-6/1*fmod(1,2)+int(1/2)*2*5e-07*0.4e-6/1)/1 \
ps=((2*8.5e-07+0.4e-6/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \
pd=((2*8.5e-07+0.4e-6/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \
nrd=5e-07/0.4e-6/1 nrs=5e-07/0.4e-6/1  mmvth=0 mmu0=0\

M_subinst_nand_04 (net01 netb vdd! vdd! ) modp  \
w=wpu/1 l=lpu \
ng=1 as=(8.5e-07*wpu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wpu/1)/1 \
ad=(8.5e-07*wpu/1*fmod(1,2)+int(1/2)*2*5e-07*wpu/1)/1 \
ps=((2*8.5e-07+wpu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \
pd=((2*8.5e-07+wpu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \
nrd=5e-07/wpu/1 nrs=5e-07/wpu/1  mmvth=0 mmu0=0\

M_subinst_nand_05 (net01 vcg! net01 vdd! psub!) modp_load  \
w=wplu/1 l=lplu \
ng=1 as=(8.5e-07*wplu/1*(2-fmod(1,2))+int((1-1)/2)*2*5e-07*wplu/1)/1 \
ad=(8.5e-07*wplu/1*fmod(1,2)+int(1/2)*2*5e-07*wplu/1)/1 \
ps=((2*8.5e-07+wplu/1)*(2-fmod(1,2))+int((1-1)/2)*4*5e-07)/1 \
pd=((2*8.5e-07+wplu/1)*fmod(1,2)+int(1/2)*4*5e-07)/1 \
nrd=5e-07/wplu/1 nrs=5e-07/wplu/1  mmvth=0 mmu0=0 extracted=1\

ic net01=3.3

//SIMULATOR OPTIONS ************************************

simulatorOptions options reltol=1e-6 vabstol=1.0e-6 iabstol=1e-12 \
tnom=27 homotopy=all limit=delta scalem=1.0 scale=1.0 \
compatible=spice2 gmin=1e-18 rforce=1.0 maxnotes=5 maxwarns=5 digits=5 \
 cols=80 pivrel=1e-3 sensfile="./sens.output" checklimitdest=psf \
temp=27
tran tran stop=1.75e-07 saveperiod=1.75e-11 \
savefile="./overlap_pmos/overlap_pmos_1raw.raw" errpreset=conservative
write="spectre.ic" \
writefinal="spectre.fc" annotate=status maxiters=50
operatingpoint info what=oppoint where=file
deviceparameters info what=parameters where=file
netlist info what=netlist where=file
```

```
function []= getdataoverlap(pth, name,fname_data, par1, par2)
%
% function to extract the timeinstances and data that is simulated
% output [time, datapoints of net01, current in oscillating state
% supplied by vdd]
%

vss = par1(1);
vdd=par1(2);
temp=par1(3);
wn=par1(4);
ln=par1(5);
wp=par1(6);
lp=par1(7);

wpl = par2(1);
lpl = par2(2);
vcg = par2(3);
psub= par2(4);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% definition of file where the simulated data is stored; in case of monte
% carlo runs each simulation result is stored in a seperate file with
% continuing numeration
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


for z=0:50
      if z==0
            fil= [ pth name '.raw/tran.tran'];
            j= num2str(z);
      else
      j= num2str(z);
            if z<10
                  j = ['00' j];
            elseif z>99
                  j=j;
            else
                  j = ['0' j];
            end;
            fil= [ pth name '.raw/mc1-' j '_tran.tran'];
    end;


    fid = fopen(fil);
    line = fgetl(fid);

    while ~any(findstr(line,'"time"'))
            line=  fgetl(fid);
    end;

    disp('1 sep index');
    disp('2 time');


    i = 3;
```

```
    while ~any(findstr(line,'value'))
              line=  fgetl(fid);
                 if any(findstr(line,'var'))
                    line=  fgetl(fid);
                 end;
                 disp( [ num2str(i) ' ' line]);
                 i = i +1;

    end;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% extraction of simulated data
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    dat  =  fscanf(fid,'%lf');

    i0 = find(dat==1);
    itime = i0 + 1;
    inet1 = i0 + 3;
    iidda = i0 + 49;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% data of interest
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    time = dat(itime);
    n1 = dat(inet1);
    idda = dat(iidda);

    t = time;
    y = n1;

%figure
%plot(time,n1,'b.-');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% shift of wave down by vdd/2 and determination of zero crossing
% of rising edge
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    n10 = n1 - vdd ./ 2;
    dn10 = diff(n10);
    dn10 = [ dn10 ; dn10(end) ];
    p0 = [];

    for k = 1 : length(n10)-1

     if ( n10(k) .* n10(k+1) ~= abs((n10(k) .* n10(k+1))) & dn10(k) > 0 )
            p0 = [ p0 k];
     end;
    end;
```

```
    timepoints = [time(p0(2):p0(end-1))];

    Datapoints = [ n1(p0(2) : p0(end-1)) ];

    currentpoints = [idda(p0(2) : p0(end-1))];
    p0(1) = [];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% calculation of period T and frequency
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    i1 = 1 : length(p0)-1;
    i2 = i1 + 1;
    Ti = time(p0(i2)) - time(p0(i1));

    T = mean(Ti);
    sT = std(Ti);
    f = 1 ./ T;

    I = currentpoints;
    time = timepoints;
    Tt= timepoints(end) - timepoints(1);

    %figure
    %plot(time, I,'.-');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% calculation of mean current
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    i1 = I(1:end-1);
    i2 = I(2:end);
    ii = (i1 + i2) ./2 ;
    dt = diff(time);

    idt = abs(ii' * dt);
    mI = idt / Tt;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% Save data to result file
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    fid_data = fopen(fname_data, 'a');

    s = [ par1 mI f par2 sT T z];

    fprintf(fid_data, '%1.15g\t %1.15g\t %1.15g\t %1.15g\t %1.15g\t
%1.15g\t %1.15g\t %1.15g\t %1.15g\t %1.15g\t %1.15g\t %1.15g\t %1.15g\t
%1.15g\t %1.15g\t %1.15g\n',s');
    fclose(fid_data);
end;
```

A.2 Final Design

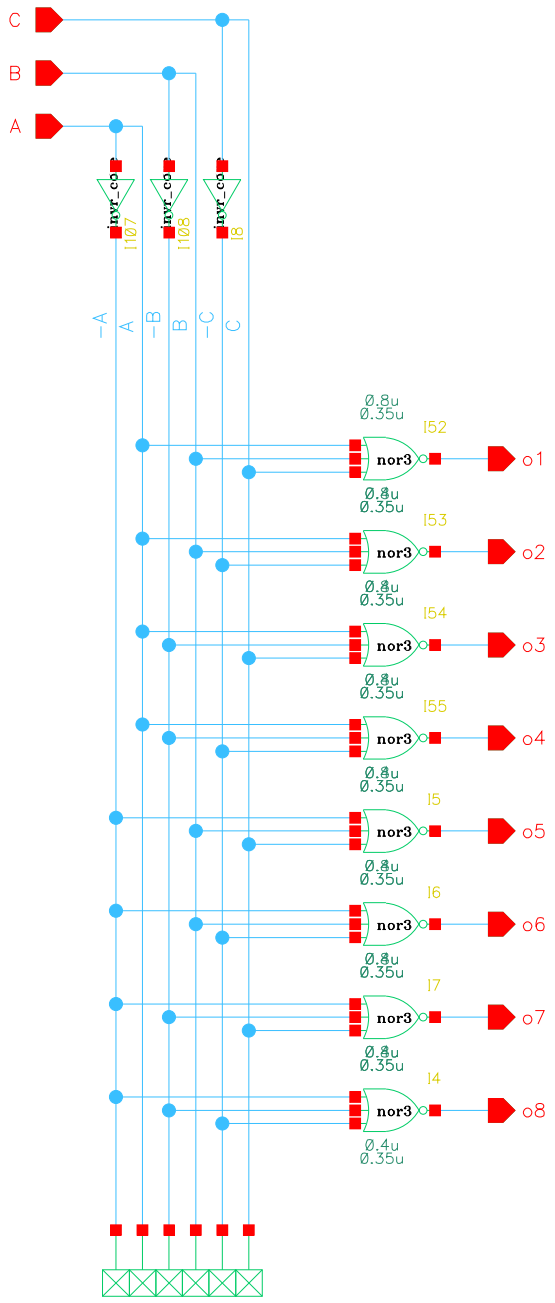


Figure A.1: Decoder design.

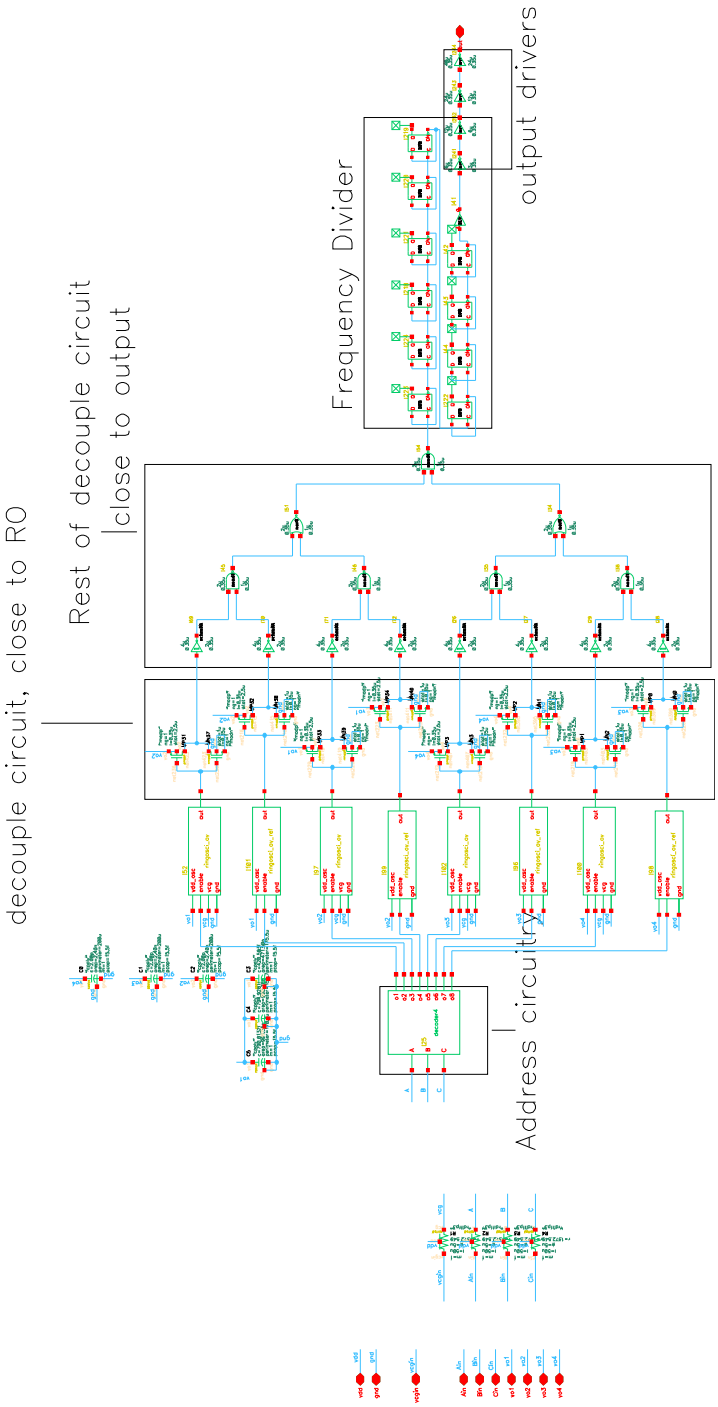


Figure A.2: Complete design of the SLM test chip with address and readout logic and eight ring oscillators. The design is intended to extract the gate to drain and gate to source overlap capacitance for both NMOS and PMOS transistors.

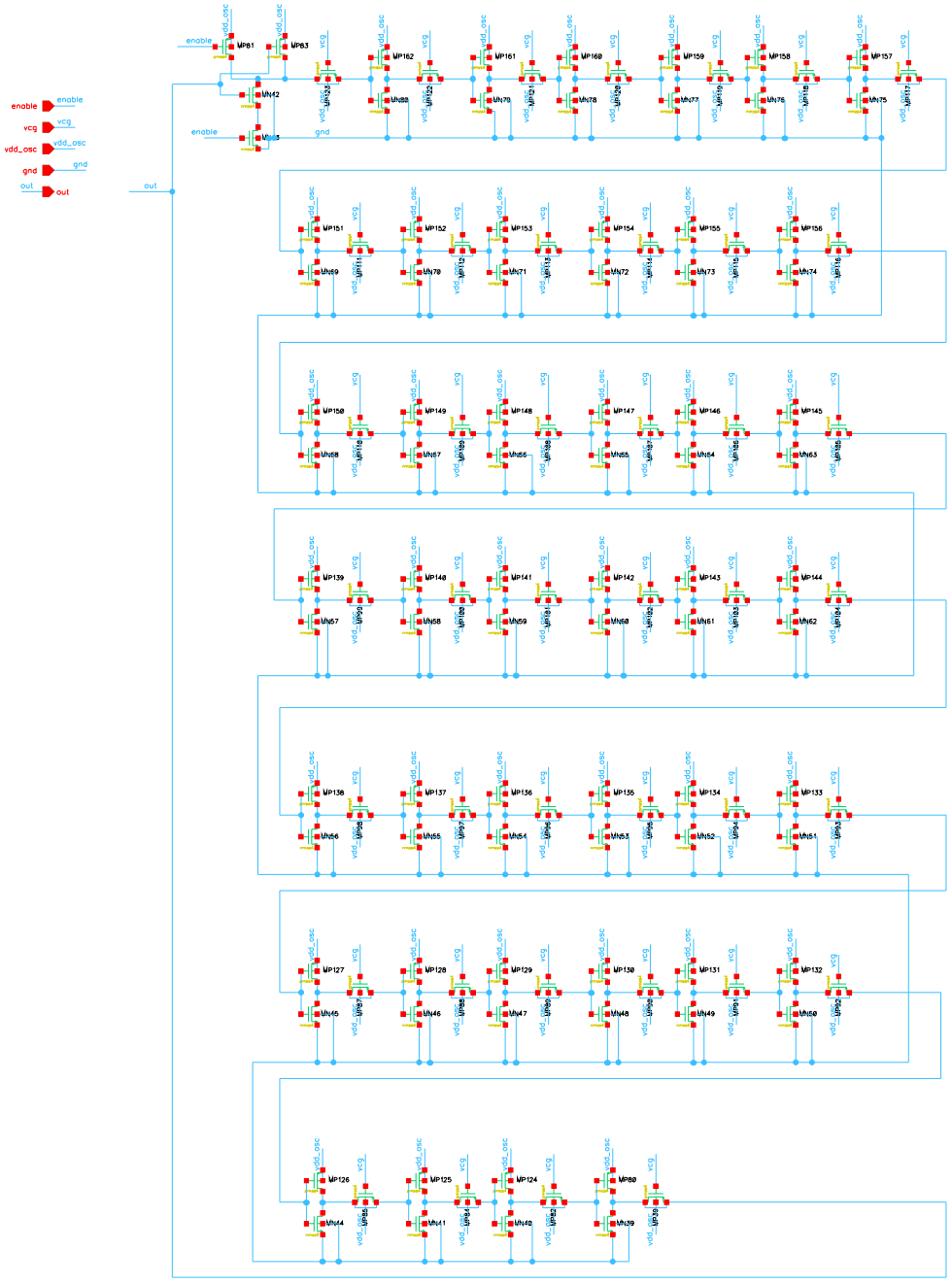


Figure A.3: Design of one 41 stage ring oscillator loaded with a PMOS load and an enable NAND gate.

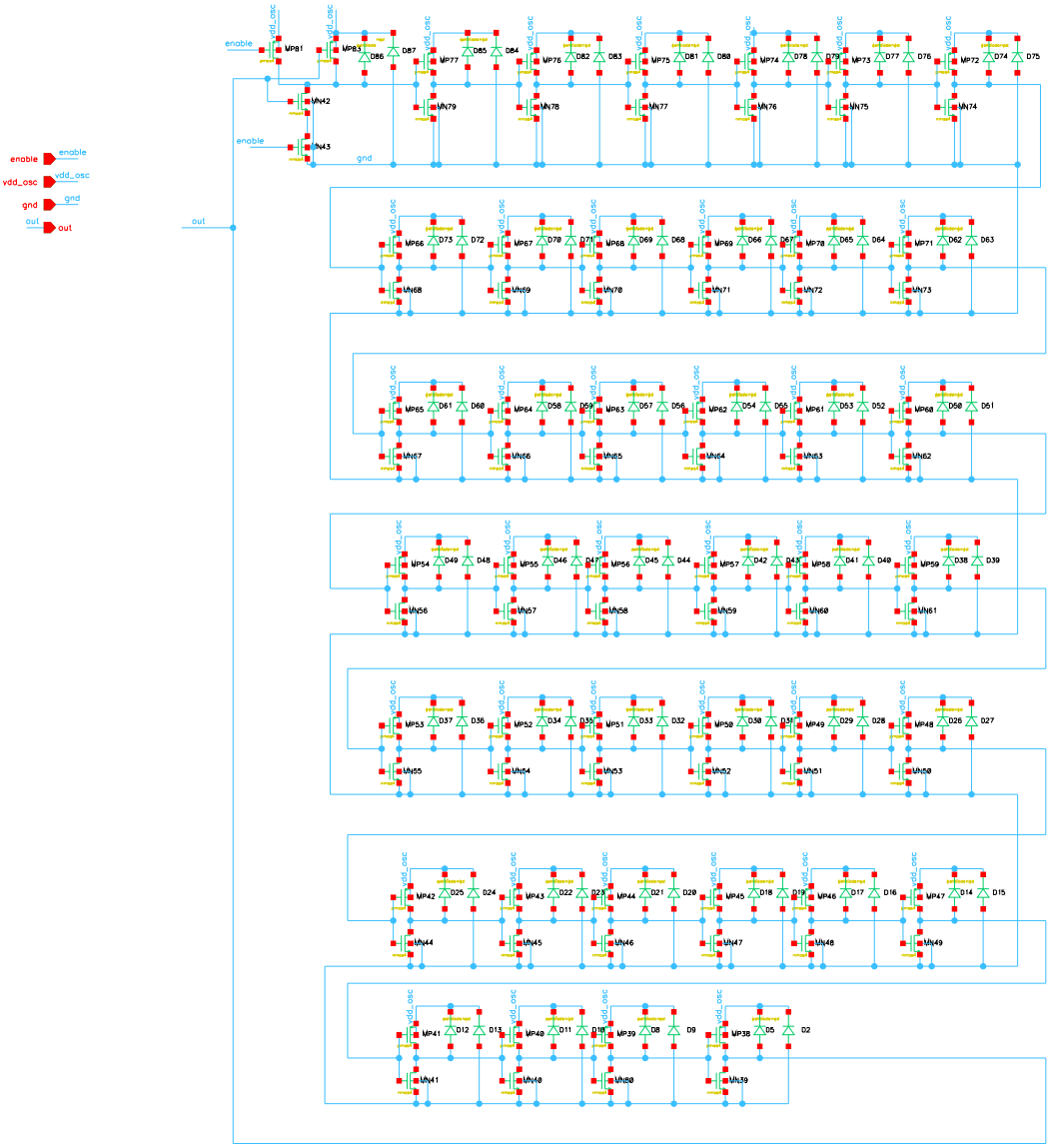


Figure A.4: Reference oscillator for the design in figure A.3. In between each inverter stage diodes are placed to represent the parasitic capacitances of the source and drain diffusion regions.

A.3 Measurement Results

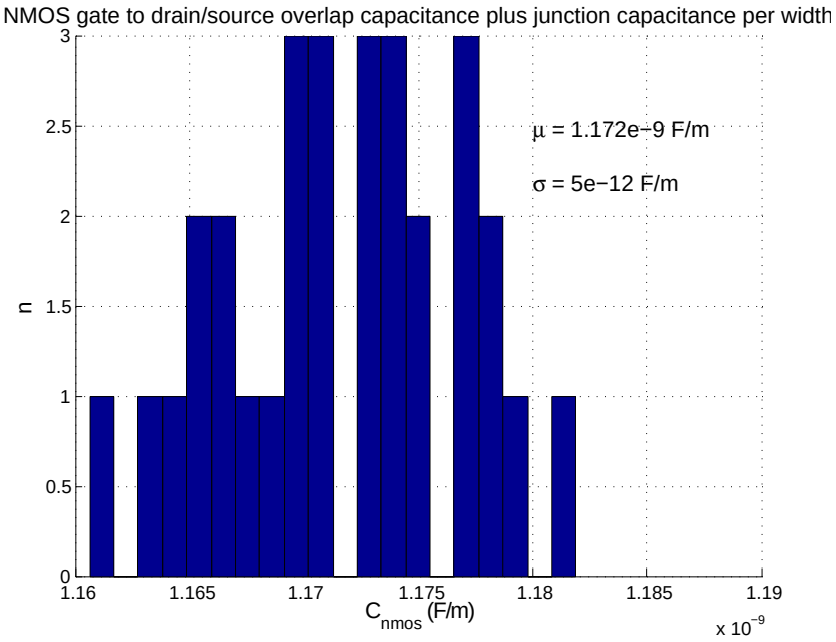


Figure A.5: C_{NMOS} results from test chip 1.

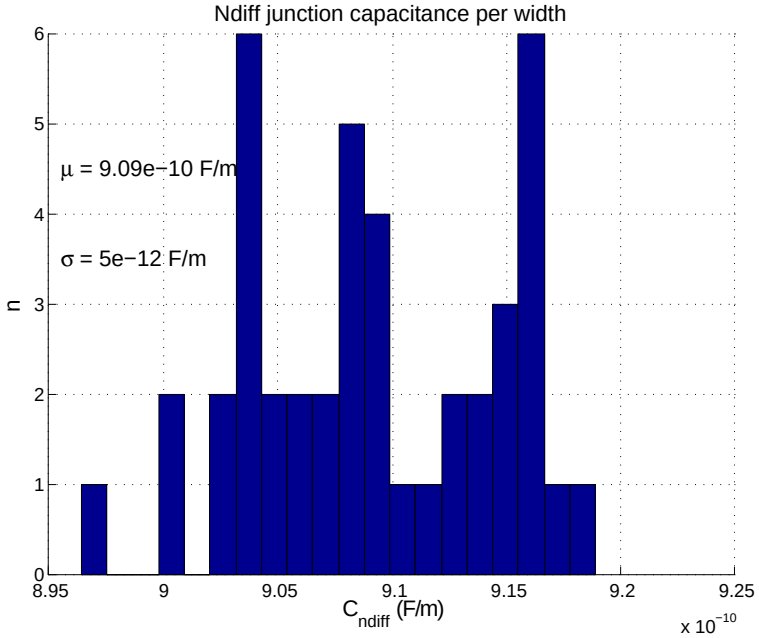


Figure A.6: C_{ndiff} results from test chip 1.

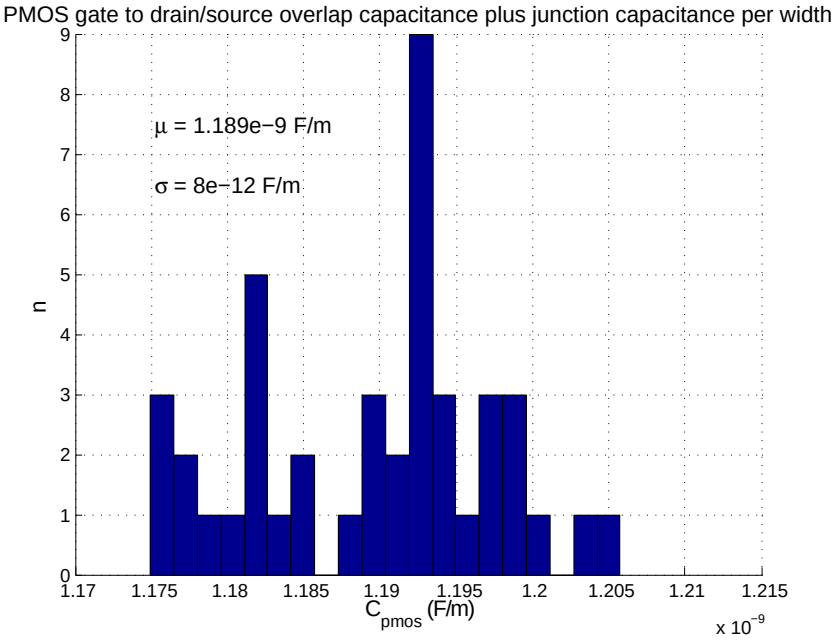


Figure A.7: C_{PMOS} results from test chip 1.

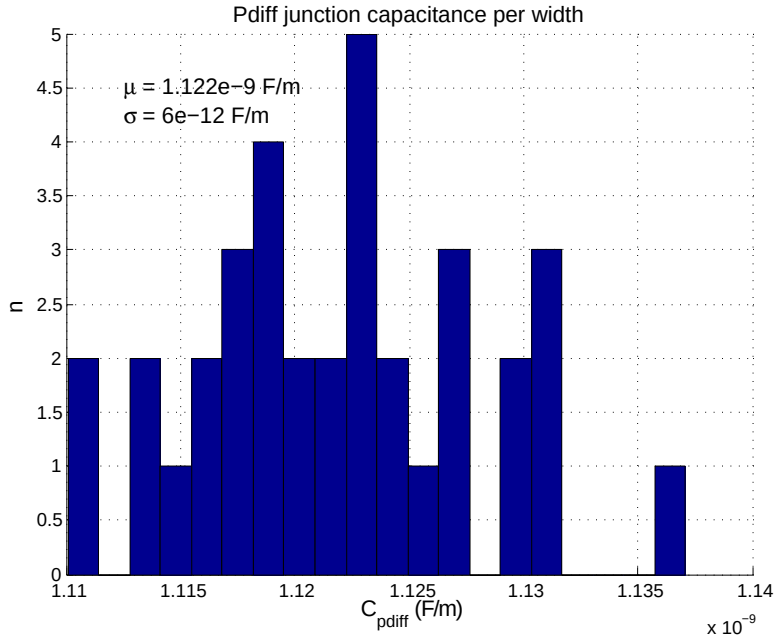


Figure A.8: C_{pdiff} results from test chip 1.

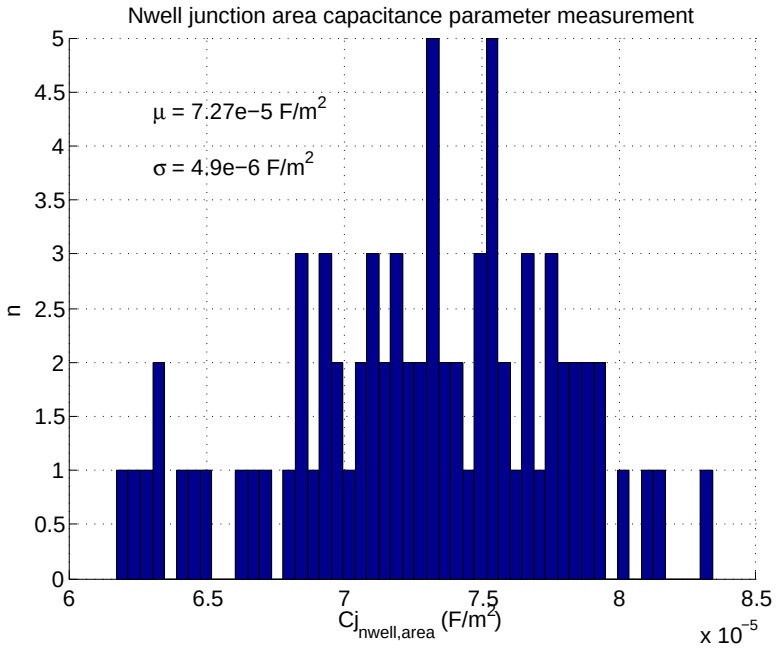


Figure A.9: $Cj_{\mathrm{nwell,area}}$ results from test chip 2.

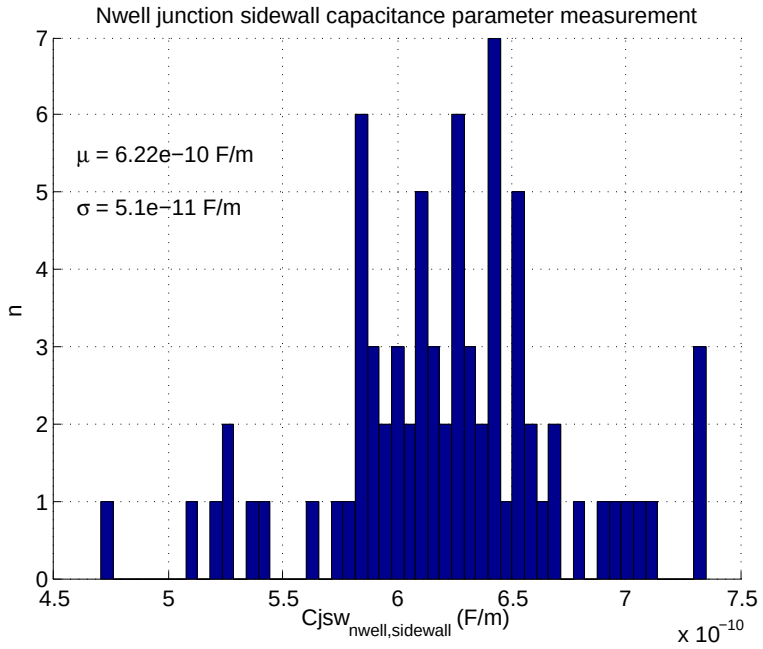


Figure A.10: $Cjsw_{\mathrm{nwell,\ sidewall}}$ results from test chip 2. The parameter corresponds to the sidewall scaling with length.

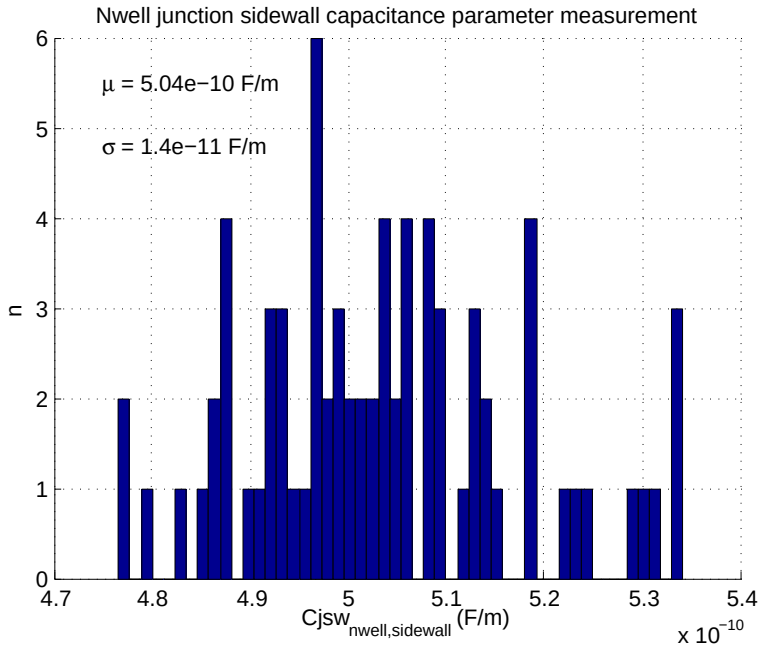


Figure A.11: $Cjsw_{\text{nwell, sidewall}}$ results from test chip 2. The parameter corresponds to the sidewall scaling with width.

Appendix B

Variability Characterization

B.1 Ring Oscillator Circuit Design

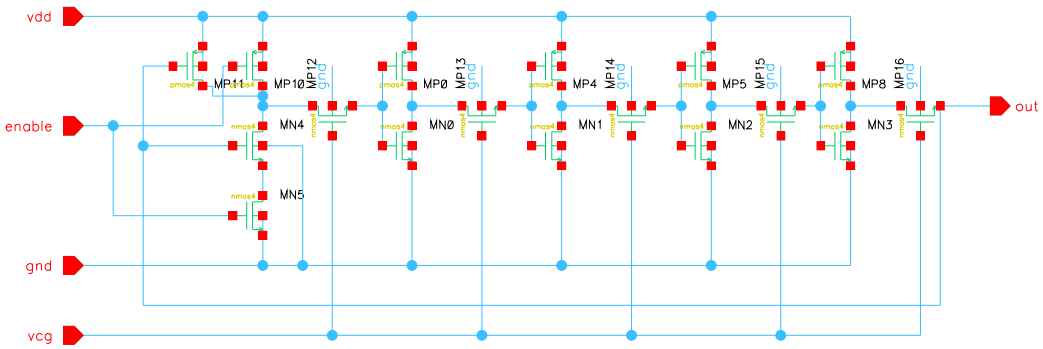


Figure B.1: Schematic of the NMOS passgate oscillator.

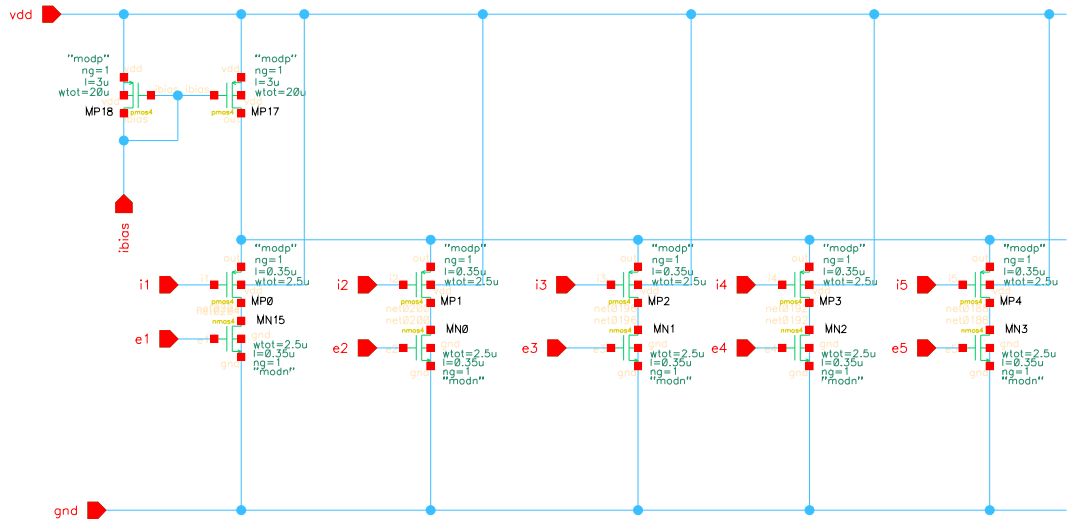


Figure B.2: PMOS source follower with NMOS switch to activate one path at a time.

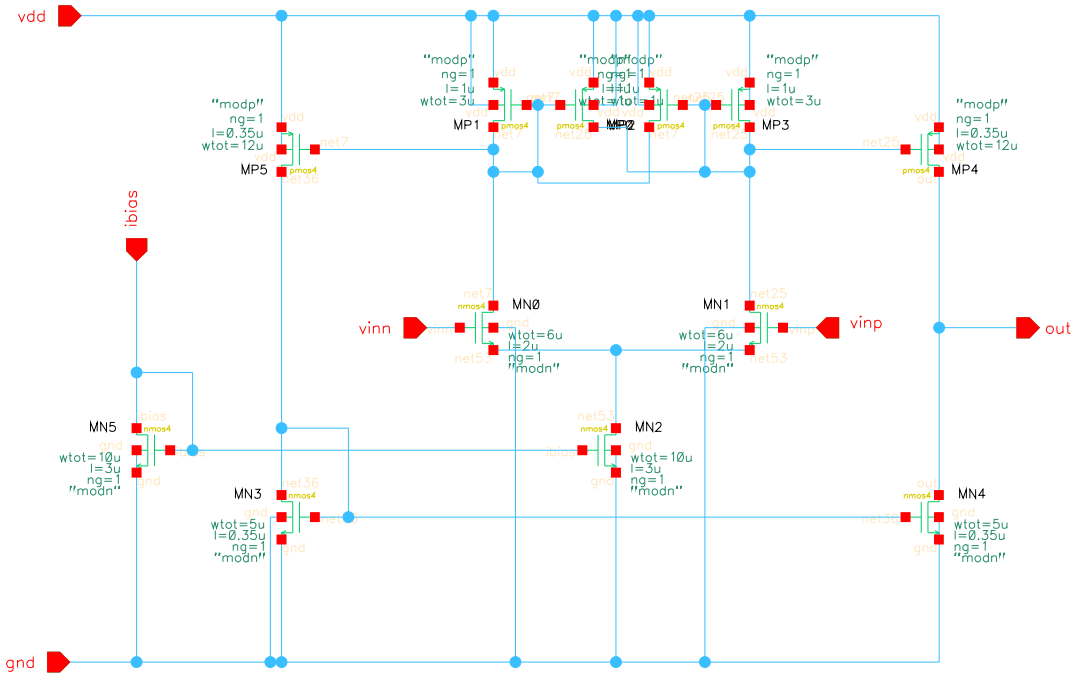


Figure B.3: Comparator with NMOS differential pair [12].

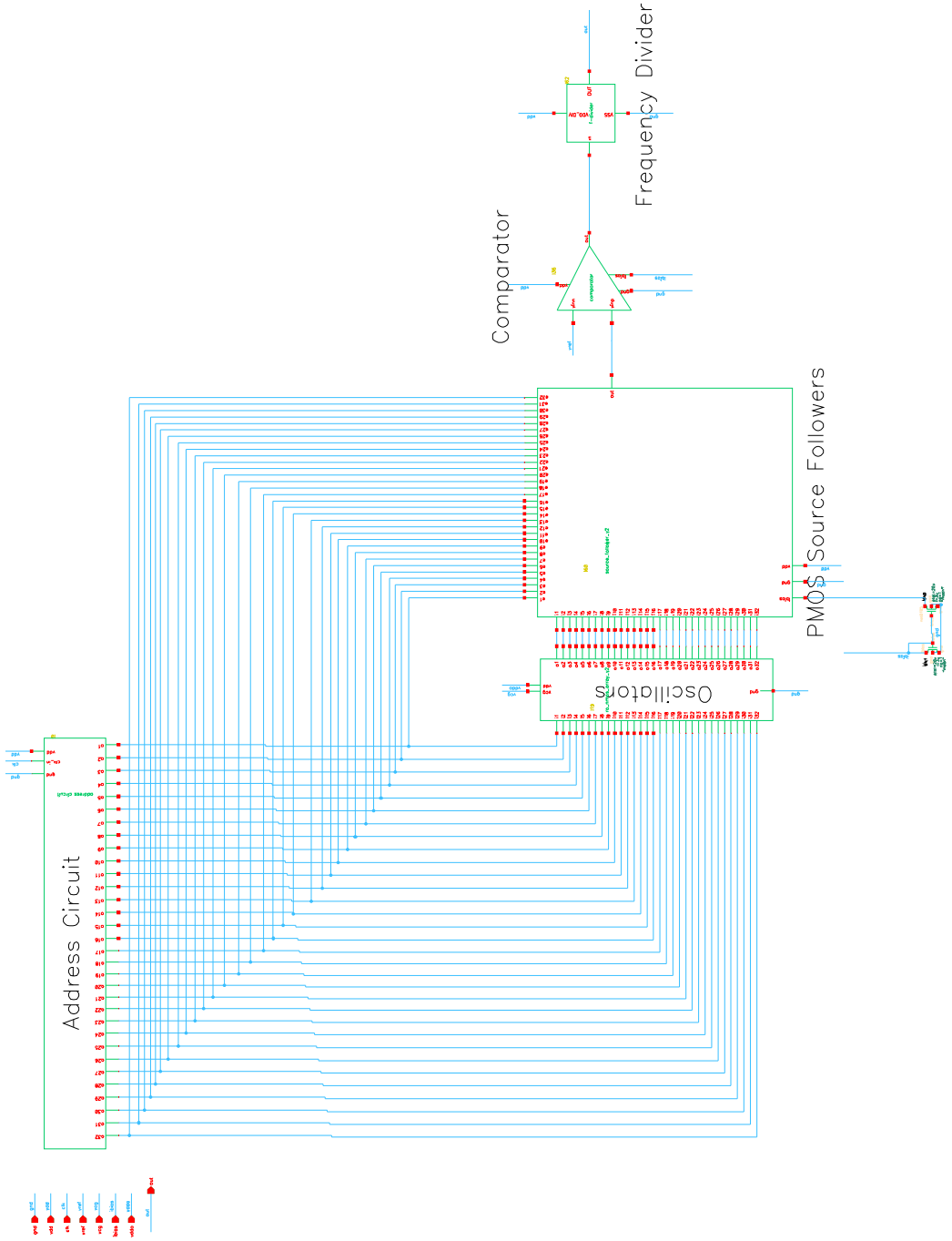


Figure B.4: Complete circuit for measurement of NMOS threshold voltage variability.

Appendix C

High-Voltage Ring Oscillator Investigations

C.1 Frequency Investigations

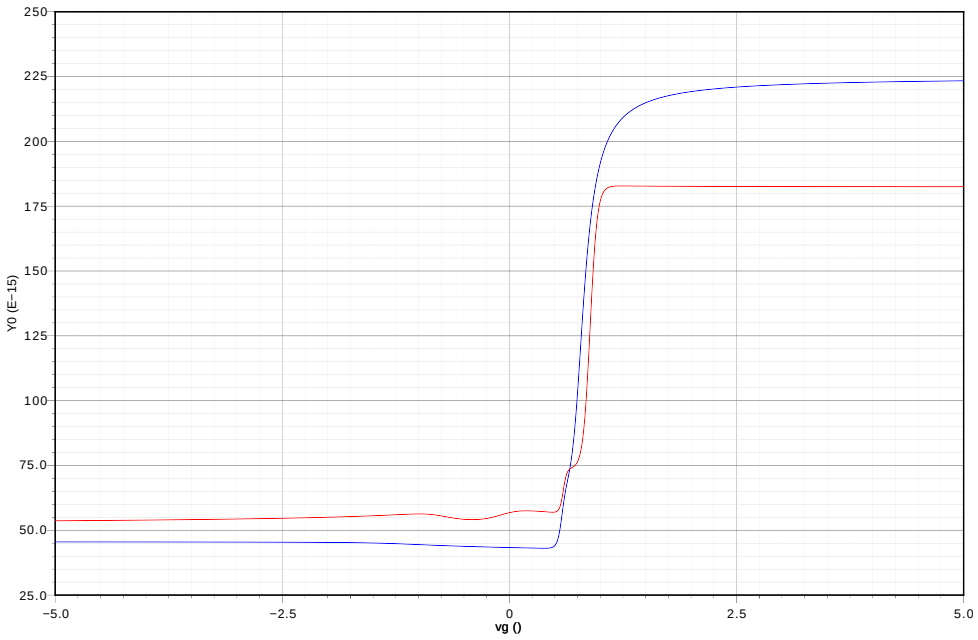


Figure C.1: Comparison of the overlap capacitance of the NMOS50m for BSIM3v3 and HiSIM_HV. red...BSIM3v3; blue...HiSIM_HV; ordinate Y0...Capacitance (F).

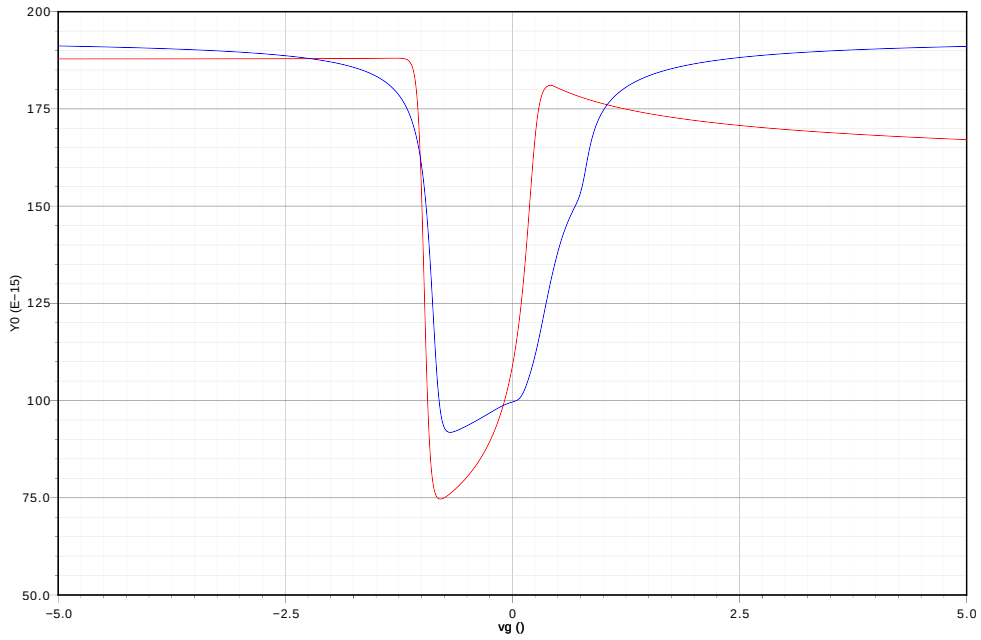


Figure C.2: Comparison of the gate capacitance of the PMOS50m for BSIM3v3 and HiSIM_HV. red...BSIM3v3; blue...HiSIM_HV; ordinate Y0...Capacitance (F).

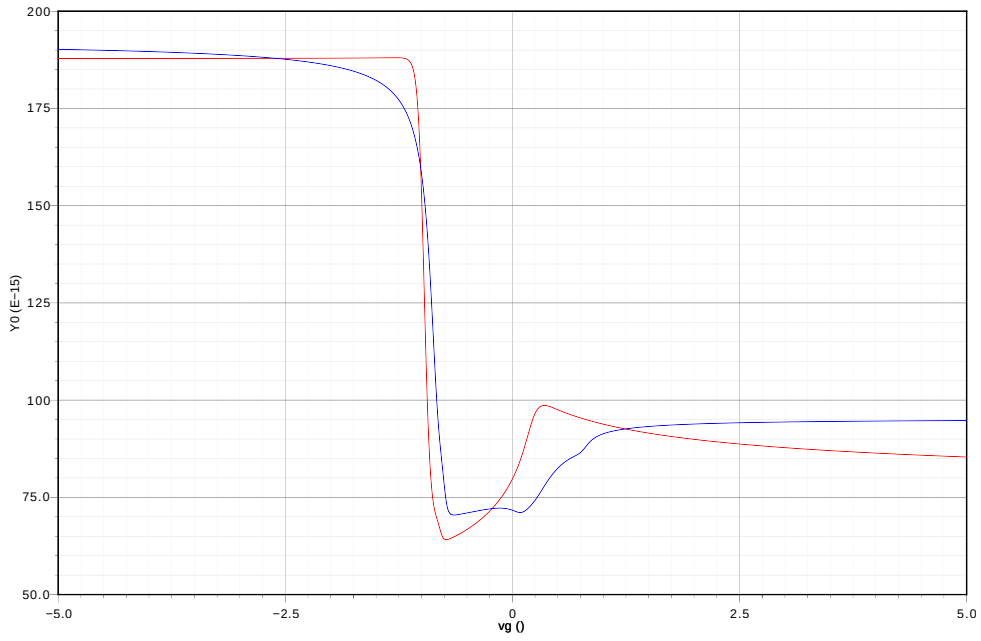


Figure C.3: Comparison of the overlap capacitance of the PMOS50m for BSIM3v3 and HiSIM_HV. red...BSIM3v3; blue...HiSIM_HV; ordinate Y0...Capacitance (F).

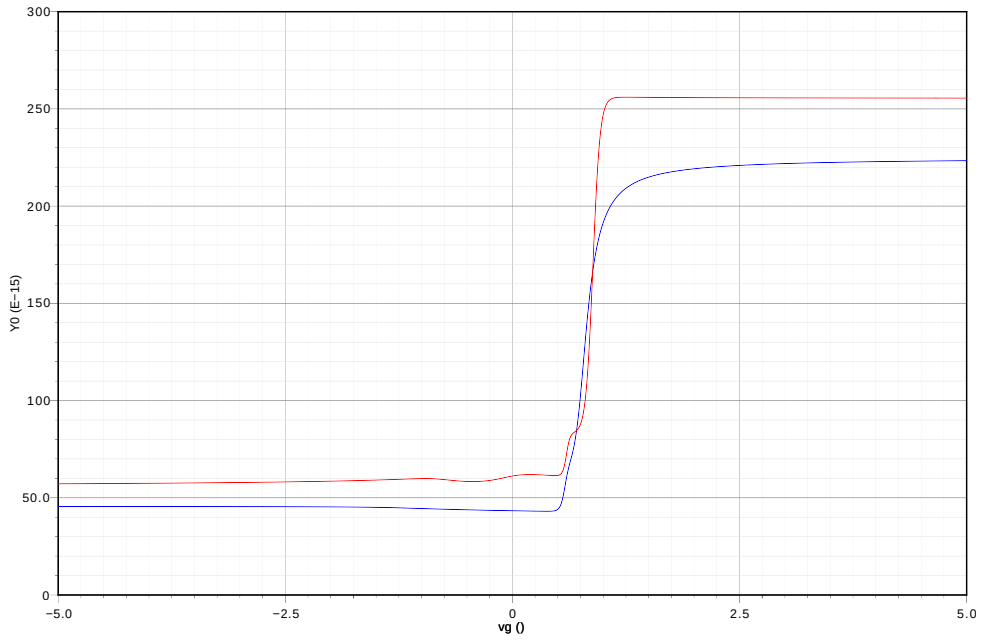


Figure C.4: Influence of BSIM3v3 parameter **dlc** on overlap capacitance. red...BSIM3v3; blue...HiSIM_HV; ordinate Y0...Capacitance (F).

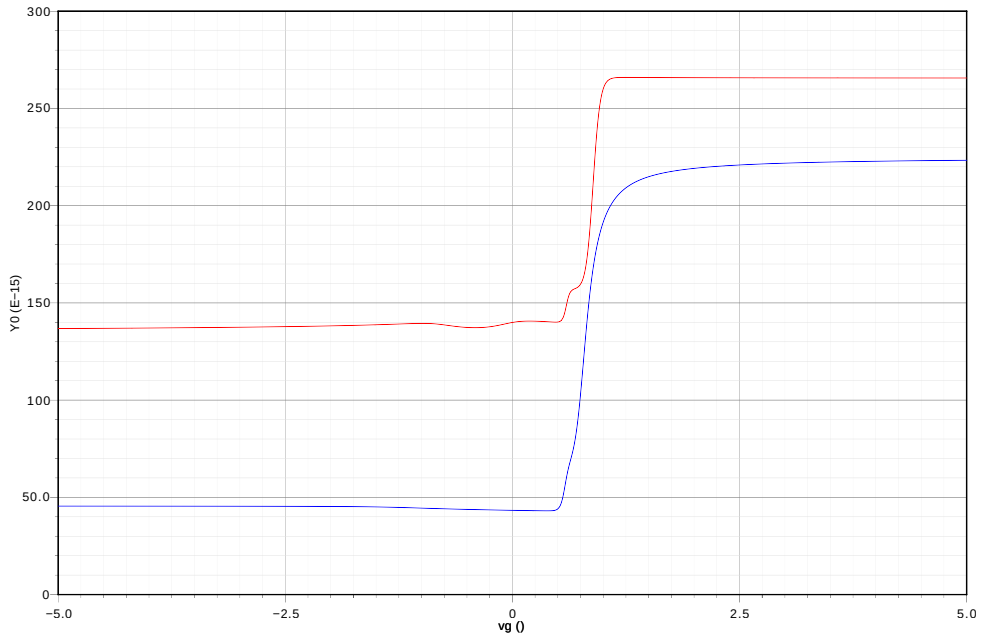


Figure C.5: Influence of BSIM3v3 parameter **cgdx** on overlap capacitance. red...BSIM3v3; blue...HiSIM_HV; ordinate Y0...Capacitance (F).