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Total Ionizing Dose Effects on CMOS Ring Oscillators

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AFFIDAVIT

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"... Nothing is more practical than a good theory ..."

—Ludwig Boltzmann

GRAZ UNIVERSITY OF TECHNOLOGY

Abstract

Faculty of Electrical and Information Engineering
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Master of Science
by Varvara Bezhenova

This thesis presents overview of the total ionizing dose effects on integrated circuits. The main focus falls onto medical imaging applications, computed tomography in particular. The purpose of this work is to create a solid background for characterisation of the radiation hardness of the given 0.18 μm CMOS technology.

State of the art in the radiation hardness research field as well as theory behind radiation effects is briefly presented. As ring oscillator is a circuit, widely used for process characterization, two ring oscillators are designed: standard cell based, and radiation hardened one. The radiation hardening technique applied is then analysed. The output stage including frequency divider, tristate buffer and output buffer is optimized. The modelling of the radiation effects on device, block and top level is performed. The effects on a single transistor are simulated with the ECORCE software. An analytical and a Cadence/Spice simulation model of radiation effects on ring oscillators are compared.

Diese Masterarbeit umfasst die Effekte der radioaktiven Strahlung auf integrierte Schaltungen. Das Schwerpunkt fällt dabei auf Anwendungen in Computertomographen. Ziel dieser Arbeit ist, eine Grundlage zur Charakterisierung der Strahlungsrobustheit für 0.18 μm CMOS Technologie zu schaffen.

Aktuelle Forschungsergebnisse sowie die theoretischen Grundlagen von Strahlungseffekten sind kurz dokumentiert. Da ein Ringoszillator eine zur Prozesscharakterisierung oft verwendete Schaltung ist, werden zwei Oszillatoren entworfen: ein auf Standardzellen basierendes und ein strahlungsrobustes Modell. Zum Erreichen dieser Robustheit wir die Inverted-Source Methode verwendet. Die Ausgangsstufe, bestehend aus Frequenzteiler, Tristatepuffer und Ausgangspuffer, ist optimiert. Die Effekte der radioaktiven Strahlung sind auf Transistor-, Block- und Schaltungsebene modelliert. Zur Charakterisierung eines einzelnen Transistors unter Einfluss von radioaktiver Strahlung wird der Strahlungssimulator ECORCE verwendet. Zusätzlich werden ein analytisches und ein Cadence/Spice Makromodell des Ringoszillators verglichen.

Acknowledgements

First of all I would like to thank my supervisor, Dr. Alicja Malgorzata Michalowska-Forsyth, for all the professional advice, patient guidance and friendly support she gave me while writing this thesis. Her charisma and motivation inspired me. Her expertise in analog design and radiation hardness provided me all the resources to complete this thesis. Her positive attitude kept me optimistic along all ups and downs of the project.

I would also like to thank the COTOMICS project team and the colleagues from ams AG, who made this thesis possible in the first place. Special thanks goes to my professor Dr. Bernd Deutschman, who showed me this opportunity. In addition I would like to thank Dr. Mario Auer, who taught me analog chip design. The knowledge I gained from him gave me a solid background for this work. I extend my gratitude to professor Dr. Peter Söser. His valuable feedback on the literature study for this work aided the improvement greatly. His knowledge of official procedures associated with thesis submission facilitated it a lot for me.

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I would also like to express my gratitude towards my English teacher and friend Olena Syvachuk, who readily helped me with grammar in such a short time.

Last but not least, my gratitude goes on my family and friends. I want to thank my parents, Olena and Sergiy Bezhenov, who believed in me. Their love kept me going. I would also like to mention Sofia Losieva, my dearest friend, whose support gave me strength in tough moments. And of course, many thanks go to my fellow students and friends, whose positive attitude provided me energy and optimism along my studies.

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Contents

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Abbreviations

CMOS	**C**omplementary-**m**etal-**o**xide-**s**emiconductor
TID	**T**otal **I**onizing **D**ose
IC	**I**ntegrated **C**ircuit
STI	**S**hallow **T**rench **I**solation
CT	**C**omputed **T**omography
e-h	**e**lectron - **h**ole (pair)
RO	**R**ing **O**scillator
RHBD	**R**adiation **H**ard **b**y **D**esign
FD	**F**requency **D**ivider
FEM	**F**inate **E**lement **M**ethod

Scope

Presented work is done in the framework of the COTOMICS project. The focus of the project falls onto the radiation hardness of electronics for computed tomography. The aim of the project is to create a set of design guidelines for radiation tolerant integrated circuits. In this particular thesis I concentrate on the design of the circuits for technology characterisation, particularly on a ring oscillator.

In the Introduction one can find the overview of the research in the field of radiation hardness of integrated circuits. The first steps on the way of radiation hardness topic exploration as well as modern challenges are discussed. The purpose of the work is specified.

Chapter 2 concentrates on the ionizing radiation phenomenon, and its effects on the integrated circuits. Main focus falls onto cumulative effects, total ionizing dose effects in particular, as they are the major ones for computed tomography applications.

In Chapter 3 the main approaches to radiation hardening are presented. Some considerations on differences in transistor characteristics after irradiation depending on technology are discussed. Radiation hardening by design (RHBD) is reviewed, including layout techniques as well as radiation hard circuit topologies.

Further, circuits design is shown in Chapters 4 and Chapter 5. Two ring oscillators, as presented in Chapter 4 and design for test, described in the Chapter 5 are meant to be used for characterization of radiation hardness of the given technology in the future. Design challenges and optimization process are also discussed in these chapters.

Chapter 6 focuses on modelling of the radiation effects on device, block and top levels. For the device radiation response analysis, the ECORCE simulation tool is used. It is briefly described in section 6.1 of this chapter. Section 6.2 gives macro-model for

simulation of the inverter cell, further used in ring oscillator simulations. Moreover, analytical model for ring oscillator parameters evaluation after irradiation is given. The results of calculations and simulations for two different ring oscillators are discussed. The conclusions on radiation hardening technique are made. The comparison of both models is done, showing the weaknesses and strengths for further use and investigation.

Finally, in the Conclusions I summarize the results of the performed work. The main outcomes are listed and discussed. The Outlook gives an overview of the next steps in this research project, based on the conclusions from this work. It includes considerations on radiation effects contributions, test structures and modelling.

Introduction

The sources of radioactivity are all around us. A harsh radioactivity in space or in a particle accelerator are only few among the vast of examples. Also solar activity and isotopes, naturally present in our surroundings cause low intensity background radiation. A plethora of applications is influenced by radiation. Electronics for space missions, medical imaging and nuclear power plants have to deal with direct radiation sources. Some effects cumulate themselves over longer periods of time causing long-lasting damage. Also security and safety oriented devices, as e.g. in automotive industry, have to consider effects of background radiation. Even a single charged particle can cause malfunction of an IC. Thus, radiation hardness assurance is a critical subject for numerous applications.

1.1 First Steps

The realisation of a need to study radiation influence on integrated circuits arose in late 1950s, as semiconductor technology started to be used in aerospace and military equipment [1]. The sensitivity of MOS devices to radiation was first discovered in early 1960s [2]. The early works determined the fundamental cause of the devices damage - the charge build-up in the SiO_2 [3].

The struggle to develop radiation hard technology escalated in 1970s [3]. Different approaches to gate-oxides hardening [4], [5], and general control of processing procedures (for example dry oxide gate oxidation at temperature of 1000 °C) [6], [7] provided sufficiently radiation tolerant devices. The dependence of the threshold voltage shift of CMOS devices on the thickness of oxide regions was discovered [8]. Work in 1980s has predicted that the gate oxide radiation problem doesn't appear at thickness less than

10 nm [9]. However, due to necessity of higher integrated circuits (IC) density, the use of field oxide introduced new total ionizing dose (TID) related challenges [3].

As it will be further discussed in this work, the prediction, mentioned above, indeed has become true to some extent. The simulations performed on a single transistor level under 130 krad irradiation show minor changes in the transistor parameters. Nevertheless, smaller feature technologies still suffer from radiation damage. The main source of parameter changes, however, appears to be in the field oxide and shallow trench isolation.

As in 1990s the focus fell onto hardening sub-micron silicon gate devices, the issues of the gate oxide TID response became minor [3]. However, the shallow trench isolation (STI) approaches, used to meet scaling requirements have shown variety of TID related failures. Nevertheless, the hardness of STI region depends on a plethora of factors, like geometry and type of trench refill oxide, creating a vast spread in hardness of similar processes [10], [11], [3].

1.2 Modern Challenges

As the technology develops, new challenges appear. Over the last 30 years the lengths of the gate have dropped dramatically, as well as the thickness of the gate oxide. The radiation hardness concerns have entered commercial applications, in opposite to the first tries driven mostly by military during the Cold War times [12]. Moreover, increased complexity of the circuits and systems challenged radiation hardness assurance by test. Thus, reliable modelling of the radiation response on device as well as on circuit level is also topical nowadays.

Although the scaling of modern digital CMOS technologies provides advantages by decreasing TID effects on threshold voltage, the mixed signal and power MOS integrated circuits, which still use thicker oxide devices, are still experiencing characteristics changes due to radiation exposure [3]. Furthermore, STI radiation response is still an issue also for smaller feature CMOS technologies.

So, it is a task of modern research and development to provide general design guidelines to mitigate the unwanted effects as well as reliable models of post-irradiation behaviour in order to be able to analyse achieved improvements without destructive tests.

1.3 Radiation Hardness in Computed Tomography ICs

In this work focus falls onto medical imaging applications, computed tomography (CT) in particular. The main particularity of medical imaging applications is long term exposure of IC to low dose radiation. Normal lifetime of a medical imaging device reaches 10 years (5 days a week, 8 hour operation) [13]. Within this life-span, electronics, used for imaging is in average exposed to a dose of more than 160 krad [14]. Such dose can lead to e.g. threshold voltage (V_{th}) shift of about 100 mV for commercial technologies with gate oxide thickness of around 6 nm [15]. Thus, sensitive imaging sensors and signal processing circuits can undergo severe damage, possibly leading to false images or general malfunction of the machinery.

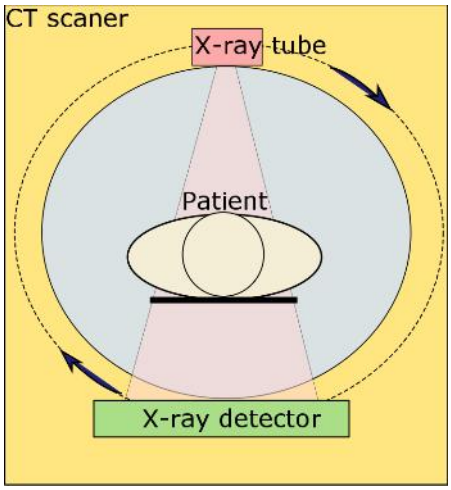

FIGURE 1.1: Computed tomography scanner

A sketch of computed tomography scanner is presented in Figure 1.1. In early models, most signal processing has been done on the external computer, CT scanner only including detector circuitry. Modern machines, in order to increase efficiency, and save space and resources, try to partially or fully integrate image processing circuitry into the CT scanner itself, which obviously leads to more severe radiation hardness requirements of the ICs.

Presented thesis has been done in a framework of COTOMICS project, dealing with radiation hardness of ICs for computed tomography. The aim of the project is to create a set of guidelines for radiation aware IC design. The purpose of this work is to set the first steps in technology capabilities characterisation, create a modelling background for later research and to define further investigation directions.

Chapter 2

Ionizing Radiation Phenomenon

Generally, radiation is a transmission of energy in the form of waves and particles. It can be natural or man-made. It is known that some atomic nuclei are less stable than others [1]. All elements starting from number Z=83 (lead) undergo nuclear rearrangement with emission of sub-atomic particles, thus are radioactive. Among them, elements from 93 to 106 have been produced artificially.

Before discussing ionizing radiation phenomenon in more detail, a few important measurement units are to be mentioned. First of all, *becquerel*, which is a measure of radioactivity [1]. It is the rate of 1 disintegration per second. Next, it is vital to know the energy of radiation. This is measured in *kilo-electronvolt (keV)*. The energy levels of radiation will be discussed further. Furthermore, one should be able to define the dose of radiation. The SI unit of dose is *Gray (Gy)*, which corresponds to absorption of one joule of energy in the form of ionizing radiation per kilogram of matter [16]. However, another unit is still widely used in the scientific community - *rad*. It was originally defined in CGS units in 1953 as the dose causing 100 ergs of energy to be absorbed by one gram of matter [16]. An *erg*, in turn, is the amount of work done by a force of one *dyne* exerted for a distance of one centimetre. **1 rad** corresponds to **0.01 Gy**.

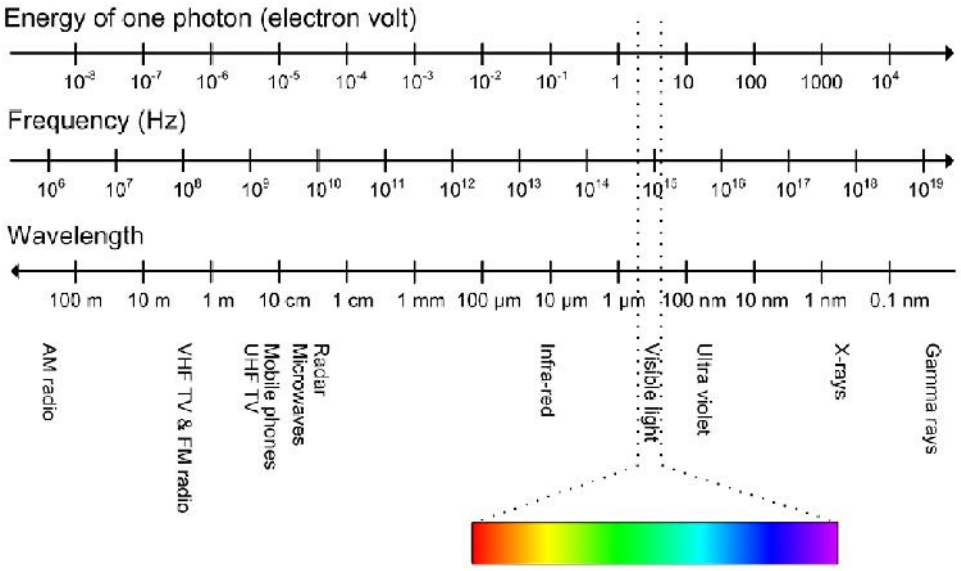

FIGURE 2.1: Electromagnetic spectrum

2.1 Types of Radiation

Figure 2.1 shows the electromagnetic spectrum. As it can be seen, the ionizing radiation as it is starts at energy levels of around 1 keV and above. It corresponds to the frequencies above 1 EHz and wavelength of below 1 nm. A brief discussion about types of radiation and their characteristic properties is presented in this section.

2.1.1 Gamma Rays and X-rays

These are forms of photon or electromagnetic radiation with the wavelength of 1 nm and shorter. A gamma ray originates from nuclear interaction, while an X-ray is caused by electronic or charged-particle collisions. The energy of one photon can be of 100 keV for soft X-rays and 1MeV and higher for gamma rays and hard X-rays. Depending on energy levels, the mechanism of interaction with matter is different [1].

2.1.2 Alpha Particles

These particles are high velocity nuclei of the He atoms. They are positively charged and have mass of 4. They are heavily ionizing due to the high energy level (typically 5MeV). The penetrating power of such particles is low, and they travel mainly in straight lines. The depth of penetration in silicon reaches approximately 20 μm [1]. Such small depth

is explained by Coulomb interaction with atoms of the material, which slows down and finally stops the particle.

2.1.3 Beta Particles, Electrons and Positrons

Either positively or negatively charged, these particles have the same mass as an electron. They can easily penetrate matter due to their small size and small charge. They possess high velocity, usually approaching the speed of light, and are lightly ionizing [1].

2.1.4 Protons

The proton, having a charge of 1 unit, has 1800 times mass of an electron and thus is difficult to deflect. Such a particle, entering the matter, can lead to the change of the atomic structure [17], so-called displacement damage, which will be discussed in following chapters.

2.1.5 Neutrons

Without a charge, and thus no Coulomb interaction involved, and possessing relatively high mass (the same as proton), those particles are especially hard to stop. A neutron can be slowed down by a hydrogenous material, which makes water an especially effective shield for these particles. The capture of a neutron causes an emission of a gamma ray [1].

2.2 Interaction Mechanisms

Different types of radiation, having different properties, interact with matter differently. However, they all result in a limited variety of products: either an electron-hole pair, a gamma ray, or a charged particle.

So, X-rays and gamma rays usually cause a photoelectric effect, Compton scattering and electron-hole (e-h) pair production in the matter. Charged particles interact via

Coulomb forces, generating e-h pairs. Neutrons, as the most penetrative particles, participate in elastic (creating gamma ray) or inelastic (resulting in a charged particle) scattering.

For electronics, the major result of the exposure to ionizing radiation, having effect on circuitry functionality, is the electron-hole pair generation.

2.3 Radiation Effects on Integrated Circuits

Different interaction mechanisms lead to energy absorption within the chip, causing ionization. Often, it is a result of photoelectric effect or Coulomb interaction. It leads to creation of electron-hole (e-h) pairs - an unwanted charge that can lead to damage of an IC [18]. In this section, basic processes are reviewed. Generally, one can differentiate between two categories of radiation effects: single event effects (SEE) and cumulative effects.

2.3.1 Single Event Effects

Single event effects are caused by a single charged particle entering matter. It is mainly point of concern to space applications. However, cosmic rays can also upset memory cells on Earth. Moreover, soft errors due to alpha particles from radioactive materials in packaging are topical since 1978 [19]. Finally, there is a suggestion that an irreducible minimum rate of soft errors is caused by radioactivity in the silicon itself [1].

So, a charged particle penetrates the matter at high speed, leaving a track of electron-hole pairs behind (Figure 2.2). This deposited charge is collected in a nearby circuit node, which may lead to a change of state of the memory cell or other issue. Moreover, ionizing radiation can trigger "on" condition of the parasitic bipolar structures in CMOS circuits, known as latch-up. Such a condition is common for complex devices. The device "locks up" and doesn't respond to control signals. A destructive consequence of a latch-up is a "burn-out" [1].

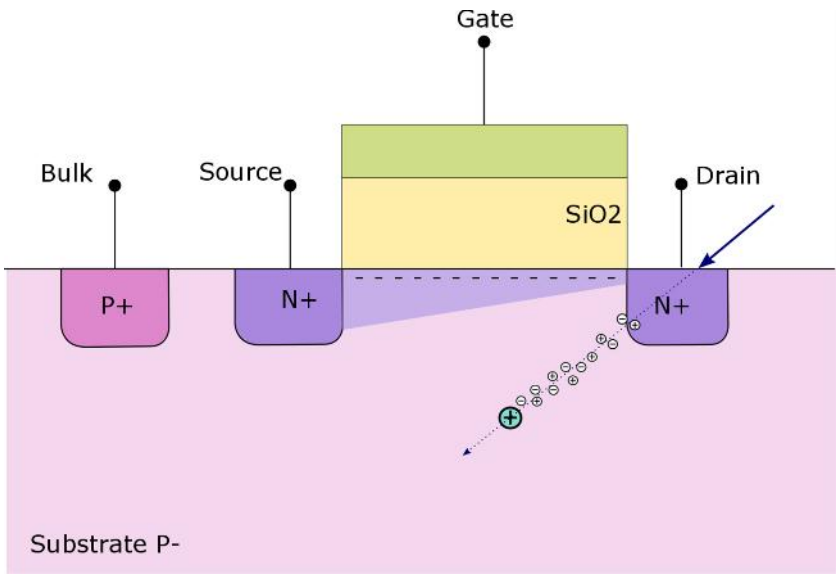

FIGURE 2.2: MOS cross-section: particle track

2.3.2 Cumulative Effects

If an IC is exposed to low energy radiation for a long period of time, the total dose causes damage, which can last for life-time. These effects can be observed already at the device level, consequently leading to degradation of device parameters, which in turn can disturb functionality of associated circuitry. Such effects are referred to as cumulative effects.

Generally there are two basic cumulative effects, coming from different interaction mechanisms: displacement damage, caused by a particle with a mass, and so-called total ionizing dose effects (TID), caused by ionizing radiation.

The focus of this thesis falls onto cumulative effects, TID in particular. However, for full overview of the problematic, displacement damage is also briefly discussed below.

2.3.2.1 Displacement Damage

A particle with mass, such as e.g. proton, can change the grid structure of the crystal when penetrating matter. The particles of the matter are displaced, so that vacancy-interstitial atom pair is created, as it is shown in Figure 2.3. Further particles cause further displacements, leading to cascade of damage.

The change in the crystal lattice leads to change of energy levels of semiconductor. This phenomenon often produces energy states close to bandgap [17], and can lead to shorter lifetime due to recombination within the material, generally increasing leakage currents and noise of the devices [1].

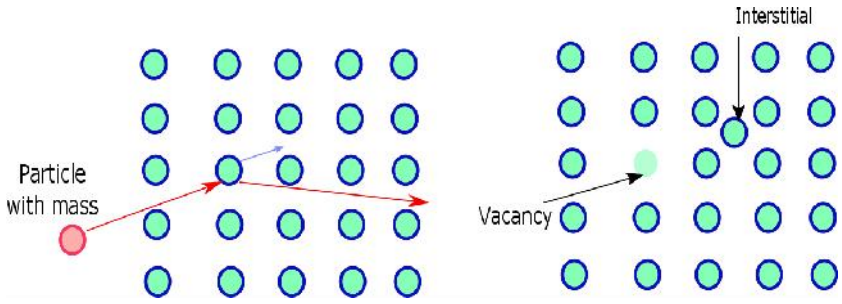

FIGURE 2.3: Displacement damage

2.3.2.2 Total Ionizing Dose Effects

As already mentioned above, total ionizing dose effects (TID) are caused by ionizing radiation. Photoelectric effect leads to generation of e-h pairs. Under application of the electric field the particles move. Electrons, having higher mobility, can escape the matter, while holes get trapped in the gate oxide and on its surface (Figure 2.4). This trapped charge creates parasitic electric field. This leads to degradation of device electrical characteristics, as for example threshold voltage shift or increase in the leakage current.

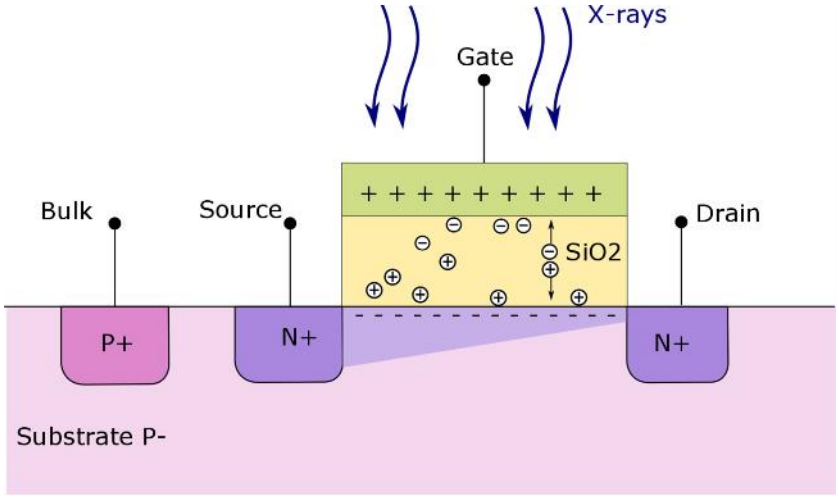

FIGURE 2.4: MOS cross-section: trapped charge

The density of the generated e-h pairs is proportional to the irradiation exposure time [20]. The total amount of energy that results in e-h pair generation is thus defined as total ionizing dose [21].

The parasitic charge in the device can be generally subdivided into three basic groups: oxide trapped charge, border traps and interface traps on the border between Si and SiO_2 [21].

The (usually) positive charge in the gate oxide *(oxide trapped charge)*, as presented in Figure 2.4, first of all leads to decrease of the drain current for a given gate-source voltage for both NMOS and PMOS, in other words, to the reduction of threshold voltage of n-channel transistor and increase of p-channel transistor threshold voltage magnitude, as shown in the Figure 2.5.

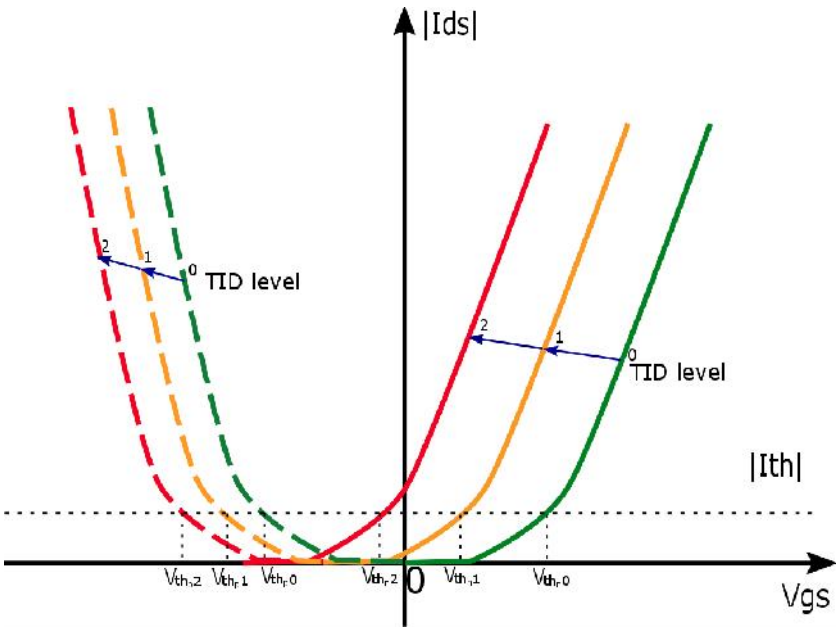

FIGURE 2.5: Transfer characteristic of NMOS (solid line) and PMOS (dashed line) transistors: oxide traps influence

The effects of the interface traps differ from the oxide trapped charge ones. Interface traps have a significant influence on carrier mobility and recombination rates. Bias-dependent trapping or de-trapping of charge at the interface leads to change in sub-threshold swing [21]. Figure 2.6 shows the change in the transfer characteristic due to the interface traps.

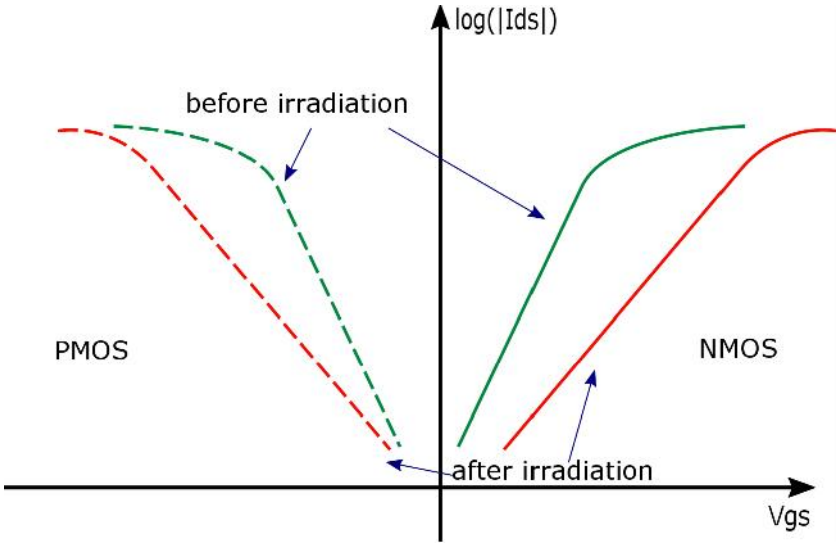

FIGURE 2.6: Transfer characteristic of NMOS (solid line) and PMOS (dashed line) transistors: interface traps influence

The effects of interface and border traps are similar, but their trapping and de-trapping rate is different [22]. Using common measurement techniques it is difficult to differentiate between those two phenomena [23].

In the charge pumping measurement, a technique, used to characterise devices with C-V curves [24], it is expected that the charge recombined per cycle is independent of waveform frequency. However, according to [24], it increases, when frequency is reduced from typical 100 kHz - 1 MHz range down to 10-100 Hz. Over these longer periods of time electrons can tunnel to traps in the oxide and recombine there. These traps are referred to as *border traps* [23].

Due to their slow charge exchange rates, border traps have the major influence on $1/f$ noise of the device, and thus should be considered as a separate phenomenon [21], [23],[25].

Finally, depending on the initial characteristics of the device, the increase in the leakage drain current can be observed, critical for some technologies [21], [26].

Chapter 3

Radiation Hardening Techniques

As soon as one becomes aware of the damage that radiation can cause in ICs, the valid question arises, how to mitigate those effects. The research in the field of radiation hardening has been going on for already over 40 years. While technologies develop, new challenges arise, and different proposals for IC radiation response improvement appear.

As the focus of this work falls onto TID effects, main attention has been paid to techniques that allow to reduce their influence. Generally, one can consider two approaches to radiation hardening: technological one and design one. Although one has seldom influence on process choice, it is still vital to understand advantages and disadvantages of different technologies for radiation tolerance of integrated circuits. On the other hand, there are two ways to improve radiation hardness of an IC at the design level: layout and circuit topology measures. All three aspects are briefly discussed below.

3.1 Technology Considerations

From the point of view of both designer and user, technology choice plays a great role in the expected circuit behaviour. Talking about radiation effects, there is also a strong dependence of the damage on the device size, gate oxide thickness and fabrication process in general.

As already mentioned in the previous chapter, one of the important technology characteristics, influencing radiation hardness of the devices, is the gate oxide thickness. Since

the building of oxide traps happens at the depth of around 3 nm, modern technologies like 0.18 μm and 0.13 μm with oxide thickness of 3.2 nm and 2 nm correspondingly experience minor radiation effects. Thus those technologies are suitable for TID tolerant applications. However, the shallow trench isolation (STI) oxide thickness reaches above 300 nm, which consequently becomes the major location of radiation damage [21]. The studies in [21] also show that silicon on isolator buried oxides technologies proves the least voltage shift, while STI technology damage has the greatest one.

Thus, it can be said, that there is a positive trend in modern small-feature CMOS technologies towards radiation hardness. However, the extra small scales, on their limits have to be investigated closely, as additional effects may appear. Also new problematic, as with leakage currents under STI, must still be addressed.

3.2 Radiation Hard by Design

3.2.1 Layout Techniques

First of all, in general, common "good practice" techniques, like guard rings and distance between devices, ensures better radiation response of ICs. In addition, other transistor topologies can be applied instead of a linear one.

A common-used transistor, as presented in Figure 3.1 (A) is more sensitive to ionization damage. In order to decrease edge currents, one can apply so-called enclosed layout, as presented in Figure 3.1 (B) and (C). Those topologies provide better isolation of the device.

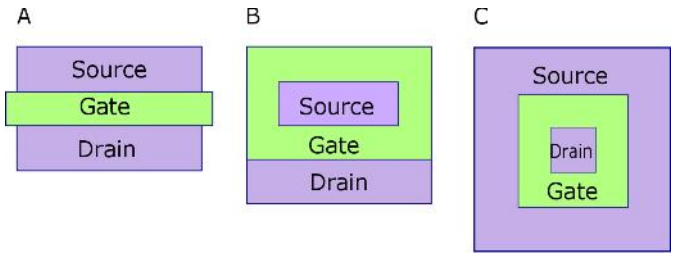

FIGURE 3.1: Linear (A) and annular (B) gate, and enclosed drain (C) transistor layouts

However, modelling of such devices presents additional difficulties. The non-linearity of the channel as well as its asymmetry in case of enclosed drain complicate require the

whole new set of models for all already known effects. So, the circuits using such layout techniques require much design experience and effort, in order to provide predictable required behaviour. Furthermore, increased gate capacitance creates additional challenges for circuit design. Finally, such layouts lead to the increase of chip area, which may become critical for some applications.

3.2.2 Circuit Topology Hardening

The main principle of circuit topology hardening lies in understanding of possible circuit damage. Providing acceptable circuit operation, even after certain degradation of single devices parameters, is a key to radiation tolerant design.

Introduction of redundancy, for instance, increases chances of correct operation after irradiation. Also, there have been proposed various methods of circuit hardening. Among them the so-called inverted-source circuit [27]. First proposed for the phase locked loop, this technique has become popular for hardening of digital circuits in general.

In an inverter, for instance, radiation induced leakage current of the NMOS transistor at logical zero input leads to unexpected voltage drop at the output due to certain r_{on} of the PMOS transistor, as shown in Figure 3.2 (A). This voltage drop leads to energy losses, and, achieving certain value can also lead to false interpretation of the signal.

An inverter cell with inverted source is presented in Figure 3.2 (B). In this case additional inverter consisting of transistors P2 and N2 ensures off-state of the transistor N1 when the input is "low" and thus reduces leakage current, providing correct logical zero even after irradiation, when it becomes more difficult to switch NMOS transistor off.

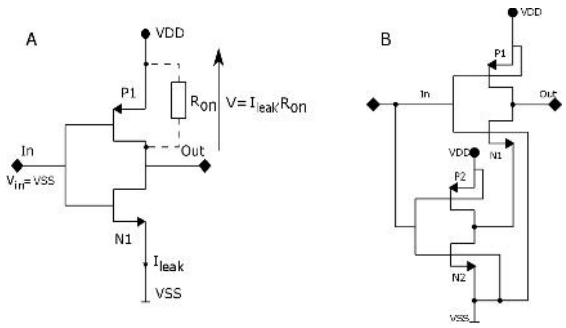

FIGURE 3.2: Radiation induced parasitic effects in an inverter (A) and inverted-source inverter (B)

Chapter 4

Ring Oscillator

As the first step to create a set of guidelines for radiation tolerant IC design, the process capabilities must be analysed. In order to provide such conclusions, some basic structures, easy to model and to explain, have to be used for characterisation. One of such structures is a ring oscillator [28]. Ring oscillator is of an advantage when it comes to characterization of standard building blocks, as for digital design. For small dimension transistors it is hard to measure dynamic characteristics. With ring oscillator one can get this characteristic from the delay measurements. Of course, ring oscillator is not sufficient for the complete technology characterization: one must also implement single transistor structures to be able to observe parameters change. Nevertheless, ring oscillator is very helpful and important for process evaluation circuit.

A simple ring oscillator (RO) consists of an odd number of inverter cells (Figure 4.1). The oscillation frequency depends on propagation time of a single cell and on number of cells [29].

$$F = \frac{1}{2N \times t_d} \tag{4.1}$$

where N is number of inverter stages and t_d is delay time of a single inverter cell. It is defined as follows [29]:

$$t_d = \frac{1}{2} \times (t_{pHL} + t_{pLH}) \tag{4.2}$$

Since delay times at rising t_{pLH} and falling t_{pHL} edges of an inverter are defined by NMOS and PMOS, it is easy to differentiate between the behaviour of both transistors and its influence on ring oscillator parameters. The t_{pHL} and t_{pLH} are inverse proportional to the threshold voltage of NMOS V_{th_n} and PMOS V_{th_p} respectively [29].

In this work two ring oscillators, a standard cell based, and radiation hardened cell based, are compared. Also the inverters, as main building block, are discussed below.

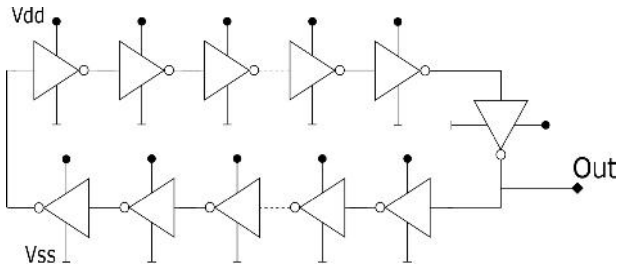

FIGURE 4.1: Ring oscillator

4.1 Standard Inverter Ring Oscillator

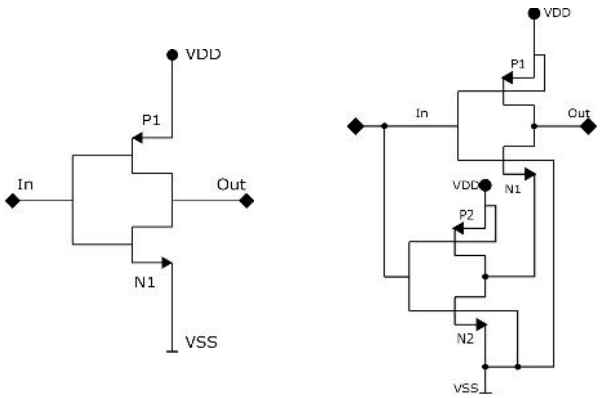

FIGURE 4.2: Inverter cell: standard (left) and inverted-source (right) topology

A usual inverter cell, as presented in Figure 4.2 (left), is the basic building block of the designed ring oscillator. The dimensions chosen correspond to the standard library cell of given technology. Thus, it facilitates characterization of the radiation hardness of the process.

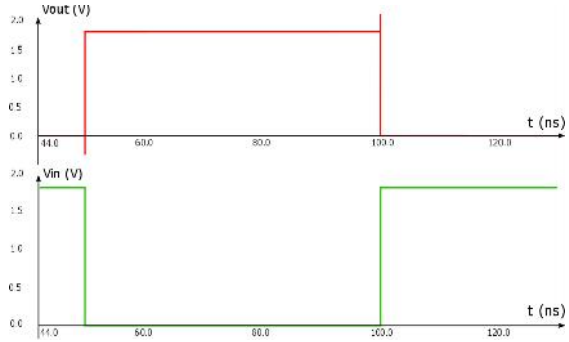

FIGURE 4.3: Simulated transient response of the standard inverter cell, $V_{DD} = 1.8V$, typical conditions

The ring oscillator consists of 151 inverter cells. Transient simulation plot of a single cell is shown in Figure 4.3. The rise time t_r (measured between 10 and 90 percent) of the single inverter cell is 20 ps, and the fall time t_f is 10 ps. The mean delay of the cell t_d is 25 ps. The oscillation frequency of the RO at supply voltage $V_{DD} = 1.8$ V is 128 MHz in typical case.

4.2 Inverted-Source Inverter Ring Oscillator

Radiation hard by design (RHBD) inverted-source inverter cell, as presented in Figure 4.2 (right), basically consists of two inverter stages: one for the basic functionality, and an additional one to make sure the NMOS is switched off at logical "0" at the input.

Inverted-source inverter is significantly slower than the standard one. Thus, fewer cells are needed to achieve the same oscillating frequency. On the one hand, it is an advantage for applications, needing moderate frequencies, on the other hand, it sets limits for high frequency ones. The radiation hardened ring oscillator consists of 75 inverted-source inverter cells. It has been chosen to achieve frequency close to the standard inverter based RO, for the test purposes.

The transient simulation has also been performed for the inverted-source inverter cell. The rise time t_r of the single cell is as for the standard one 20 ps, but the fall time is significantly higher $t_f = 126$ ps, because of the additional inverter stage. The delay time t_d is 56 ps. The oscillation frequency of the RO at $V_{DD} = 1.8$ V is 118 MHz in typical case.

4.3 Comparison of Two Ring Oscillator Designs

The layout of the single standard inverter is shown in Figure 4.4 (A) and the layout of the radiation hardened inverter - in Figure 4.4 (B). As it can be seen, introduction of additional transistors for radiation hardening does not increase the area of the standard inverter layout and thus leads to the chip area decrease when speaking of the whole ring oscillator.

The layouts of the ring oscillators are shown in Figure 4.5. Since the area of the single inverter is the same, and number of cells of the radiation hard by design oscillator is twice less than for the standard cell based one, the total area of the block is also significantly smaller. The area of the standard inverter based ring oscillator is 0.0027 mm^2 and area of the inverted-source cell based one is 0.00175 mm^2.

Thus, for the applications, needing relatively low oscillation frequencies, this radiation hardening technique brings more advantages, than disadvantages. Still, one must consider that for the high frequency applications this method presents critical limitations.

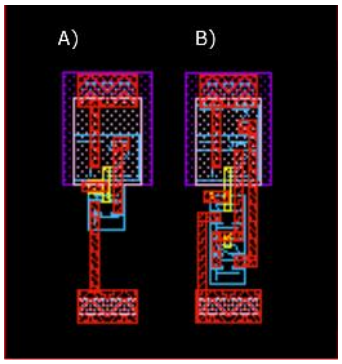

FIGURE 4.4: Layout of the standard (A) and inverted-source (B) inverter

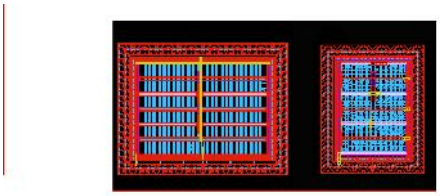

FIGURE 4.5: Layout of the standard (A) and inverted-source (B) inverter based ring oscillators

Chapter 5

Design for Test

As expected from the literature research, the change in oscillating frequency can be dramatic. Thus, it is important to ensure IC operation and testability both before and after irradiation.

To enable accurate and reliable frequency measurement, the circuit must be able to drive the capacitive load of the test probe. For this purpose an output buffer is needed. On the other hand, the output buffer must be fast enough to buffer oscillating frequency even after irradiation, in case it doubles or even triples, due to parameter shift [28].

It is possible to increase the number of inverters in order to decrease the frequency of the oscillator, or to increase the size of a buffer in order to cope with higher frequencies. As a result of optimization process, the decision was made to include also a frequency divider. A single feedback looped D-flip-flop allows to decrease frequency by two. For the same result one would have to double the number of inverters in the ring oscillator. Thus, this approach saves chip area.

In order to be able to switch between two oscillators, the tristate buffer has also been included.

Last, but not least, correct operation of the test structure to measure RO frequency after irradiation must be provided. So, frequency divider and output buffer must be radiation hard. In order to keep the results consistent, the same hardening technique (inverted-source) has also been used for those cells.

Each block has been characterised separately and then the complete test bench was implemented. For block characterization, typical simulations at room and increased (70 C) temperature, as well as process corner simulation has been performed, with supply voltage of 1.8 V. For the test bench only the typical simulation has been done. The number of the cells is over 300, which leads to the very long simulation times. That is why after characterization of each block for the worst case, only the typical conditions functionality has been verified on the top level.

More detailed discussion on each element of the circuit the reader can find in further subsections.

5.1 Frequency Divider

Among the variety of frequency divider (FD) topologies, the one has been chosen for its simplicity and controllability.

Each stage of feedback-looped D-flip-flops divides input frequency by two. The schematic of the block can be seen in the Figure 5.1. The modified radiation hard D-flip-flop is presented in Figure 5.2. The discussed earlier inverted source technique has been applied to NMOS transistors, in order to reduce radiation induced leakage currents.

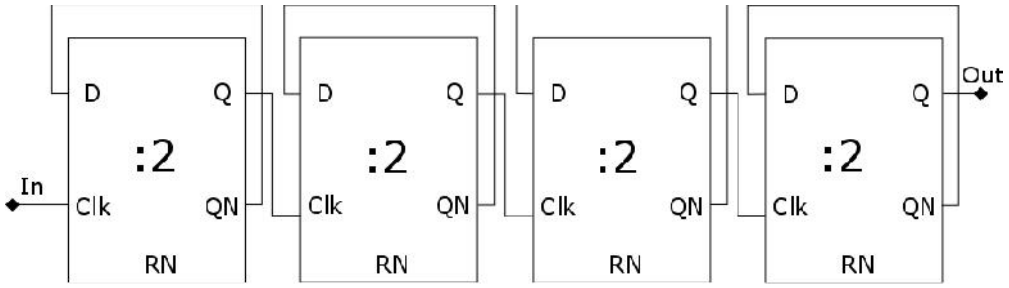

FIGURE 5.1: Frequency divider

The output stage of the flip-flop includes two inverted source inverter cells for signal stabilization. Transistor P5 receives "reset not" signal in order to initiate predefined states of the cell.

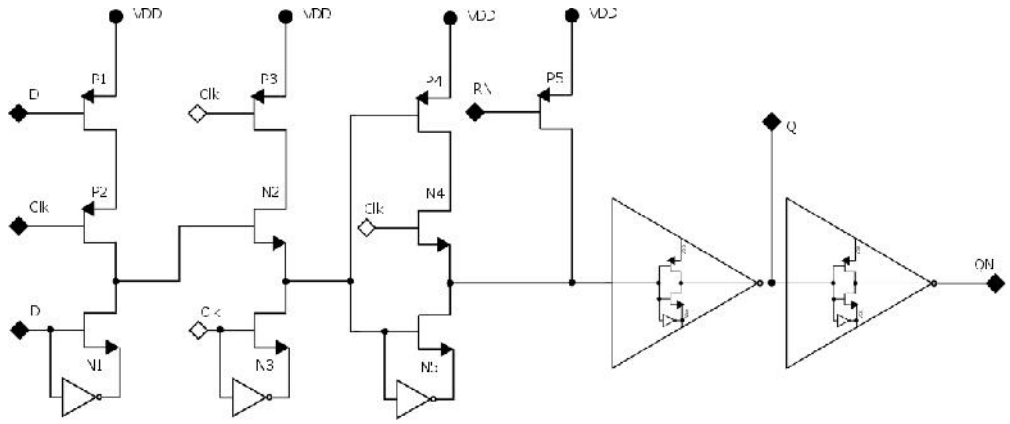

FIGURE 5.2: Modified radiation hard D-Flip-flop with inverted source technique

It has been found out that the behaviour of the radiation hardened by design D-flip-flop strongly depends on the NMOS bulk potential. The isolated devices are available in the given technology. Thus, there are two possibilities of bulk connection for the NMOS transistors with inverted source: to the source or to the ground. Possibility of the different bulk potential for some devices of the circuit creates new opportunities: for instance, radiation response of the devices also depends on bulk bias [30]. For this reason, connection of the bulk to source has also been investigated. However, the simulation has shown that for the correct cell operation the bulk terminal of all NMOS transistors must be connected to ground. Otherwise the capacitance at transistors N1, N3 and N5 is too large, resulting in delays that disturb correct operation of the flip-flop. The transient response of the frequency divider with bulk connected to the source is shown in Figure 5.3.

Once the parasitic capacitance was eliminated from the signal path, the operation was correct. The right transient response of a frequency divider with division factor 8 is shown in Figure 5.4. In this case all NMOS bulks are connected to ground.

For the frequency divider it is important to be able to follow RO frequency. So the worst case for the circuit performance would be the worst speed case of this cell. The cell parameters for typical and worst speed are summarized in Table 5.1.

TABLE 5.1: Simulated parameters of frequency divider

	typical 27 C	worst speed 27 C	worst speed 70 C
t_r, ps	164	171	189
t_f, ps	125	134	149
$f_{in_{max}}, GHz$	6.9	6.5	5

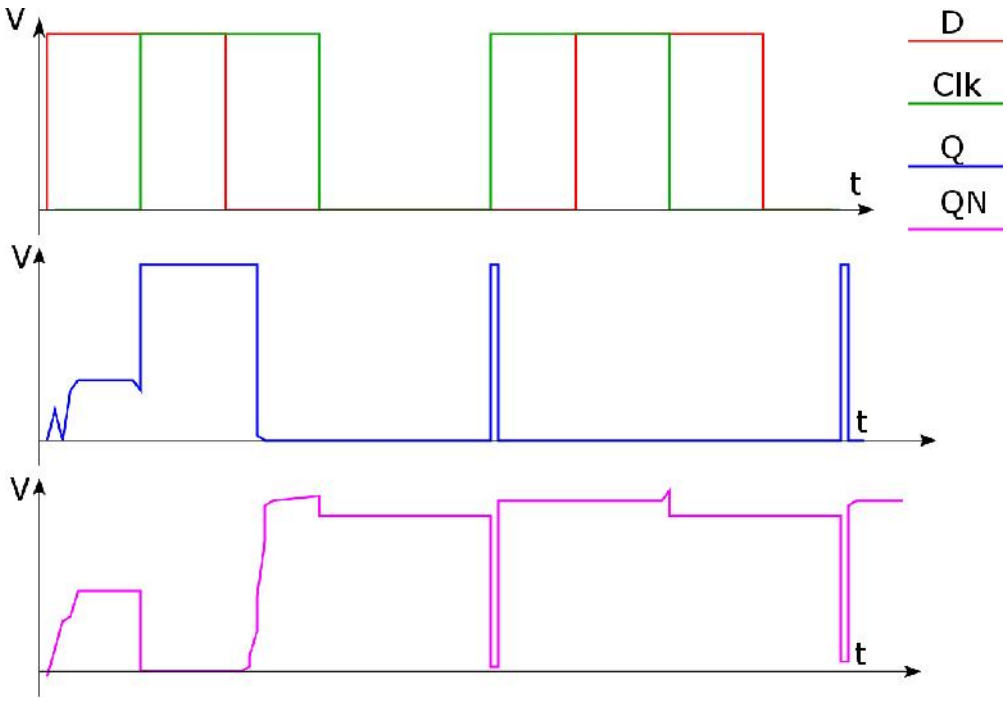

FIGURE 5.3: Demonstration of a D-Flip-flop functionality problem with NMOS bulk connected to source

FIGURE 5.4: Simulated transient response of a frequency divider, $V_{DD} = 1.8V$

5.2 Tristate Buffer

In order to be able to measure test structures with a single output buffer, the tristate buffer has been chosen as a logical unit. The choice has fallen onto this cell, in order to leave some flexibility at the top level of the chip. Multiplexer or NAND gates assume

predefined number of inputs and are complex. The use of tristate buffer, which is relatively small allows integration of multiple oscillators, even if it was not planned initially. However, the danger of enabling few cells at a time is a drawback of this choice, which has to be carefully considered at test.

In this work there are two tristate buffers connected to either standard inverter based or radiation hardened ring oscillator. Same as for other blocks, inverted source technique was applied to critical nodes. Figure 5.5 presents the schematic of this block. The inverted-source technique in this case was used for the input and output stages. The probability of malfunction due to leakage current in the path from P3 to N3 was considered as insignificant.

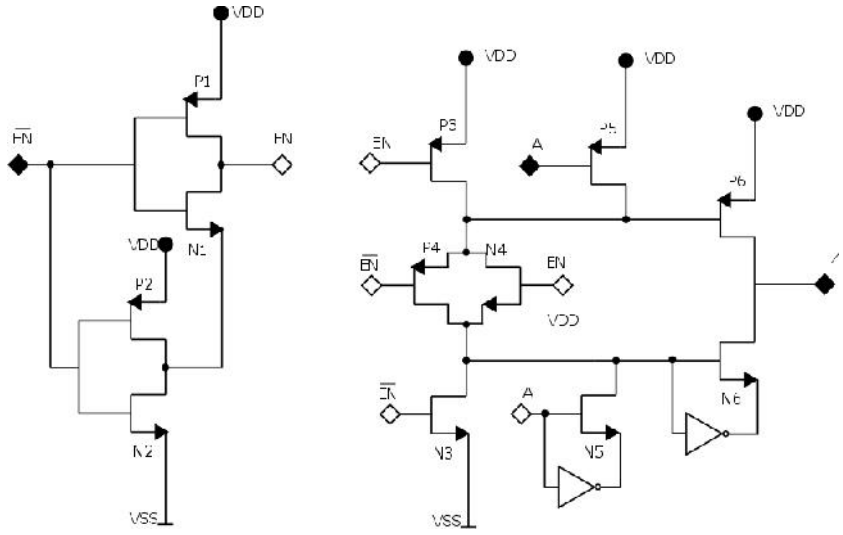

FIGURE 5.5: Circuit of modified radiation hardened tristate buffer with inverted-source technique

For the tristate buffer, the worst case conditions are the same as for the described above frequency divider. The results of the simulations are listed in Table 5.2. For both ring oscillators frequency divided by 16 with the help of frequency divider does not exceed 9 MHz, which means the tristate buffer will be able to buffer the signal correctly

TABLE 5.2: Simulated parameters of tristate buffer

	typical 27 C	worst speed 27 C	worst speed 70 C
t_r, ns	111	113	119
t_f, ns	69	79	79
$f_{in_{max}}, MHz$	11	10.4	10.1

5.3 Output Buffer

Finally, the output buffer consists in total of 126 double inverter stages and 3 single ones. It allows to drive capacitive load up to 100 pF at input frequency up to 10 MHz. Inverter cells with inverted-source have also been used in this device. The schematic of the block is presented in Figure 5.6.

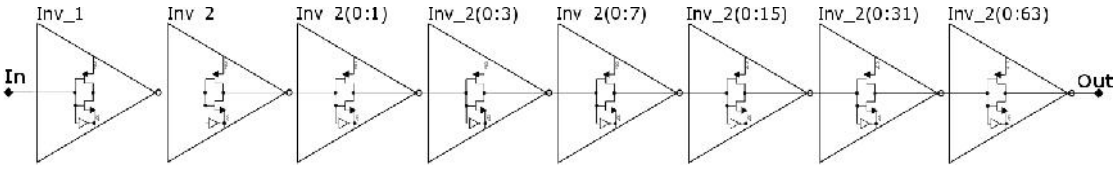

FIGURE 5.6: Output buffer

The transient response of the output buffer is presented in Figure 5.7. Input signal frequency of 10 MHz at supply voltage of 1.8 V has been applied. Above mentioned load of 100 pF has been used. The peak current of the output buffer reaches 120 mA, which must be considered for the layout.

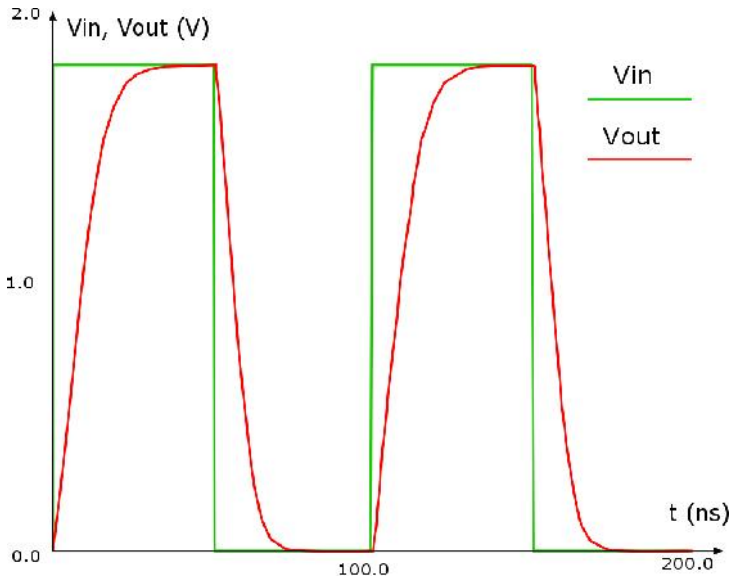

FIGURE 5.7: Simulated transient response of the output buffer: $V_{DD} = 1.8V$, $C_{load} = 100pF$, $f_{in} = 10MHz$

Finally, the parameters of the output buffer under the load of 100 pF are summarized in the Table 5.3.

TABLE 5.3: Simulated parameters of output buffer with 100 pF load

	typical 27 C	worst speed 27 C	worst speed 70 C
t_r, ns	115	119	122
t_f, ns	73.6	77.1	78
$f_{in_{max}}, MHz$	10.6	10.2	10.0

5.4 Top Level

The schematic of the top level circuit is shown in Figure 5.8. Frequency divider with division factor 16 and a tristate buffer are implemented in each RO path. The output signal corresponds consequently either to standard cell based or inverted source cell based RO, dependent on the tristate buffer selection. The tristate buffer is introduced after the frequency divider because of the speed limitations of the cell.

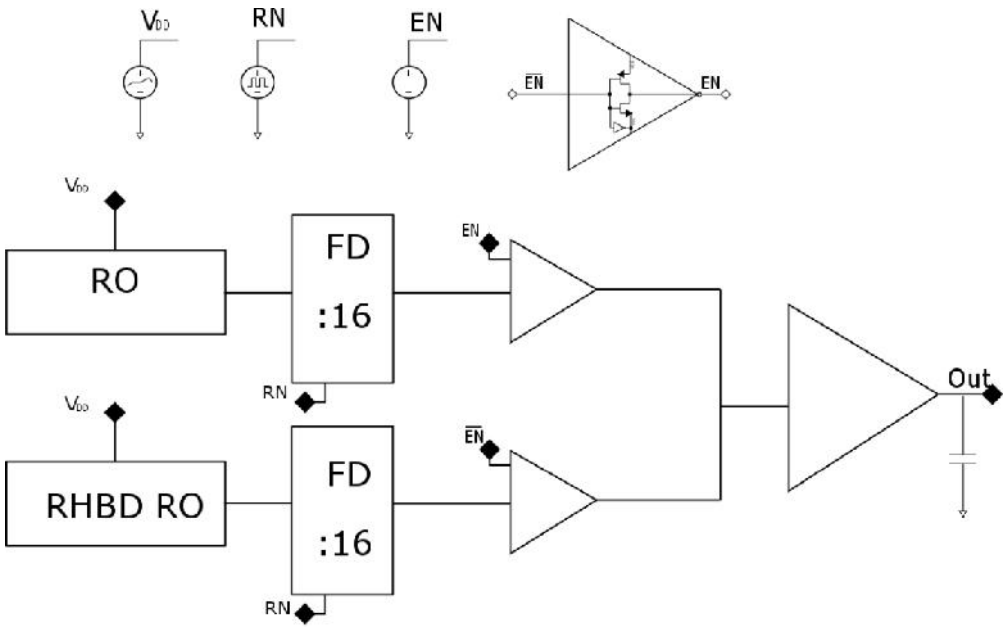

FIGURE 5.8: Schematic of the top level

Another important point of the test bench design is power supply ramp, driving start-up. If the speed of the ramp approaches nominal oscillating frequency, two different states can propagate over the circuit, in case the threshold voltage and input capacitance of two or more inverters approaching equal. The sketch in Figure 5.9 demonstrates normal (A) behaviour and behaviour in case of too fast start up (B) for a simplified ring oscillator consisting of 5 inverter stages.

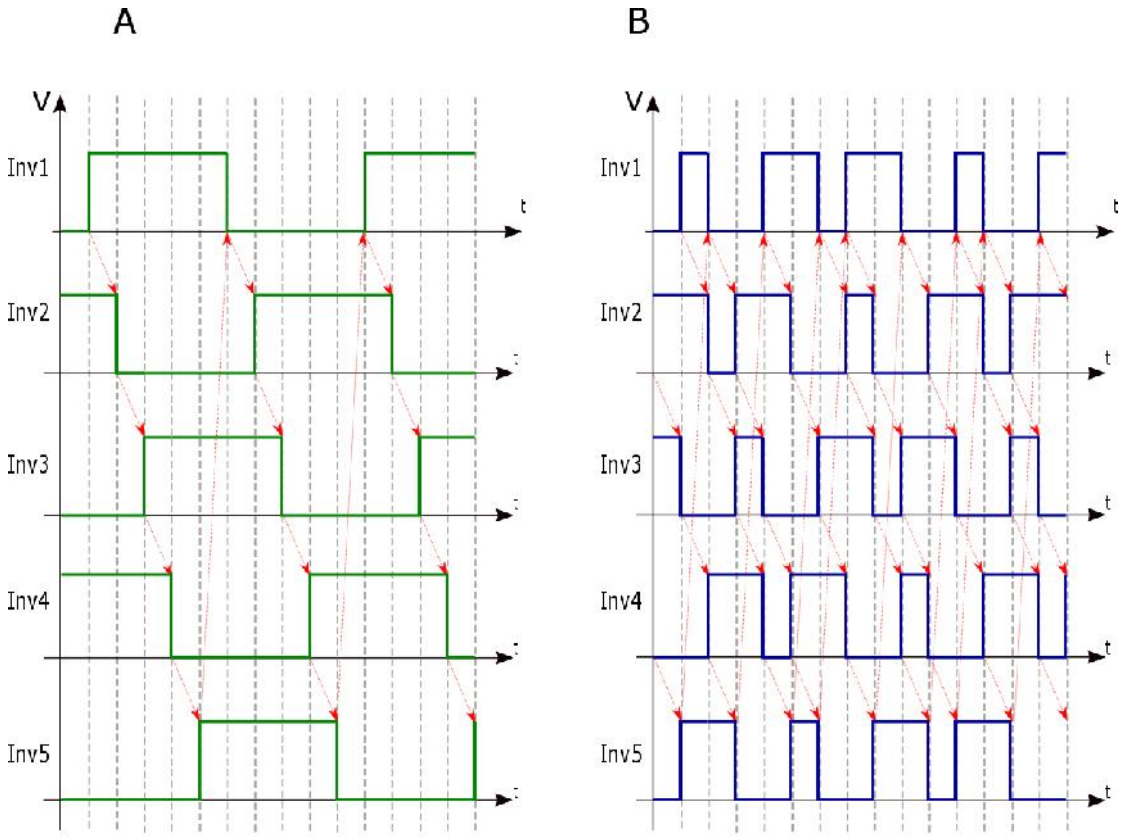

FIGURE 5.9: Demonstration of a 5-stage ring oscillator normal operation (A) and functionality problem in case of too fast start-up (B)

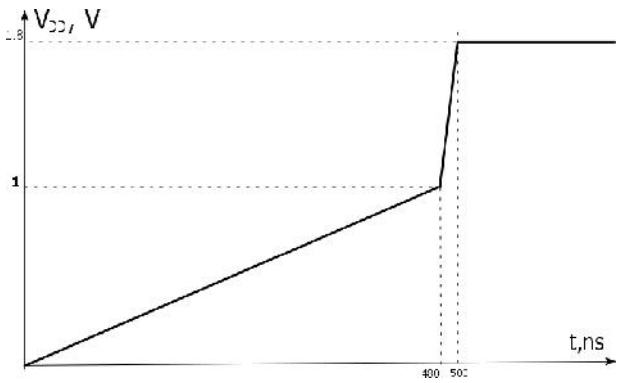

FIGURE 5.10: Power supply ramp up of the top level

In case of 128 MHz oscillating frequency, if the speed of the ramp approaches 10 ns, this phenomenon is almost sure to occur. However, this is not an issue for the real sample measurements in the future, since the speed of the real power source is much lower than the designed oscillating frequency: some hundreds of milliseconds. So, for the simulation test bench, in order to keep the simulation times short, but still achieve reasonable results, the ramp as it is shown in Figure 5.10 has been implemented for VDD source.

The transient response of the top level, presented in Figure 5.8, is shown in Figure 5.11. Here V_{ro} is signal of the standard inverter based RO, $V_{rhbd\ ro}$ in RHBD RO output, $V_{FD_{ro}}$ and $V_{FD_{rhbd\ ro}}$ are signals after frequency division of RO and RHBD RO correspondingly, $V_{tristate}$ and V_{out} are outputs of the enabled tristate buffer, connected to RHDB RO and of the output buffer correspondingly.

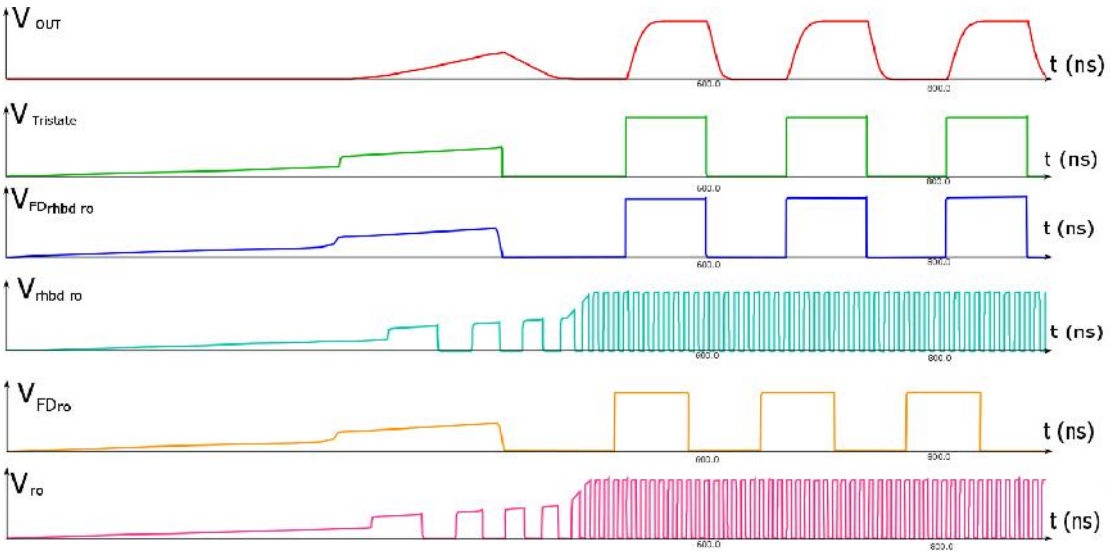

FIGURE 5.11: Simulated transient response of the top level schematic at $V_{DD} = 1.8V$

The "worst case" process condition parameters of the designed blocks are listed in Table 5.4. The frequency of the ROs is given for the worst case power (thus, the highest one), whereas the frequency for the tristate and output buffers means the highest possible buffered frequency in case of worst speed. The frequency of the FD is maximal dividable frequency of the RO.

TABLE 5.4: Summary of simulated top level designed blocks parameters

	t_r, ps	t_f, ps	f, MHz	Note
Inverter	30	20	—	t_r, t_f are delays at the rising...
RHBD inverter	30	84	—	...and falling edges
Ring oscillator	—	—	128.8	
RHBD RO	—	—	118.1	
FD	190	150	5000	t_r, t_f are rising and falling times
Tristate buffer	119×10^3	79×10^3	10	
Output buffer	122×10^3	78×10^3	10	maximal frequency at 100pF load

Chapter 6

Modelling of TID Response of the Ring Oscillators

6.1 Single Device Effects Simulation

As discussed above, there are two most significant consequences of the TID damage in a transistor: threshold voltage shift and increase in a leakage current. In order to predict circuit behaviour, a single device radiation response has to be analysed.

The values of parameter change have been extracted with the help of multiphysics finite element method (FEM) radiation simulation tool ECORCE[1] as well as from the literature. A simplified 1-D model of a transistor, has been created and a total dose of 130 krad was simulated. The model of the device is presented in Figure 6.1. Simulation of the dose rate of 8.5 rad/s and 4 hours exposure has been performed.

FIGURE 6.1: 1-D model of a MOS transistor

As it can be seen in Figure 6.2, the threshold voltage of NMOS decreases, thus leading to complication of switching the transistor off. The change in PMOS threshold voltage is also negative, thus making it greater in absolute value. However, the change in the

[1] http://ecorce2d.free.fr/

V_{th} is not significant, due to the low thickness of the gate oxide.

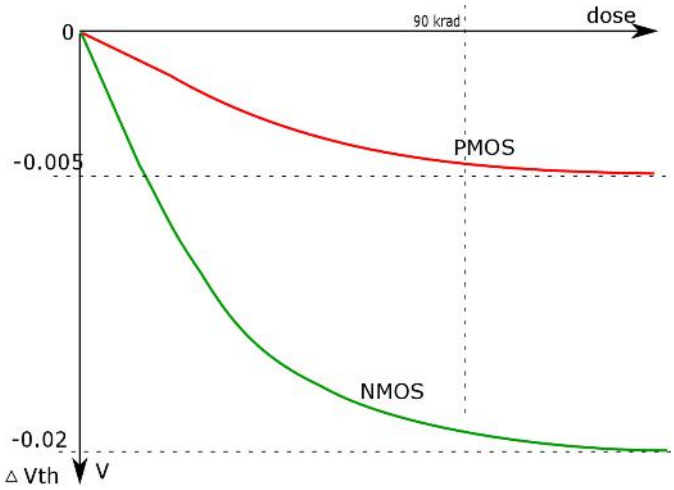

FIGURE 6.2: Threshold voltage shift of the PMOS and NMOS transistors obtained with ECORCE for TID 130 krad

Since the gate oxide thickness is less than 5 nm, the major TID caused dark current appears not in the "as drawn" transistor, but is caused by parasitic device. Figure 6.3 shows the leakage current path and parasitic MOS devices, composed by STI. Since the thickness of STI oxide for commercial technologies reaches over 300 nm, this part of the chip experiences much higher damage. The charge build up at the side wall of the shallow trench isolation causes additional leakage I_{ds}.

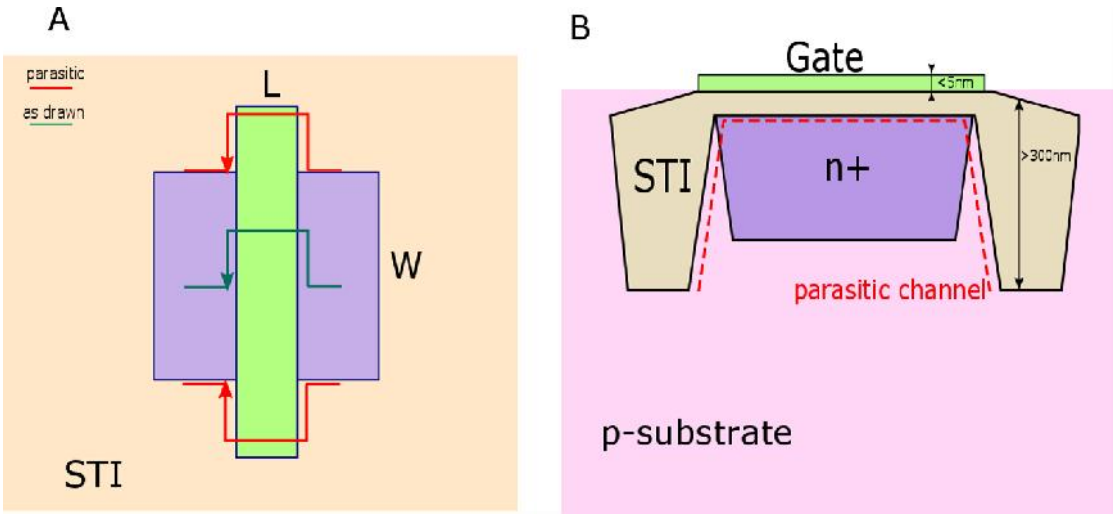

FIGURE 6.3: Leakage current path (A) and cross-section of a transistor with STI (B)

Finally, as it has been found out from the literature [21], [28], [15], [31] the parameters changes can be much more significant in the real life. Thus, the values from

the literature have been taken for further simulations, as the worst case condition: $\Delta V_{th_n} = 0.3V, \Delta V_{th_p} = 0.1V, I_{leak} = 1\mu m$.

So, the simplified model of NMOS and PMOS, as shown in Figure 6.4, is proposed, where current source represents leakage current and voltage source represents threshold voltage shift. Since the dark current of PMOS does not change significantly (it stays in order of initial leakage current) [15], it can be neglected.

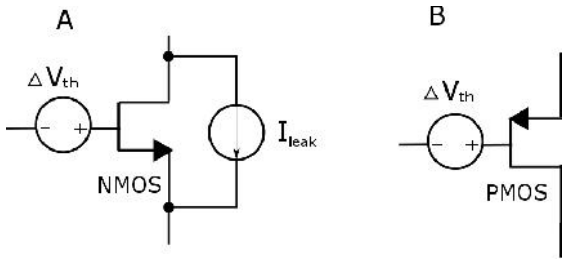

FIGURE 6.4: Macro-model of NMOS(A) and PMOS (B) after irradiation

6.2 Radiation Effects on a Single Inverter Cell

The simplified model of the considered above effects can be defined for the inverter cell as in the Figure 6.5, where voltage sources represent V_{th} shift and current source represents radiation induced leakage current.

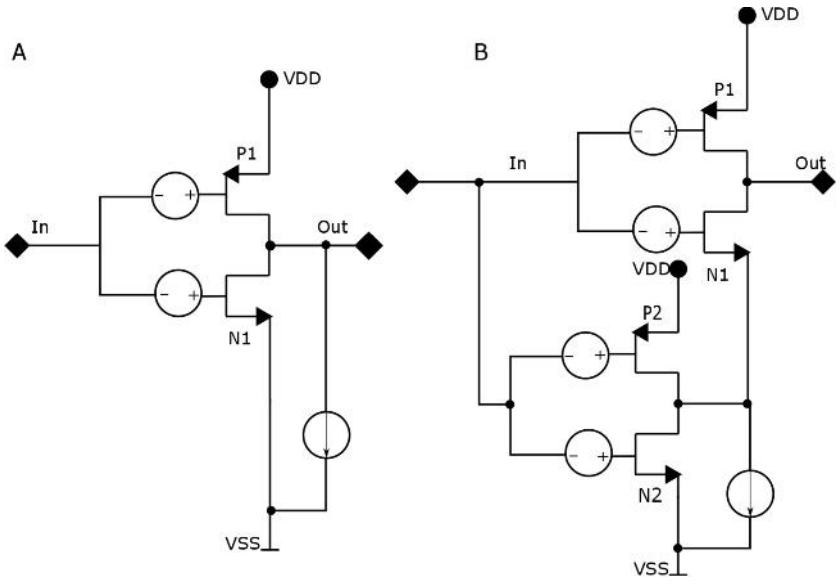

FIGURE 6.5: Macro-model of the radiation effects on inverter cell (A) and inverted-source inverter cell (B)

In order to analyse change in the cell behaviour, the transfer functions of the inverters before and after irradiation have been compared. Total dose in this case equals 130 krad. For digital circuits, correct voltage levels of logical 1 and 0 and the steepness of the transfer function are very important. The change in these parameters have been observed and analysed.

Since inverted-source technique is meant to mitigate dark current, only this parameter was included in order to see the advantages this technique brings. For demonstration purpose, the simulated dark current has been chosen 10 μA. The Figure 6.6 shows the difference between radiation response of standard and radiation hardened inverters. As one can see, the output voltage of the standard inverter does not reach 1.8 V any more, whereas the RHBD one still operates correctly. Still, there is some change in the transfer function of the inverted source inverter. It is explained by leakage current of the additional inverter, which leads to false voltage at its output and thus to some additional voltage drop, allowing leakage current of the main inverter to flow.

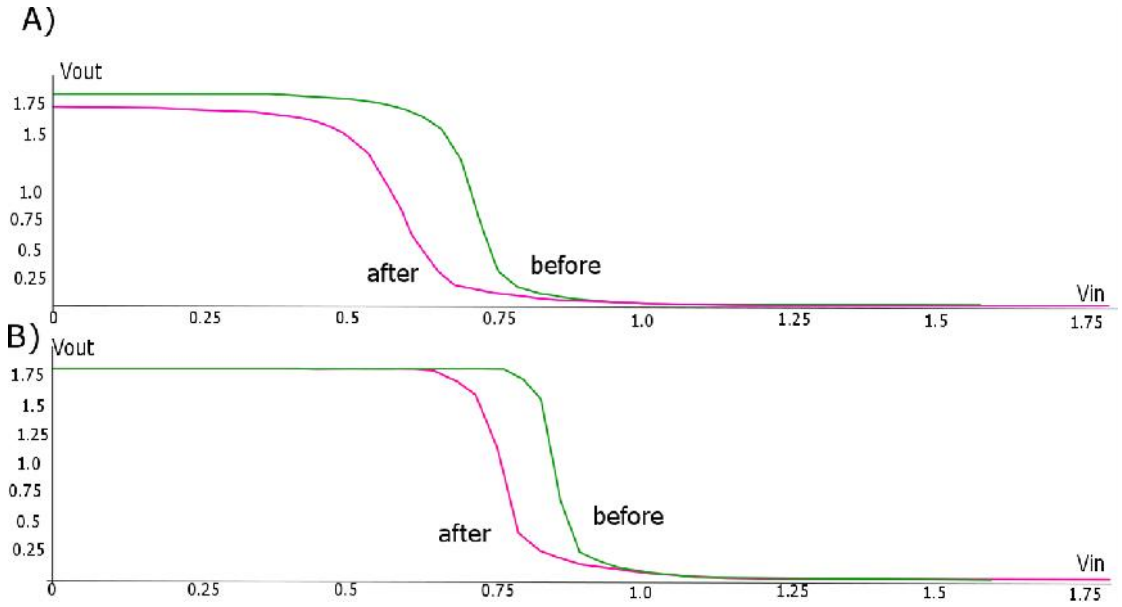

FIGURE 6.6: Transfer function of the standard (A) and inverted-source (B) inverter cells before and after irradiation: 10 μA NMOS leakage current influence

Next, in order to draw conclusions about circuit operability after irradiation, all parameters have been included into simulation. For this simulation the maximal values of the threshold shift (300 mV for NMOS and 100 mV for PMOS) have been taken, and the leakage current value is 1 μA, because of the small size of the transistor. Figure 6.7 shows that change in the RHDB cell is significantly less than in the standard one. One can see that in this case V_{th} shift has greater influence on the cell parameters.

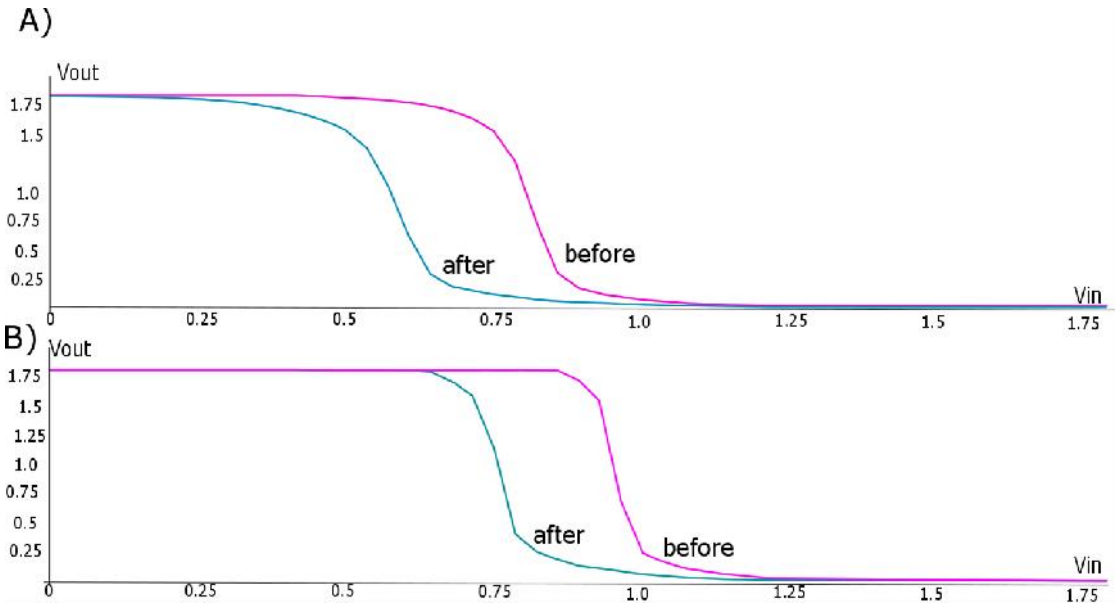

FIGURE 6.7: Transfer function of the standard (A) and inverted source (B) inverter cells before and after irradiation: $I_{leak} = 1\mu A$, $\Delta V_{th_n} = 0.3V$ and $\Delta V_{th_p} = 0.1V$ influence

Additionally, transient analysis has been performed. Both inverters show decrease in the mean delay time: by 8 percent for the standard inverter, and by 12 percent for the RHBD one. It means consequent increase in the oscillation frequency of the RO. The radiation response of the ring oscillator is discussed in the following subsection.

6.3 Effects of Radiation on Ring Oscillators

As the electrical parameters of the single devices change, the circuit characteristics change as well. In this section, two approaches to the TID effects on ring oscillators modelling are implemented. First, analytical model, taking into account V_{th} shift [28], has been applied. Further, proposed model of the inverter cell has been applied to simulate ring oscillator radiation response. The discussion of the obtained results follows in the next section.

6.3.1 Analytical Model

The frequency of ring oscillator is defined as [28]:

$$F = \frac{1}{2N \times t_d} \tag{6.1}$$

where N is number of inverter stages and t_d is delay time of a single inverter cell. It is defined as follows [28]:

$$t_d = \frac{1}{2} \times (t_{pHL} + t_{pLH}) \tag{6.2}$$

where delay time of the inverter at falling edge t_{pHL} depends on NMOS parameters and delay time at rising edge t_{pLH} on PMOS as follows [28]:

$$t_{pHL} = \frac{C}{\mu_n C_{ox} (\frac{W}{L})_n V_{DD}} a_n \tag{6.3}$$

$$t_{pLH} = \frac{C}{\mu_p C_{ox} (\frac{W}{L})_p V_{DD}} a_p \tag{6.4}$$

and a_n and a_p are defined as follows [29]:

$$a_n = \frac{8V_{DD}^2}{7V_{DD}^2 - 12V_{DD}V_{th_n} + 4V_{th_n}^2} \tag{6.5}$$

$$a_p = \frac{8V_{DD}^2}{7V_{DD}^2 - 12V_{DD}|V_{th_p}| + 4V_{th_p}^2} \tag{6.6}$$

Some parameters of equations (6.3)−(6.6) are considered unchangeable with increasing TID: oxide capacitance C_{ox}, device linear sizes W, L, supply voltage V_{DD}, mobility of NMOS and PMOS μ_n and μ_p, and output capacitance of the inverter C [28]. Thus, according to this model, the change in the ring oscillator behaviour depends only on threshold voltage V_{th} shift of NMOS and PMOS, as in equations 6.5 and 6.6.

After substituting values of V_{th} for few TID levels into 6.5 and 6.6 for standard inverter based ring oscillator the expected change in the circuit behaviour is presented in Figure 6.8, where the oscillating frequency is plotted over TID step, corresponding to threshold voltage shift, as shown in Figure 6.9. The threshold voltage shift reaching maximally 0.3 V for NMOS and 0.1 V for PMOS, as discussed in previous chapter. The curve form was approximated in MatLab environment accordingly to the results of the ECORCE simulation.

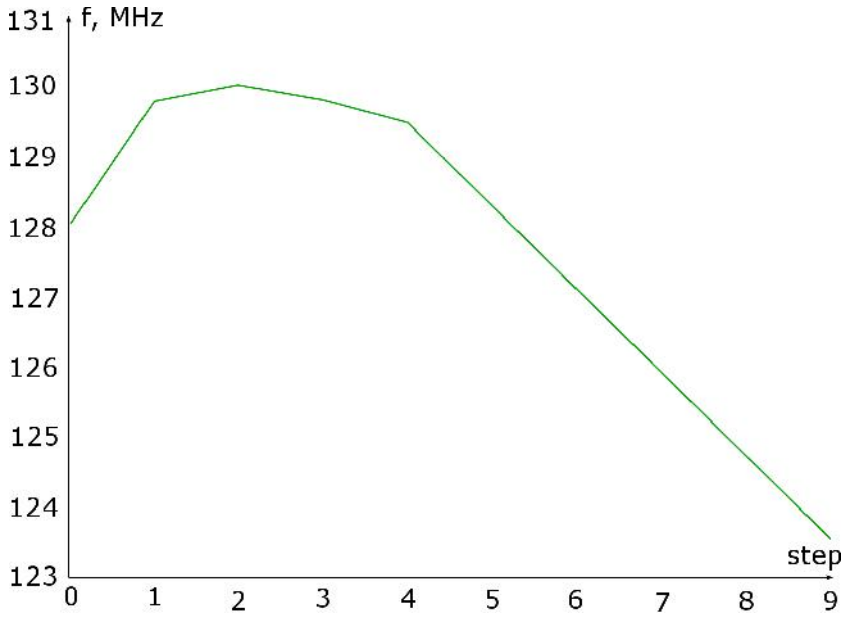

FIGURE 6.8: Expected frequency of the standard inverter based ring oscillator after irradiation obtained from analytical model

The initial increase in the frequency is explained by decrease of the V_{th_n} as it is significant already at low irradiation doses. The following decrease starts at the dose, where change in V_{th_p} becomes grater than the one of NMOS. As threshold voltage for both transistors becomes more negative, for PMOS it means increase of the magnitude, which consequently means increase of t_{pLH} and thus the decrease of the oscillation frequency.

Table 6.1 summarizes influence of the threshold voltage shift of PMOS and NMOS on cell delays and on oscillation frequency correspondingly.

However, this theoretical model does not cover the influence of the leakage current. Consequently, it cannot show improvement of the circuit radiation response due to inverted-source technique, as leakage current is the effect mitigated by this approach. That is why the following subsection presents Cadence-Spice simulation results on circuit level,

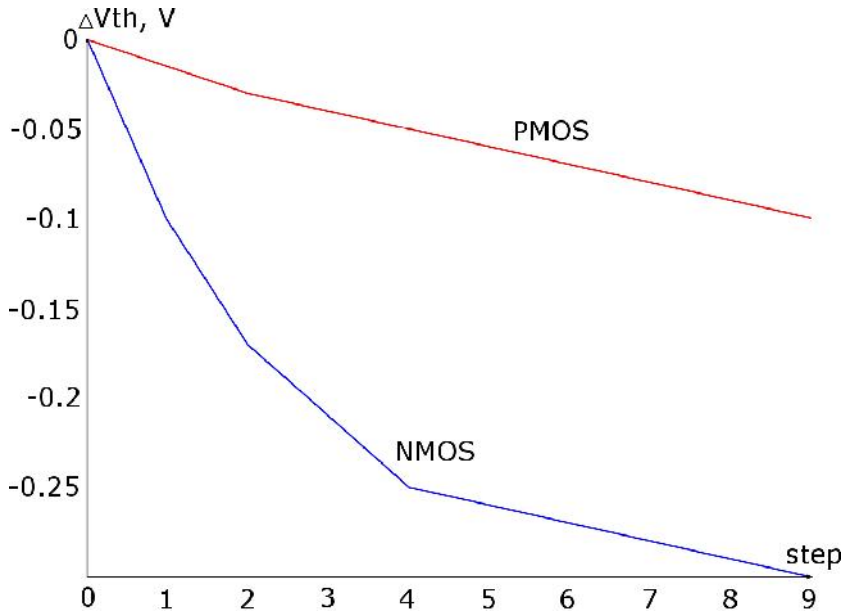

FIGURE 6.9: Threshold voltage shift used for frequency change calculations

TABLE 6.1: Radiation response of the standard inverter based ring oscillator according to analytical model

Dose step	V_{th_n}, mV	t_{pHL}, ps	V_{th_p}, mV	t_{pLH}, ps	t_d, ps	f, MHz
0	355	13.42	-450	38.31	25.87	128
1	255	11.95	-465	39.09	25.51	129.8
2	185	11.07	-480	39.87	25.47	130
3	145	10.65	-490	40.41	25.51	129.81
4	105	10.18	-500	40.96	25.57	129.49
5	95	10.07	-510	41.53	25.80	128.33
6	85	9.98	-520	42.11	26.04	127.15
7	75	9.88	-530	42.70	26.29	125.96
8	65	9.78	-540	43.31	26.54	124.75
9	55	9.68	-550	43.93	26.81	123.52

using presented in Figure 6.5 macro-model and compares obtained data with theoretical calculations done in this chapter in order to evaluate degree of influence of the dark current on radiation response of the ring oscillator.

6.3.2 Simulation of the Radiation Effects on Ring Oscillators

In order to perform comparative analysis of two ring oscillator topologies, the circuit-level simulation, including radiation effects, has been carried out. The simulation has been performed in the Cadence analog simulation environment. The change in the devices' parameters is presented by the piecewise linear voltage and current sources,

instead of DC sources as in Figure 6.5. Thus, modelled case represents changes in the circuit behaviour when exposed to radiation during operation.

The frequency change over time for standard inverter based RO and for RHBD RO is shown in Figure 6.10 and Figure 6.11 correspondingly. As expected from the single inverter simulation results, because of the delay time decrease, the frequency increases for the whole irradiation period, unlike computational results, presented in previous subsection. It has to be also mentioned that radiation induced increase in the leakage current has significant effect on ring oscillator, as it has been seen on the block level simulation. However, introduction of inverted source topology increases the influence of the threshold voltage shift on the oscillating frequency.

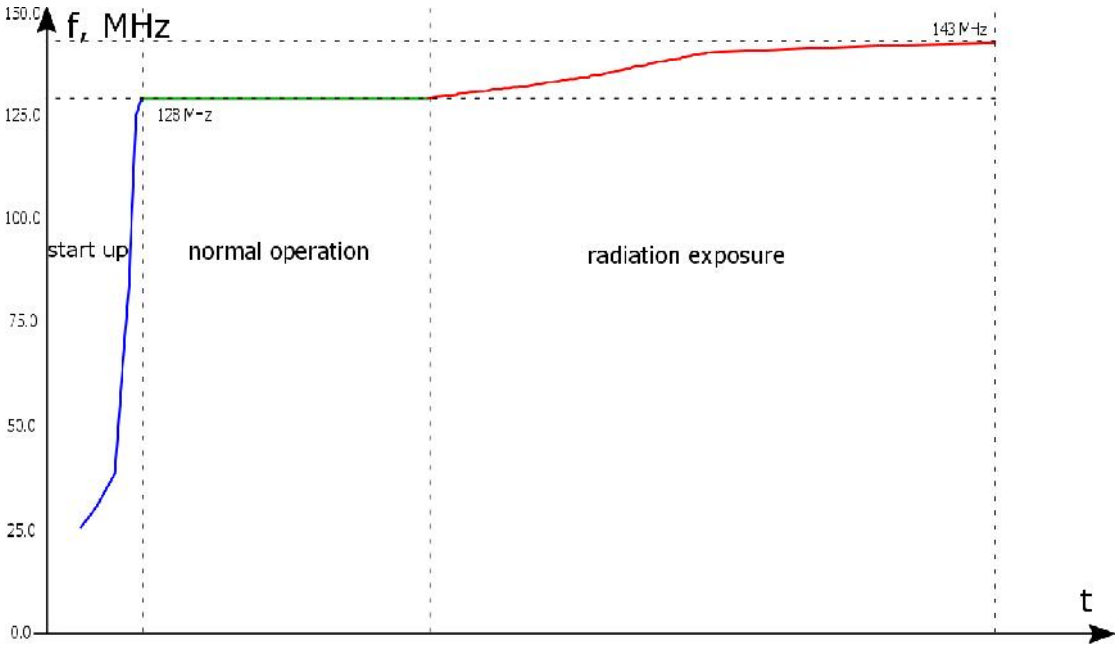

FIGURE 6.10: Simulation results: frequency of the standard inverter based ring oscillator under radiation with radiation induced $I_{leak} = 0..1\mu A$, $\Delta V_{th_n} = 0..0.3V$ and $\Delta V_{th_p} = 0..0.1V$, and $V_{DD} = 1.8V$

Table 6.2 presents the summary of the parameters of the designed blocks: inverter (Inv), inverted source inverter (RHBD Inv), ring oscillator (RO), RHBD ring oscillator, oscillators signals after frequency division (RO FD and RHBD RO FD correspondingly), frequency divider (FD), tristate buffer (TrBuf) and output buffer (OutBuf) before and after irradiation.

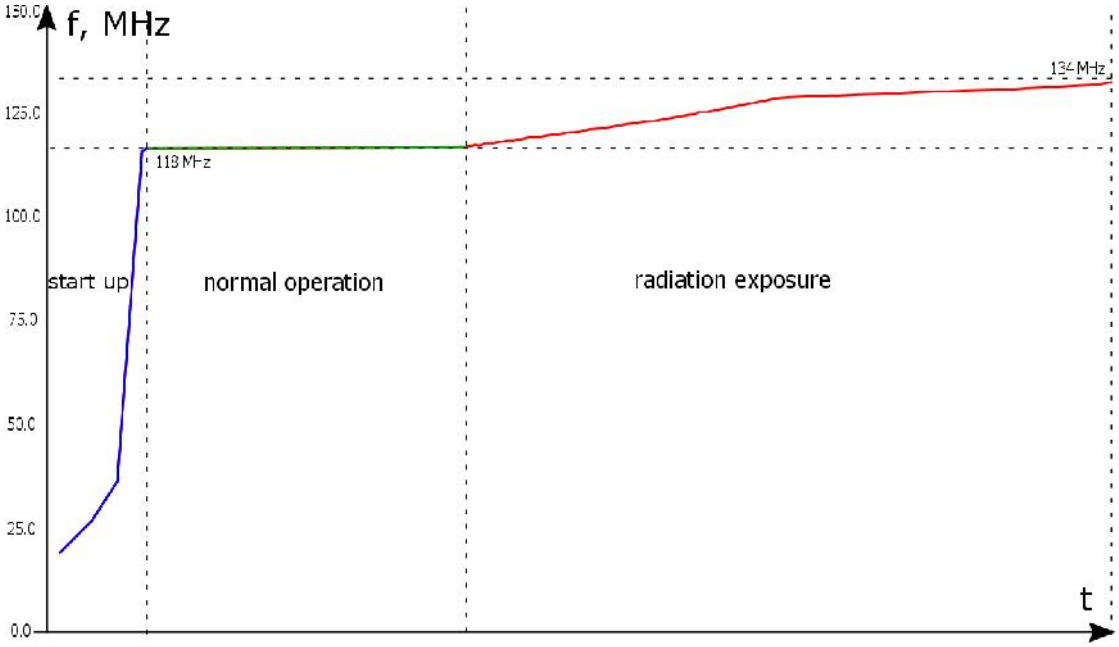

FIGURE 6.11: Simulation results: frequency of the RHBD ring oscillator under radiation with radiation induced $I_{leak} = 0..1\mu A$, $\Delta V_{th_n} = 0..0.3V$ and $\Delta V_{th_p} = 0..0.1V$, and $V_{DD} = 1.8V$

TABLE 6.2: Results of simulation: parameters of the test structures before and after irradiation and parameters of the output stage blocks

Test Structures				Notes
		t_d, ps	f, MHz	
Inv	before	25	—	$V_{DD} = 1.8V$,
	after	23	—	typical conditions
RHBD	before	56	—	$V_{DD} = 1.8V$,
Inv	after	49	—	typical conditions
RO	before	—	128	$V_{DD} = 1.8V$,
	after	—	143	typical conditions
RO FD	before	—	8	$V_{DD} = 1.8V$,
	after	—	8.9	typical conditions
RHBD	before	—	118	$V_{DD} = 1.8V$,
RO	after	—	134	typical conditions
RHBD	before	—	7.375	$V_{DD} = 1.8V$,
RO FD	after	—	8.375	typical conditions
	Output	Stage		
	t_d, ns	t_f, ps	$f_{in_{max}}$, MHz	
FD	0.189	0.149	5000	worst speed, 70C
TrBuf	119	79	10.1	worst speed, 70C
OutBuf	122	78	10.0	worst speed, 70C, $C_{load} = 100pF$

6.4 Results Discussion

First of all let us compare the two models. The analytical model describes exactly the influences of each threshold voltage shift. However, it does not take into account the leakage current and also must be extrapolated for inverted source inverter based ring oscillator. Furthermore, it does not take into account additional geometry dependent effects, like short channel effects. In small feature technologies, threshold voltage can vary dramatically for different sizes of devices.

The macro-model, implemented in Cadence, in turn, demonstrates advantages of the inverted source inverter in comparison to the standard one. The more detailed model of the device parameters is one more advantage of this modelling approach. However, it still has some drawbacks as for the use in characterisation of the ring oscillator. The use of ideal current sources does not exactly represent the phenomenon of leakage current in this circuit. Even at the off state, the current is forced, thus corrupting the actual parameter values.

As one can recall, for same input parameter range (I_{leak}, ΔV_{th_n} and ΔV_{th_p}) the trend in the oscillation frequency change is different for computed and simulated models. Nevertheless, the mechanism of change is the same. However, as different results show, the exact analytical model behind the delay time of the inverter still has to be adapted. The short channel effects must be taken into account. Eventually, the origin of the dark current influence, causing additional voltage drop, must be included.

Thus, as the next step in the TID effects research the Verilog A model can be created in order to simulate all parameters changes accordingly to their physical nature, e.g. ensuring $I_{leak} = 0A$ when $V_{GS} = 0V$.

Finally, coming back to the circuit design, the inverted-source inverter has been proved to be more robust against radiation induced changes in the dark current. However, the threshold voltage shift of additional structure contributes to parameters degradation at the higher circuit levels, in this case influences frequency of the ring oscillator.

The relative change in frequency for both topologies, although it is caused by different effects, is still eleven to thirteen percent. Thus, the inverted-source inverter does not improve radiation hardness of the ring oscillator, while it shows significant improvement of the single inverter cell.

Conclusions

The radiation hardness is very topical for a vast number of applications. In particular, integrated circuit for medical imaging suffer from radiation effects. A computed tomography scanner electronics is exposed to the total dose of 120 to 160 krad over the lifetime. The effects of this exposure can lead to severe damage, as discussed in Chapter 2.

In this work, a background for a given CMOS technology radiation hardness characterisation has been created. For this purpose, two ring oscillators were designed: a standard cell based one, with oscillating frequency of 128 MHz, and radiation hardened one, with oscillating frequency of 118 MHz. Special attention has been paid to the circuitry operability after irradiation. In order to ensure this correct operation, the output stage and the output frequency of the oscillators have been optimized. A radiation tolerant frequency divider with division factor 16 and input frequency range up to 5 GHz, tristate buffer and output buffer, both capable of driving frequencies up to 10 MHz with capacitive load of 100 pF, have been designed. It has been ensured that the output stage can drive ring oscillators signals even after parameter degradation after irradiation, allowing change in oscillating frequency to reach up to 30 percent.

The models, implemented in this work, have been proved useful for preliminary analysis of circuit radiation response. The ECORCE simulator has been used for device radiation response simulation. The trend in the threshold voltage shift has been observed. It has also been found out that the main part of leakage current is the STI dark current, since the thickness of the STI is significantly higher than the one of the gate oxide, therefore free holes cannot easily escape the volume and lead to parasitic electric field. On the circuit level, two approaches have been investigated: the computational model according to [29] and simulation model as presented in Chapter 6, section 2. The analytical model shows direct relation of the irradiation influenced parameters to the oscillation

frequency and helps to differentiate between NMOS and PMOS contributions to the circuit behaviour. Thus, it can be used as additional method for understanding radiation effects in CMOS, especially in standard logic gates. The Cadence simulation macro-model can further be used for preliminary analysis of circuit radiation hardness at the design stage. It has also shown importance of the additional effects, such as short channel effect, which is not taken into account in the mentioned above computational model.

Also, the radiation hardening technique "inverted source" has been tested. As it is known from the literature research, this method is efficient for radiation induced increase of the dark current mitigation. The leakage current of 10 μA has been simulated, and the transfer function of the inverter has been evaluated. The inverted source inverter has shown correct behaviour, reaching both VDD and VSS, whereas the standard cell logical high reached only 1.72 V. However, going beyond CT applications, at higher dose levels, the value of the current can eventually exceed 20 μA, and the change in the output voltage can consequently lead to the wrong interpretation of the signal.

This technique has also been implemented for the output stage design. The correct operation of the cells shows universality of the inverted-source design for digital cells. Finally, the layout area of the inverted source inverter does not exceed the limits of a standard cell area, so this radiation hardening method is also cost efficient. Thus, it can be concluded that this method is useful for digital circuits and possibly can also be extended for analog circuits improvement, where leakage currents can be very high.

However, the change in the threshold voltage leads to similar changes in the delay times of the named above cells: approaching 8 to 12 percent. Consequently, oscillating frequency change of both RO is similar, 11 to 13 percent. As the radiation hardened inverter cell has two more transistors, also influenced by radiation, their threshold voltage shift is also contributing to the change of the circuit parameters. So, inverted source technique might be not efficient for the radiation hard ring oscillator design. Nevertheless, comparison of standard cell based and RHBD RO will help to differentiate between threshold voltage shift contribution and dark current contribution to the circuit performance degradation. Moreover, it is of advantage for applications targeting relatively low oscillating frequencies, delay of around 50 ps for the same cell size whereas the standard inverter has delay of approximately 20 ps, which means less inverters for the same oscillating frequency, when using RHBD one.

Outlook

As it has already been mentioned, the presented thesis has been done in the framework of COTOMICS project, dealing with radiation hardness of ICs used for computed tomography. The aim of the project is to create a set of design guidelines for radiation tolerant integrated circuits for medical imaging applications.

This master thesis gives a background for the first step on the way to creating a list of guidelines - technology characterisation. As the next step of the research, the designed circuit will be produced and tested, together with other test structures, including individual transistors. The measurement results will be compared with the models. The models will be consequently improved and adapted, taking into account measurement results. Moreover, in order to implement the simulation model realistic, a Verilog A model, taking into account parasitic current and voltage sources dependence on the operating conditions can be used to replace simple transistor behavioural one, in order to see radiation damage from a single transistor on block level.

Additionally, TID effects in the STI have to be investigated more closely. In the extra small feature technologies, with gate oxide thinner than 5 nm, the major effect of irradiation takes place in the STI, since its thickness exceeds 300 nm. It is assumed that the main part of the dark current is the STI leakage. Moreover, inter-device leakage, which was not included into this work, has to be taken into account. Thus, some additional structures must be implemented on the test chip in order to be able to differentiate between those phenomena.

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