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Multichannel Mixed Signal Test Equipment for Automotive ICs

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Contents

1 Abstract

During a development process of a new product evaluation is essential. This implies appropriate measurement equipment. Therefore an accordingly test equipment is unpreventable to achieve exceptional results. Thus a redesign of the already existing test equipment, the *TestStation*, is reasonable to extend the measurement possibilities. This document describes at first the basic idea of the new I/O interface. Afterwards the design is split up and described in detail. A description of the developed test board, which was used for the practical evaluation in the lab, follows. After that, a detailed description of the digital design, including an FPGA, follows. The whole measurement is controlled via a LabVIEW® program on a windows host. Finally the measurement results are discussed and a recommendation of the best channel is made.

2 Introduction

In general a new I/O structure for the existing *TestStation* has to be implemented. The *TestStation* is a test box which is used for the evaluation of different ICs in the lab. Therefore the *TestStation* has to be very flexible. Over the time complaints regarding the voltage range and the bandwidth of the I/O structure were made. However the biggest concern was to increase the number of analog channels of the *TestStation*. Therefore a redesign was reasonable.

The first step for a redesign of the I/O structure is to ensure the proper functionality for future use cases. For this reason it is necessary to cover the requirements of all *TestStation* users. This would cause a new interface that would be a benefit for every user.

These requirements imply a faster (up to 30 Mhz) and higher (+/- 10V) signal range. With that enhancement the *TestStation* can also provide a clock signal for the measured RF devices. Thus it is not necessary to have an oscillator on the future test pcb. Besides that the developed test board should also have the opportunity to evaluate an 80 MHz LVDS interface for future usage.

The approach is to develop a principle for the new I/O structure at first. This new principle should be simulated to ensure the required functionality. After the simulation a test pcb has to be made to validate the new interface in the lab. This ensures that all requirements are fulfilled under a test environment. For testing the new I/O channel in the lab, it is also necessary to build a digital test environment for the communication with the analog circuit. Therefore a digital design has to be implemented, including an FPGA. To have proper control of the whole design, it is necessary to create a reasonable control interface. This should be done with a LabVIEW® program on a windows host. After the evaluation process a recommendation of the new I/O interface should be made.

3 Analog Channel

3.1 Basic Concept

Figure 1 shows the principal of the new I/O structure. Basically the analog channel consists of four sections: *DAC Stage*, *MUX*, *GAIN Stage* and *DIFF Stage*. This analog circuit is controlled via an FPGA. A detailed description of these sections follows below.

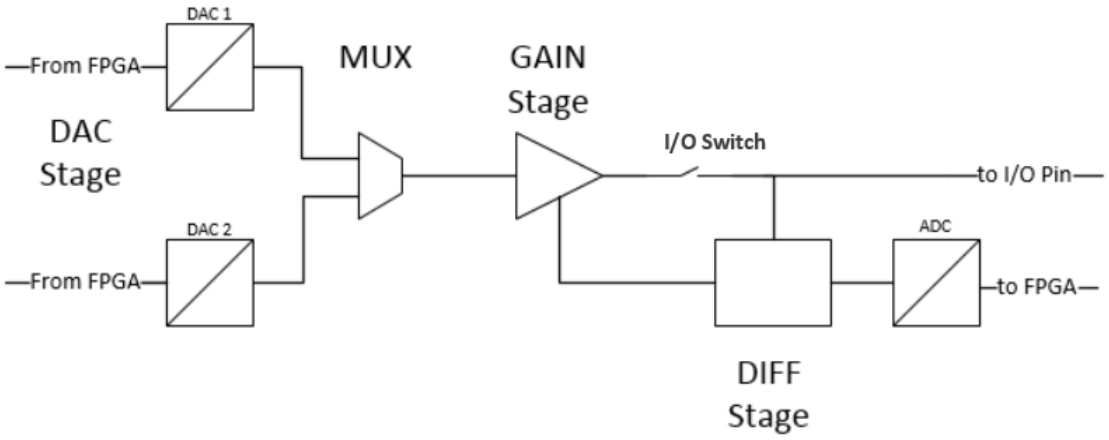


Figure 1: Basic Concept

3.2 DAC Stage

This stage receives the digital data from the FPGA via SPI commands and converts this data into analog voltages. Therefore two digital to analog converters are used. One for generating high speed signals and the other for applying the adjust voltage for the first DAC, as well as for providing a second reference voltage at the multiplexer. This second reference is used for generating arbitrary waveforms, which will be discussed later.

The first converter (AD9106) is a 12 bit high speed converter, with a sampling rate of up to 180 MSPS. Among other features, this converter has a built-in test pattern generator. This results in an more advantageous design. These patterns can be configured via SPI. The AD9106 has got four differential current outputs. This fact makes it necessary to include a current to voltage stage afterwards. The resulting single ended voltage can then be used for the next stage. The CV stage is further described in chapter 3.3.

The second DAC (AD5668) provides the adjust voltage for the previous described DAC, to achieve a better accuracy during the conversion process. Hence it is not necessary to use a very fast converter

for this application. Therefore the sampling rate of 95 kSPS of this converter is sufficient. This converter is also used for the second reference voltage to generate the above mentioned arbitrary waveform. This means that for every channel two voltage levels from this converter are needed. One for the adjust voltage and one for the second reference voltage. Therefore the fact, that the first converter (AD9106) has got four channels and the second (AD5668) has got eight channels is perfect for this application. Further informations about generating the arbitrary waveform can be found in chapter 3.4.

3.3 Current to Voltage Stage

The picture below shows the circuit of the current to voltage stage.

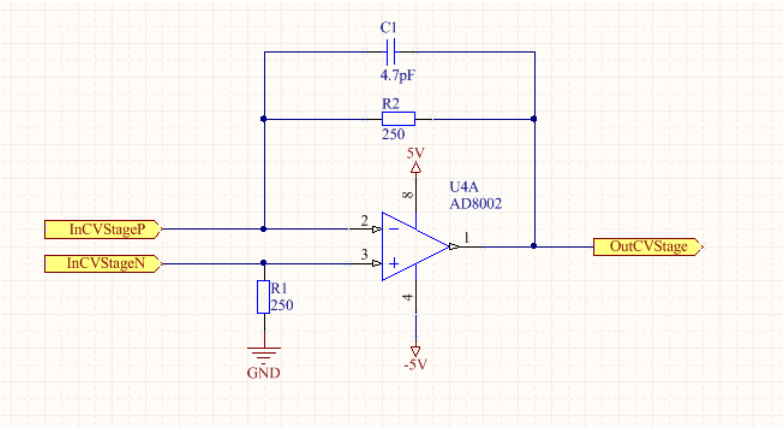


Figure 2: Current to Voltage Stage

It has to be considered, that with this configuration the output signal is inverted. The reason therefore will be discussed later. The resistors R_1 and R_2 are defining the gain and therefore the output voltage range of this stage. A transimpedance amplifier (AD8002) with a bandwidth of 600 MHz is used for this application. The used values for the decouple capacitors for this amplifier are 0.1 μF and 10 μF. Of course the smaller capacitor has to be placed closer to the supply pin of the IC. The output voltage is determined as follows:

$$V_{OUT} = -R \cdot (\pm) \triangle I = -250 \cdot (\pm)4m = \pm 1 \text{ V}. \tag{1}$$

Where $\triangle$I is the output current of the digital to analog converter (AD9106), which is 4 mA. This voltage range is used for the first configuration, which uses the THS4022 in the gain stage. If the other operational amp (THS4012) is used, this voltage range has to be increased. Further information about that can be found in chapter 3.5.

3.3.1 Simulation

All simulations were done with the build-in SPICE simulator in Altium®.

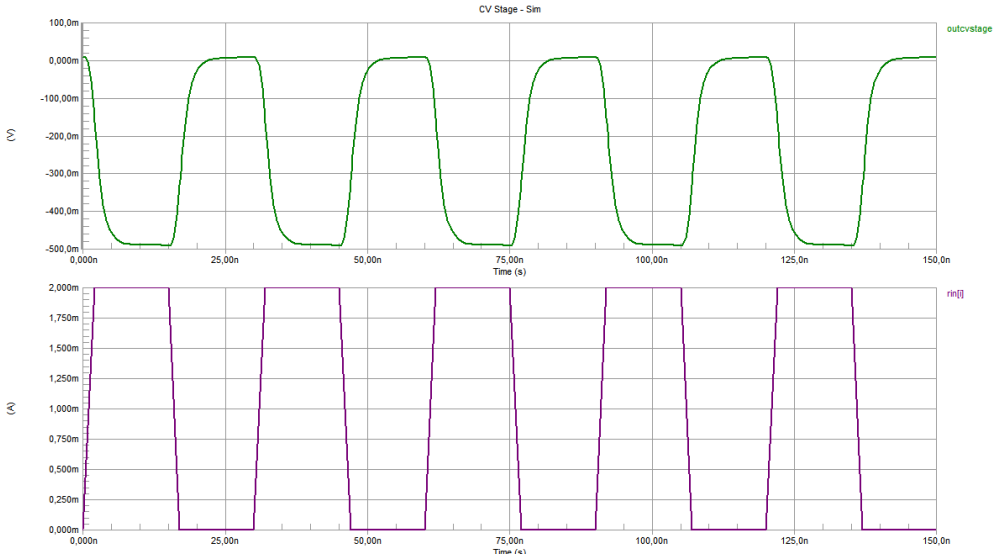


Figure 3: CV Stage - V_{out} compared to I_{in}, f = 30 MHz

Figure 3 shows the operation of the current to voltage stage. The violet curve represents the input current and the green curve the output voltage of the amplifier. With an input current of 2 mA, the output achieves a voltage of -500 mV. This ensures the correct function and a correct gain factor for this setting. Figure 4 shows that at a frequency of 30 MHz the amplifier already has a slight amplitude attenuation and therefore a phase shift of the signal.

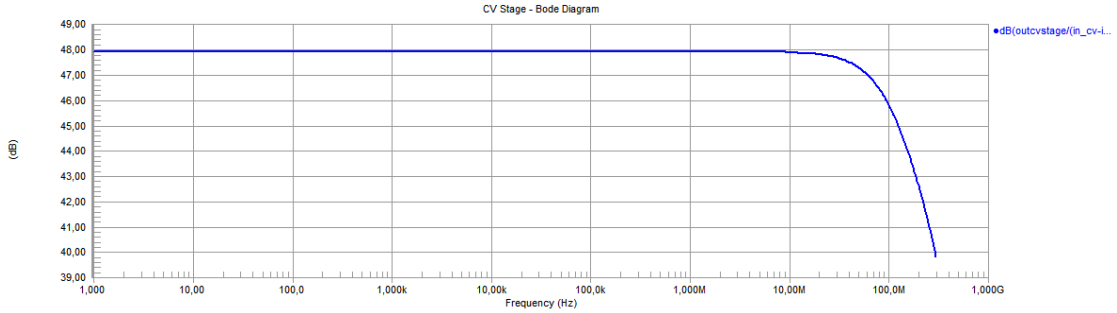


Figure 4: CV Stage - Bode Diagram

3.4 Mulitplexer

Basically the multiplexer (AD8182) is used to switch between the two outputs of the DACs, to generate an arbitrary waveform (figure 5).

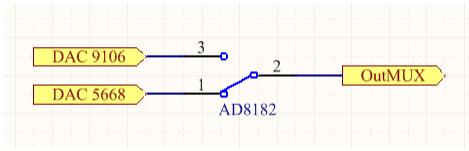


Figure 5: Multiplexer

The resulting waveform will be injected into the device under test, which is a big improvement to the previous design. This fact and the possibility to generate test patterns within the DAC stage makes the new interface very flexible.

The most important criteria for selecting the multiplexer was the switching time. With a very short ON- (10.5 ns) and OFF-time (11 ns), this multiplexer just fulfils the needed requirements for generating a 30 MHz signal. Further information about the used multiplexer can be found in figure 28.

3.5 Gain Stage

The gain stage is necessary to achieve the required signal range of +/- 10 V at the output pin. This stage is realized with an inverting operational amp. Thus the signal is then again in phase, because the CV stage also inverts the signal coming from the high speed digital to analog converter. The selection of the used amplifier for this stage was very important and not easy, because the requirements are very high. These requirements are a high bandwidth, low settling time and a the amp should also provide the previous mentioned signal range of +/- 10 V. There were only two operational amplifiers available, which could closely facilitate the mentioned requirements. These are the *THS4012* and the *THS4022* from Texas Instruments.

These two amps basically distinguish in a different bandwidth (THS4022 has a higher bandwidth) and in the fact, that the THS4022 is only stable at a gain of 10(-9) or greater. The other amplifier (THS4012) is unity gain stable. Both ICs are dual operational amplifiers, this is also important to reduce space on the future I/O board. The used decouple capacitors for both amplifiers have a value of 0.1μF and 10μF. Further information about these amplifiers are listed in table 28.

The next figure shows the gain stage using the THS4022.

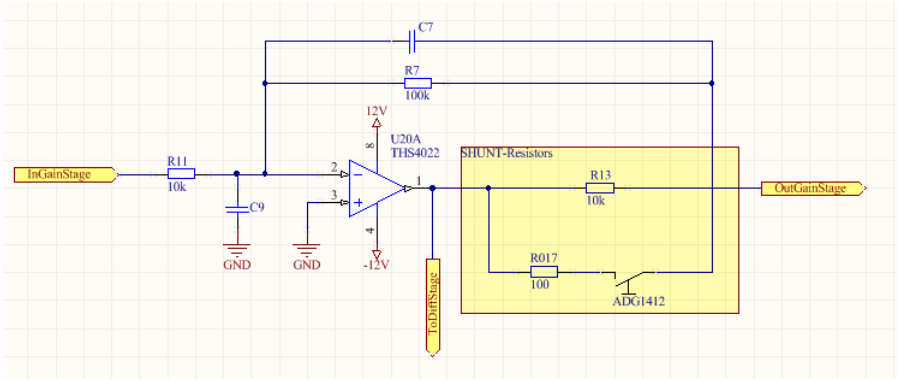


Figure 6: Gain Stage - THS4022

To achieve a gain of -10, the resistor values are calculated as follows:

$$A_V = -\frac{R_7}{R_{11}} = -\frac{100k}{10k} = -10 \tag{2}$$

To be flexible during the evaluation phase, two filter were added. These active and passive low pass filters are used for filtering higher unwanted frequencies.
The final cut off frequency was determined in the lab during the evaluation process. The calculation of the passive filter is shown below.

$$fc = \frac{1}{2 \cdot \pi \cdot R \cdot C} \tag{3}$$

$$C_9 = \frac{1}{2 \cdot \pi \cdot R_{11} \cdot fc} \tag{4}$$

Formula 5 shows the calculation of the included active low pass.

$$C_7 = \frac{1}{2 \cdot \pi \cdot R_7 \cdot fc} \tag{5}$$

The second operational amp (THS4012) has got a lower bandwidth than the THS4022. But this amplifier in contrast is unity gain stable. Because of that it is not necessary to amplify the signal with a factor of at least 10 (or -9) and lower gains can be used. With a lower gain, the cut off frequency of the low pass behaviour can be shifted to a higher frequency. But this modification also means that a higher gain factor of the current to voltage stage is needed to achieve the required

signal range at the output. Without this modification, this amplifier could not be used because of the lower bandwidth. This lower bandwidth would cause a phase shift and an attenuation of the desired signal. The measurement results of the whole stage can be found in chapter 10.4.
The gain stage also includes shunt resistors which are used to measure the voltage and the current at the output pin. The explanation of the shunt resistors can be found in chapter 3.6.

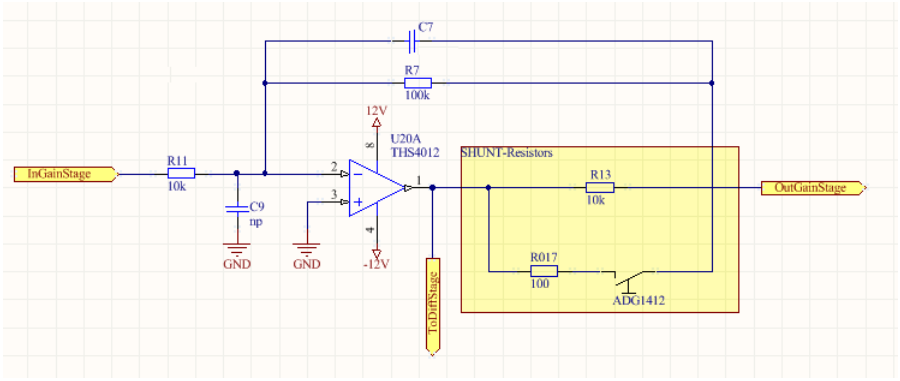


Figure 7: Gain Stage - THS4012

3.5.1 Simulation

- **THS4022**

  The figure below shows the bode diagram of the gain stage, including the THS4022. The simulation was done with the following component values: $R_1 = 1\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$. and $C = 2.2\ \text{pF}$. These values achieved the best results during the simulation. If the feedback resistor is decreased, also the shunt resistor has to be decreased otherwise the amplifier will have a bigger load. The actual used resistor values were evaluated in the lab.

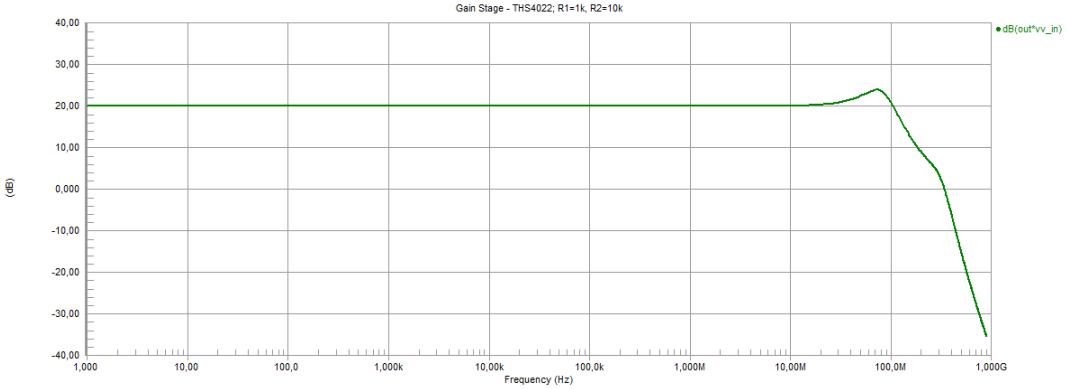


Figure 8: Simulation Result - THS4022 - Bode Diagram

- **THS4012**

  The next figure shows the simulation result of the gain stage, using the THS4012. The used component values are $R_1 = 1\ \text{k}\Omega$, $R_2 = 3.5\ \text{k}\Omega$. No filter capacitors are used in this simulation.

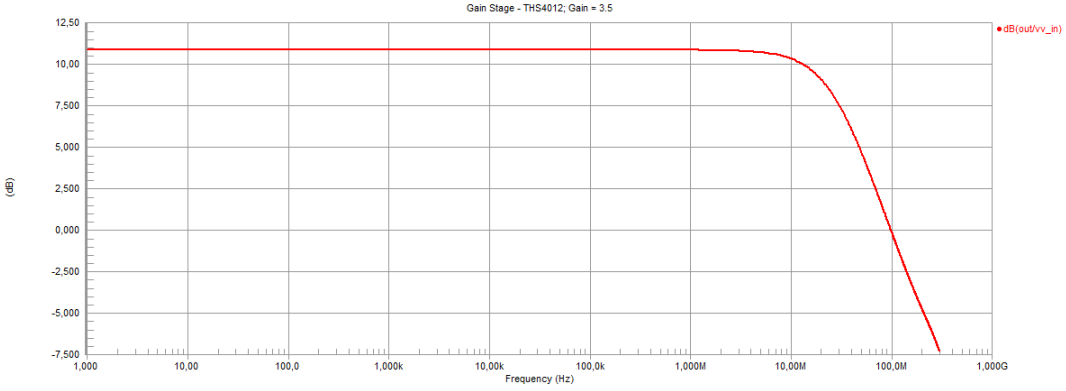


Figure 9: Simulation Result - THS4012 - Bode Diagram

3.6 Changing the Measurement Range

It is also possible to change the measurement range of the I/O channel, to achieve a better accuracy during the whole signal range. To change the measurement range, the shunt resistor within the gain stage can be changed. This is managed with a switch (ADG1412), as shown in figure 10.

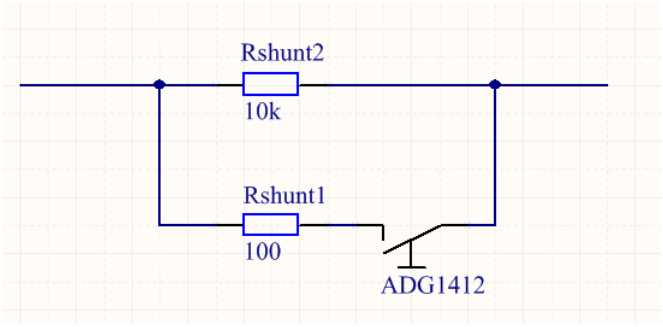


Figure 10: Changing the Shunt Resistor

If the switch is closed, the total resistance of these parallel resistors is 100.5 Ω. It is also important to consider the ON-resistance of the switch in this calculation, which is 1.5 Ω.

$$R_{SHUNT} = \frac{R_{shunt2} \cdot (R_{shunt1} + R_{ON})}{R_{shunt2} + R_{shunt1} + R_{ON}} = \frac{10k \cdot (100 + 1.5)}{10k + 100 + 1.5} = 100.5\Omega \tag{6}$$

For measuring lower signals, the shunt value will be increased to achieve a higher voltage drop at the resistor. This results in a higher signal to noise ratio which ensures a better accuracy. Opening the switch increases the shunt resistance to 10 kΩ. The table below shows the recommended measurement range.

Switch	Shunt [Ω]	Current Range [A]
OPEN	10k	10u - 10m
CLOSE	100,5	10m - 100m

Figure 11: Recommended Measurement Range

3.7 Changing the I/O Mode

Changing the I/O mode of the analog channel is handled via a switch (ADG1412) at the output. If the channel is used as an output, the switch has to be closed to drive the signal out to the connector. In this mode the current consumption of the device under test can be measured. For the use as an input, the switch has to be open to measure the voltage at the pin. Figure 1 illustrates this.

3.8 Differential Stage

To measure the voltage drop at the shunt resistor, an analog to digital converter (AD9257) is used. The AD9257 is a 14 bit converter with a sampling rate of up to 65 MSPS. This IC includes eight channels, whereby space on the board can be reduced. But this converter requires a differential input signal of 2 V_{PP} for the conversion of the analog signal. Therefore the single ended voltage at the shunt resistor has to be converted into a differential signal, before applying it to the input of the ADC. Attention has to be paid on to the fact that the voltage is measured at two points at every channel. Before and after the shunt resistor. Therefore the voltage drop at the shunt resistor can be measured and thus the current through the resistor can be determined. Figure 12 illustrates this. Three different versions of this stage were developed and evaluated.

To minimize the influence of the analog channel to the device under test, a voltage follower is included at the second differential stage (FromInputPin - figure 12). This follower causes a high input impedance coming from the device under test to the differential stage.

Coming from inside the gain stage, this voltage follower is not needed. Therefore the two differential stages for every channel distinguish in the fact that the voltage follower is only included at the point outside the gain stage. This is the same for every variation of the differential stage. The three different variations are described in detail below.

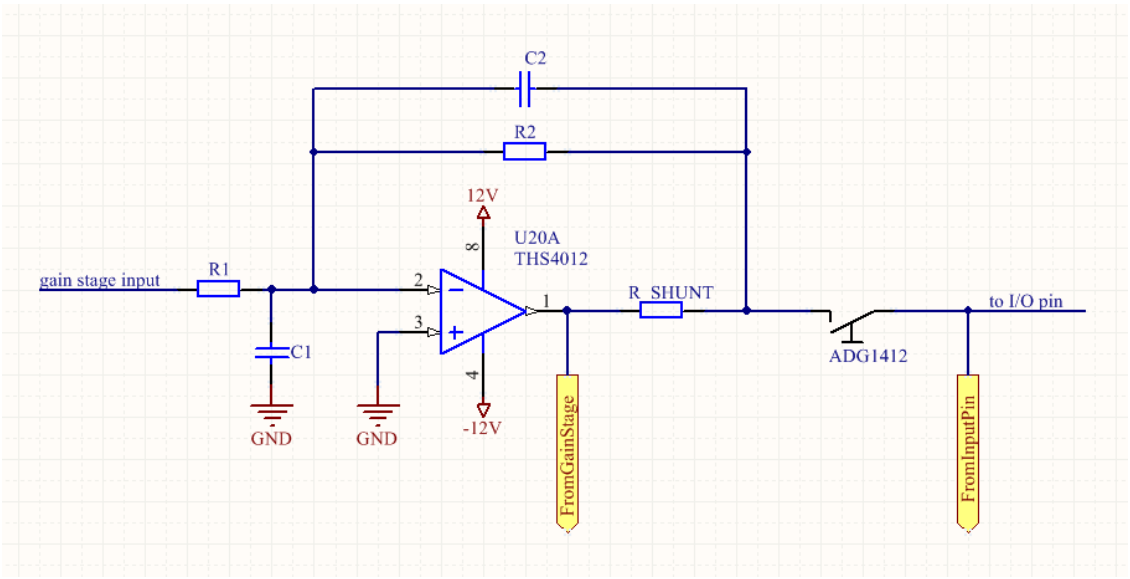


Figure 12: Gain Stage - Measurement Points for Differential Stage

- **Differential stage A**
  The first version generates the differential signal with an operational amplifier (ADA4938-2), as shown in figure 14. The voltage range at the input of the differential stage is +/- 10V. Therefore the signal has to be scaled before applying it to the differential amplifier. Otherwise the differential amplifier could be damaged. This is done with the known amplifier, the THS4022.

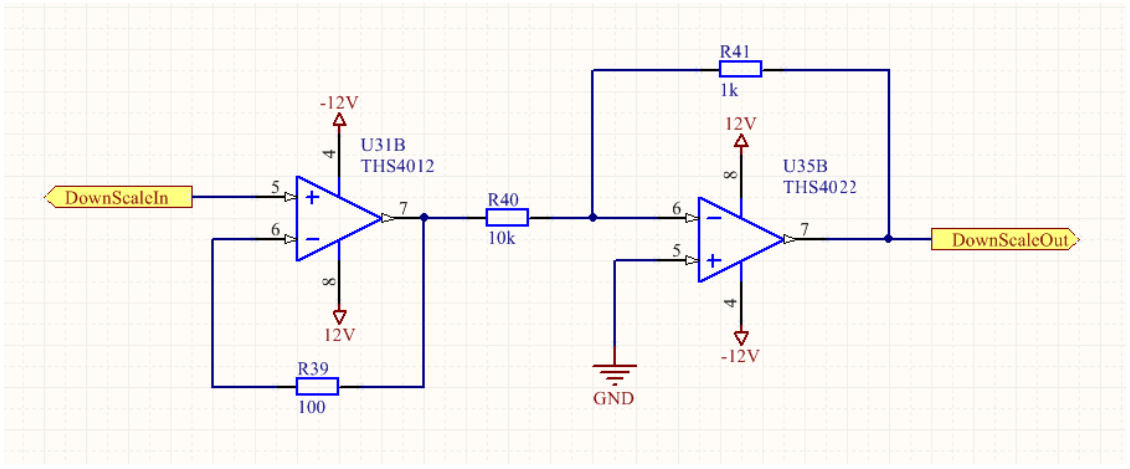


Figure 13: Differential Stage A - Scaling the Signal

The resistor values for a gain of -$\frac{1}{10}$ are determined as follows:

$$A_V = -\frac{R_{41}}{R_{40}} = -\frac{1k}{10k} = -\frac{1}{10} \tag{7}$$

The chosen values are $R_{41} = 1$ kΩ and $R_{40} = 10$ kΩ. To optimize the settling time and minimize ringing, a 100 Ω resistor is used in the feedback loop of the voltage follower. This is recommended, according to the data sheet.

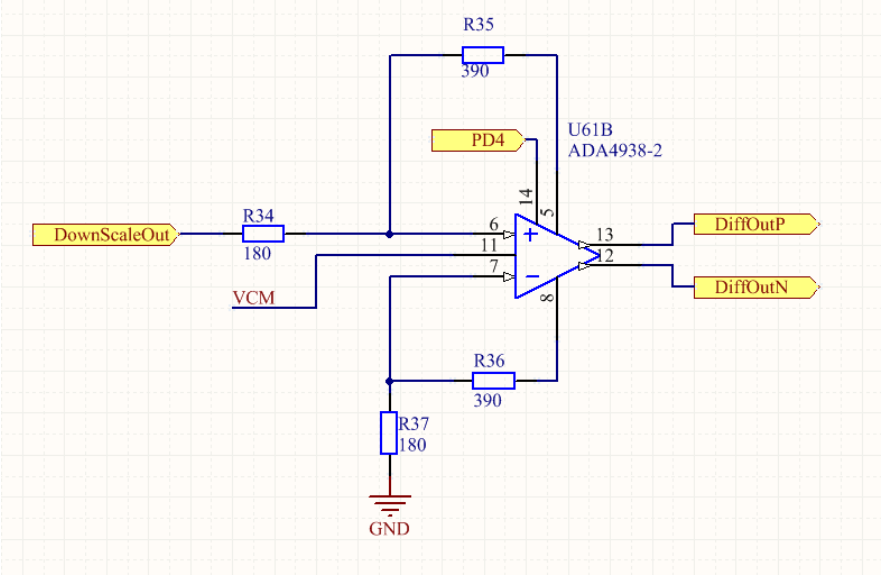


Figure 14: Differential Stage - Version A

The used differential amp has an input voltage range of +/- 1 V. The required differential signal swings around the common mode voltage with an amplitude of 2 V_{PP}. Therefore the signal has to be amplified by two. The chosen resistor values therefore are $R_{34} = R_{37} = 180$ Ω and $R_{35} = R_{36} = 390$ Ω.

- **Differential stage B**
  The second version builds the differential signal with two operational amplifiers one after another. Again a voltage follower is included to achieve a higher input impedance. Figure 15 shows this stage. These two amplifiers generate the differential signal sequentially. The first amplifier inverts and scales the signal. The output of this amp is the negative differential component of the differential signal. The second amplifier only inverts the signal to get the positive component. As mentioned before, the voltage follower is only included at the outside, coming form the input pin.

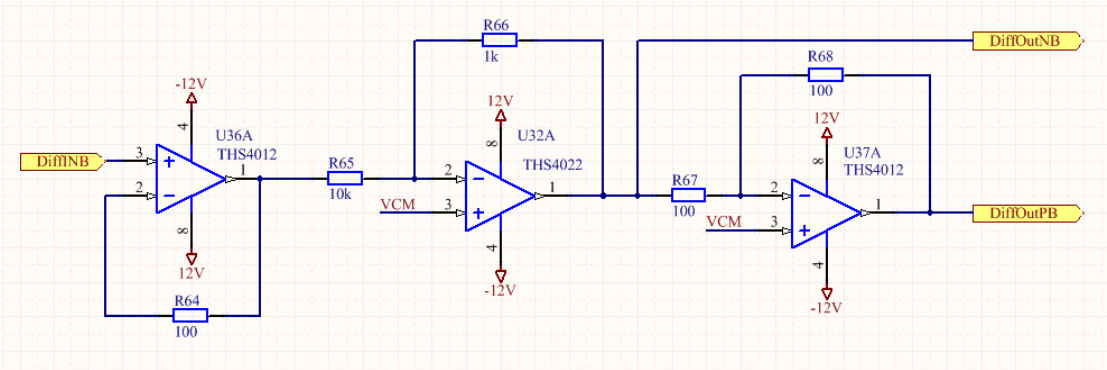


Figure 15: Differential Stage B

- **Differential stage C**
  The last variation needs a detailed description. This version also builds the differential signal with a differential amplifier. But the configuration therefore is different, compared to version A. Figure 16 illustrates this principle.

  This configuration performs as follows: If the output switch is closed (SW3), the channel works as an output. It is possible to measure the voltage drop at the shunt and determine the current consumption of the device under test. Therefore the switches in figure 16 have to be set as follows: SW1 = CLOSE and SW2 = OPEN. This ensures that the voltage drop of the shunt resistor can be measured and with that also the current.
  If the channel works as an input (SW3 = open), the switches have to be set as follows: SW1 = OPEN and SW2 = CLOSE. In this case the inverting input of the differential amplifier is connected to ground. Therefore the voltage applied at the pin can be measured. As mentioned above, it is needed to open one and close another switch. The used switch (ADG1413) has got two switches with positive and two switches with a negative logic. Therefore it is possible to change the circuit configuration with only one control signal to the third mode.

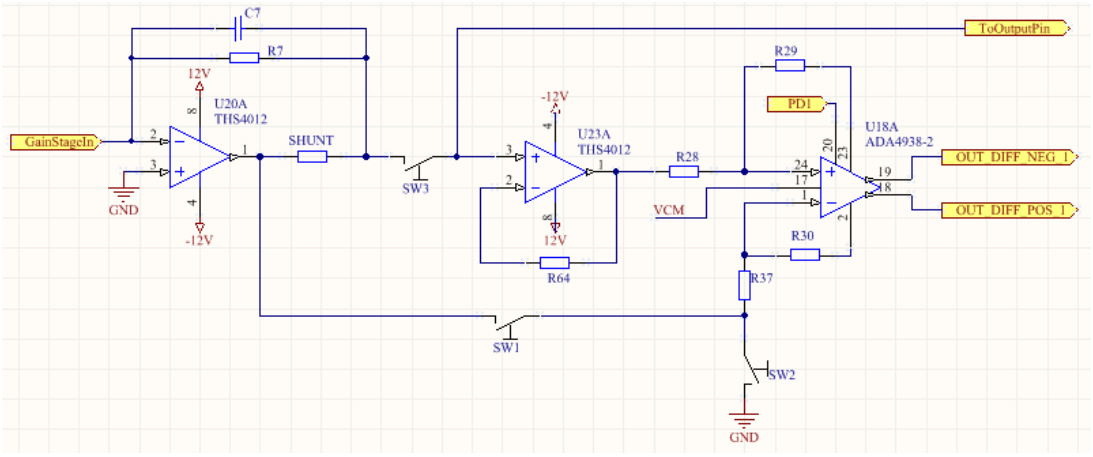


Figure 16: Differential Stage C

Figure 17 shows the circuit for scaling the signal for this variation. With this circuit the amplifier can be used as a follower or as an inverter. The idea behind this is as follows: If this configuration is used as an inverter, the signal range is scaled from +/- 10 V to +/- 1 V and of course the signal is then inverted. When using the operational amp as a follower, the full signal range is applied to the differential amp. To achieve a signal range of +/- 2 V at the differential output, the signal has to be scaled by a factor of 1/5 at the differential amplifier. The resistor values are calculated as follows:

$$A_V = \frac{1}{5} = \frac{R_{29}}{R_{28}} = \frac{R_{30}}{R_{37}} \tag{8}$$

The chosen values are $R_{28} = R_{29} = 200\ \Omega$ and $R_{30} = R_{37} = 1\ \text{k}\Omega$.

This configuration could cause a damage of the differential amp. But the resistors R_{28} and R_{37} in combination with the feedback resistor are dividing the input signal. Therefore this configuration is used to evaluate if the differential amp would be damaged during this mode. The table below shows which resistors have to be placed for the two different functions.

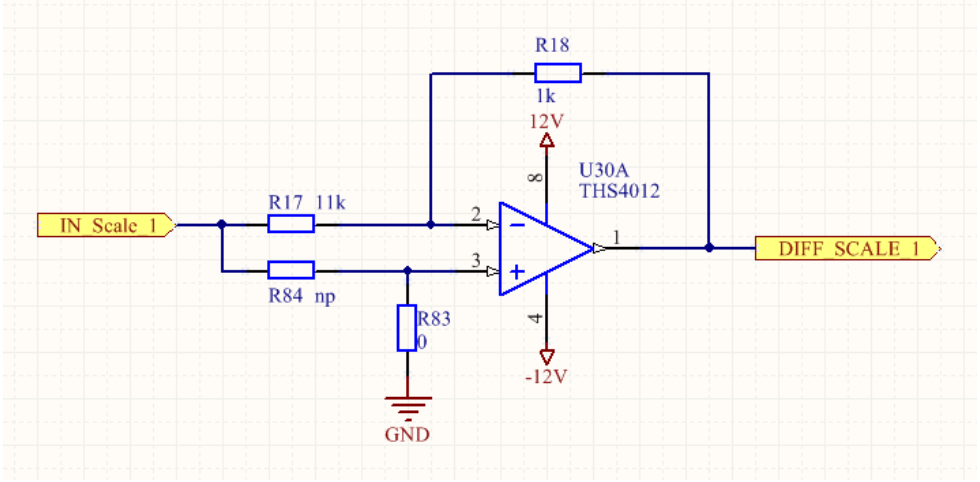


Figure 17: DiffStageC - Downscale

MODE	R17 [Ω]	R18 [Ω]	R83 [Ω]	R84 [Ω]
Follower	n.p.	100	n.p.	0
Inverter (donwscale)	11k	1k	0	n.p.

Figure 18: Follower - Inverter, Resistor Values

The measurement results of these three modes have been evaluated in the lab. The results can be seen in chapter 10.4.7.

Unfortunately there was no simulation model for the used differential amplifier available. Therefore no simulation results are included here.

3.9 ADC Stage

The used ADC (AD9257) is a eight channel switched capacitor ADC. The converter has a resolution of 14 bit, with a sampling rate of up to 65 MSPS. This sampling rate can be configured via SPI. The converter is used to measure the voltage drop of the shunt resistor. Thereby it is possible to calculate the current through the resistor.

- **ADC Filter**

  The circuit in figure 19 shows the design of the passive ADC filter. With that design it is possible to build a low pass filter from first to fourth order. Therefore different variations of the filter can be evaluated and tested in the lab. The ultimately used filter and the selected component values are described in chapter 10.4.

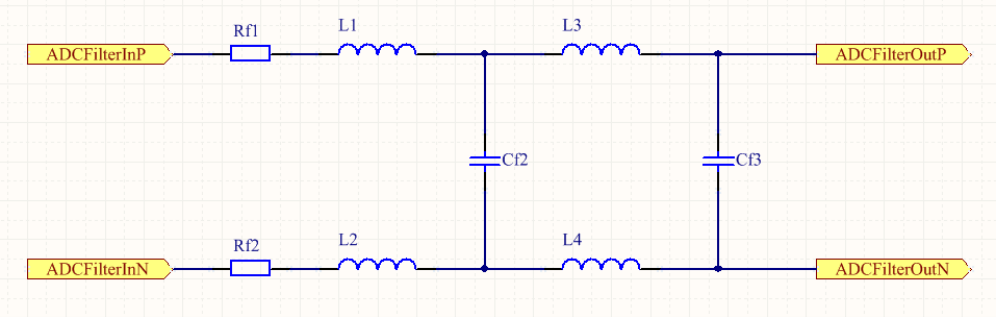


Figure 19: ADC Filter

- Common Mode Voltage

  The AD9257 has got a common mode voltage output. This voltage is used as a reference voltage within the differential stage. The common mode voltage needs to be buffered before applying it to the amps at the differential stage. This is done with the THS4012 configured as a voltage follower in figure 20. The recommended setting for using this amp as a follower is to include a 100 Ω resistor in the feedback path. This optimizes the settling time and minimizes ringing.

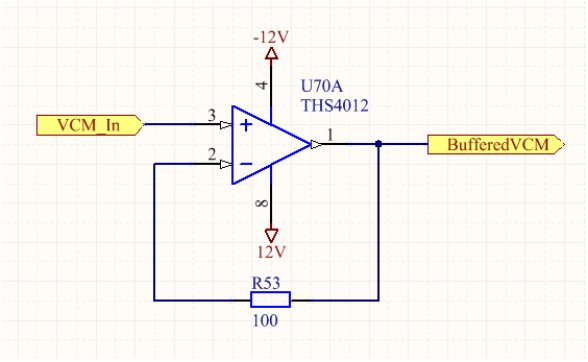


Figure 20: Common Mode Voltage Buffer

3.10 Voltage Supply

The *TestStation I/O Evalboard* has got three supply connectors. These connectors imply voltage levels of 6 V as well as +/- 12V. All other voltages are derived from these voltage levels.

Most of these levels (1.2V, 1.8V, 2.5V, 3.3V, 5V) are generated via regulators, except the negative voltage (-5V) is generated with an DC-DC converter.

With this converter (ADP1111) the output voltage can be inverted, greater (boost/step-up mode), or less (buck/step-down mode) than the input voltage. The circuit for creating the required -5V from the applied 6V is shown in figure 21.

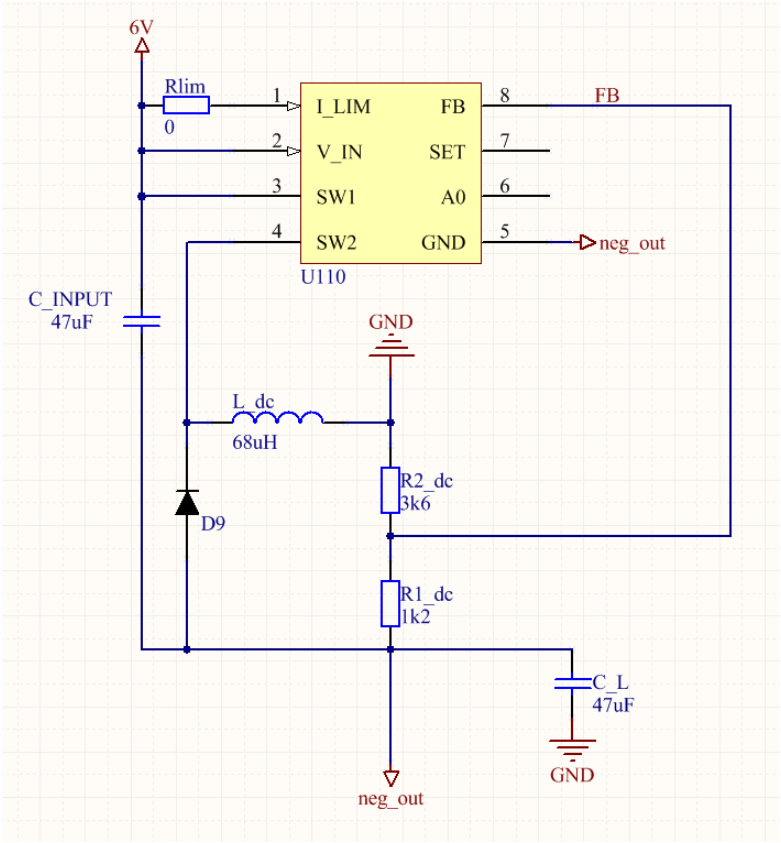


Figure 21: DC-DC Converter Circuit

The ADP1111 uses an internal power switch and an internal reference voltage of 1.25 V for the conversion process. If the voltage at the FB pin falls below the internal reference, the 72 kHz oscillator turns on. Now the ADP1111 drives a current into the inductor and this forces a negative output potential. If the voltage at the FB pin is above the reference voltage, the oscillator turns off. The output voltage is determined by the following formula:

$$|V_{OUT}| = 1.25 \cdot \left(1 + \frac{R_2}{R_1}\right) \tag{9}$$

With $R_2 = 3\text{k}6\ \Omega$ and $R_1 = 1\text{k}2\ \Omega$ the output voltage is due to:

$$|V_{OUT}| = 1.25 \cdot \left(1 + \frac{3k6}{1k2}\right) = |5V| \tag{10}$$

R_{lim} can be placed for reducing the maximum current into the internal power switch. With the design in figure 21 this is not necessary, because the peak current does not exceed 650 mA.

Formula 11 calculates the required inductor power. The IC is supplied with 6V from the connector and the maximum required current is 90 mA. This current is determined through the maximum current consumption of the used components. V_D is the voltage drop of the selected diode.

$$P_L = (|V_{OUT}| + V_D) \cdot I_{OUT}) = (5 + 0.5) \cdot 0.09 = 495mW \tag{11}$$

For every switching cycle the inductor must provide the following energie:

$$\frac{P_L}{f_{OSC}} = \frac{495mW}{72kHz} = 6.87\mu J \tag{12}$$

The current through the inductor is calculated as follows:

$$I_L(t) = \frac{V_L}{R'} \cdot \left(1 - e^{\frac{-R' \cdot t}{L}}\right) \tag{13}$$

The internal switch of the converter can be modeled as a base emitter diode with a voltage drop of 0.75 V and a series resistor of 0.65 Ω. If follows:
R' = 0.65 Ω + $R_{L(DC)}$
V_L = V_{IN} - 0.75 V

$$I_{PEAK} = \frac{5.25}{0.85} \cdot \left(1 - e^{\frac{-0.85 \cdot 7\mu s}{68\mu H}}\right) = 517.5mA \tag{14}$$

$$E_L = \frac{1}{2} \cdot (68\mu H) \cdot (517.5mA)^2 = 18.2\mu J \tag{15}$$

The energy of the inductor (18.2 μJ) is higher than the required energy of 6.87 μJ. A inductor value of 68 μH is therefore sufficient for this application. The selected capacitor is a tantalum electrolytic capacitor with a value of 47 μF. It is important that the capacitor has got a low ESR to ensure low output ripples of the signal.
For D_9 a shottky diode (1N5818) is recommended. However there is no SMD package available for this type. So the similar MBRS130T3G with an SMD package was used to reduce board space.

To provide the other voltage levels regulators were used. These regulators have a fixed output voltage. So for every voltage level another regulator is used. Figure 22 shows the circuit for

creating these different voltage levels, in which only the LD1117S12TR needs the resistor at the output (R_{100}) to generate 1.2 V. The other regulators do not need this resistor.

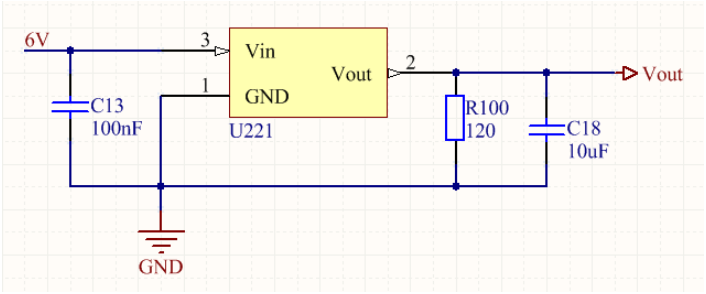


Figure 22: Circuit for Providing the Different Supply Voltages

Used IC	Voltage Level
LD1117S12TR	1.2 V
LD1117AS18TR	1.8 V
LD1117S25CTR	2.5 V
LD1117AS33TR	3.3 V
LD1117S50CTR	5 V

Figure 23: List of Used Regulators

Figure 23 shows a list of the used regulators. These regulators have a typical dropout voltage of 1.15 V. The exclusion is the LD1117S50CTR with a dropout voltage of 1 V. Therefore it is possible to create 5 V out from the 6 V connector with that IC. The used regulators provide an output current of 0.8 - 1 A. For stability reasons a 10 μF capacitor is added at the output of every regulator.

4 LVDS Interface

Besides other requirements of the analog channel, the developed test pcb should also provide the possibility to evaluate a 80 MHz LVDS interface for future usage. In general LVDS (**L**ow **V**oltage **D**ifferential **S**ignal) is used for signal transmission at higher frequencies. Here the data transfer is realized with the difference between two signal levels. The driver generates a constant current which is applied to the positive or negative path, dependent on the logic level. The other signal is then tied to ground. The two data lines should be placed close together to achieve excellent noise immunity.
In this design the LVDS signal is buffered during the transmission from the connector to the FPGA. This is done with the *DS90LV804* from Texas Instruments®. This is a 4 channel LVDS buffer with a data rate of up to 800 MBPS. The input of this IC is terminated with an impedance of 100 Ω. Therefore the trace to and from the buffer was also matched with a impedance of 100 Ω at 80 MHz. The next figure shows the required geometric proportion for achieving this matching.

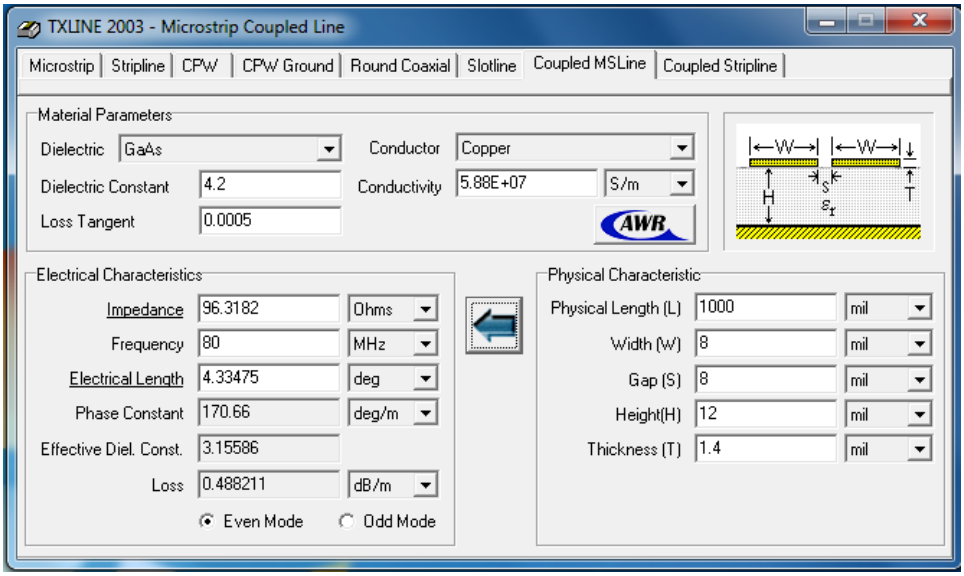


Figure 24: Matched Impedance for 80 MHz - LVDS Interface

It was necessary to create a trace with a width of 8, a height of 12 and a thickness of 1.4 mil. The gap between the two signal lines is 8 mil.

5 FPGA

5.1 General Description

The used FPGA is a *Spartan 3 - XC3S400*, with a PQ208 package. This FPGA provides 141 I/O pins within 8 banks.

5.2 Defining the I/O Standard

Each of these 8 banks can be configured independently, regarding the I/O standard. It is necessary to provide three different I/O standards for this design. These are the single ended standards *LVCMOS33* and *LVCMOS25*, as well as the differential standard *LVDS25*. The definition of these signals is done within the constraints file (chapter 8.1.1).

5.3 Clock Management

The **D**igital **C**lock **M**anagers (DCMs) are providing the clock resources for the internal logic of the FPGA. The used FPGA has got 4 DCMs which are located at the corners of the FPGA. These DCMs consist of four blocks:

- **Delay-Locked Loop (DLL)**
  The DLL compensates the delay of the clock which occurs due to the routing path. The inputs of the DLL unit are *CLKIN* and *CLKFB*. The output signals are *CLK0*, *CLK90*, *CLK180*, *CLK270*, *CLK2X*, *CLK2X180*, and *CLKDV*.
- **Digital Frequency Synthesizer (DFS)**
  The DFS is used to multiply or divide the input clock signal. This is done with user defined input signals *CLKFX MULTIPLY* and *CLKFX DIVIDE*. The output signals *CLKFX* and *CLKFX180* are then derived from the input signal *CLKIN*.
- **Phase Shift (PS)**
  This unit controls the phase shift between the clock outputs (*PSDONE*, *STATUS[0]*) and the clock inputs (*PSINCDEC*, *PSEN*, *PSCLK*) of the DCM.
- **Status Logic**
  This Logic is and indicator of the current state of the DCM. This is done via the *LOCKED* and *STATUS* signals.

Figure 25 shows the block diagram of a Spartan 3 DCM.

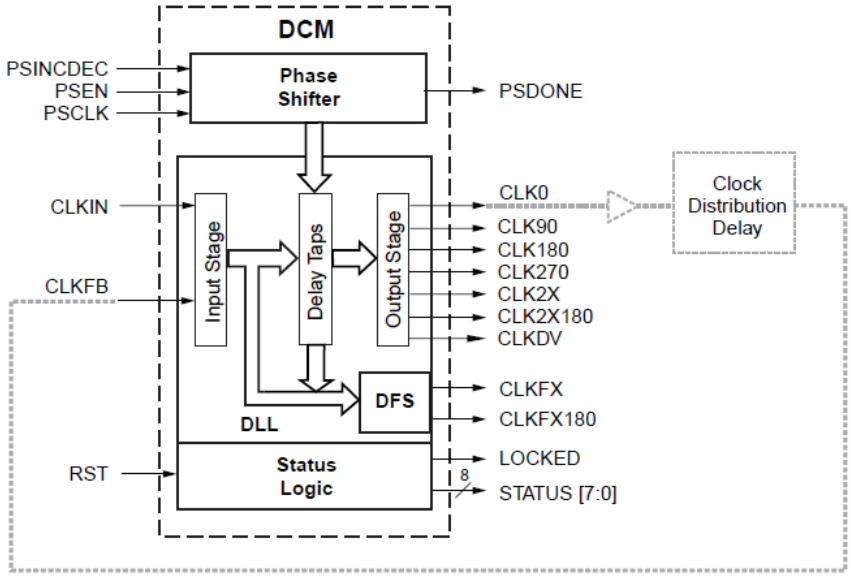


Figure 25: DCM Functional Block Diagram, [4]

5.4 Power Management

In this design three supply voltages are used. These different levels are needed for internal logic as well as for defining the standard of the I/O signals.

In my design 2.5 V is used to provide the LVCMOS25 standard as well as the LVDS25 standard for differential signals. 3.3 V is used to provide the LVCMOS33 standard. 1.2 V is used for internal Logic (VCCINT). Attention has to be given to the supply of bank 4 and 5. It is needed to supply these banks with 2.5 Volt during power on. The reason therefore is that the configuration pins are located there and the whole configuration logic of the FPGA uses 2.5 Volt.

5.5 Decoupling the supply

Each of these Supply Voltages has to be decoupled separately to achieve a balanced decoupling network. To reach a flat impedance, it is necessary to roughly divide the quantity of capacitors by two, for every decade of increase in size (value of capacitor). To make it more clear, here is an example:

The FPGA has got four pins for the VCCINT supply (1.2 V). This means that four small capacitors are needed because every supply pin should have a block capacitor next to it. For this small capacitor it is recommended to use a value of about 0.01 - 0.047 μF. At the next step the number of capacitors has to be divided by two. This means $4/2 = 2$.

Two is now the number of capacitors for the next decade of size (0.1 - 0.47 μF). To finish this example one more capacitor with a size of 1.0 - 4.7 μF is needed. This procedure was repeated for

every supply. Therefore this ratio is hold to for every FPGA supply network.

Figure 26 shows the layout of the decouple network.

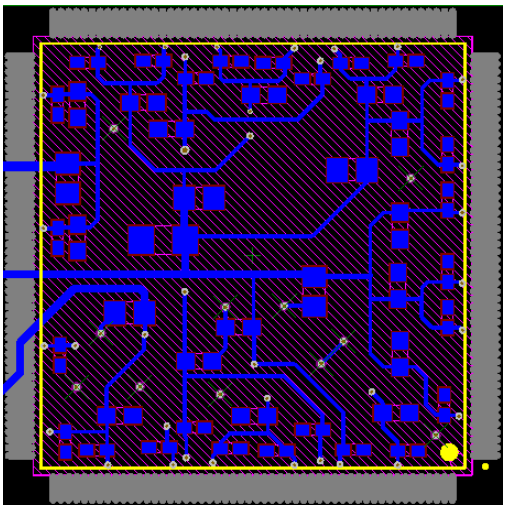


Figure 26: FPGA Decouple Network - Layout

5.6 Programming the FPGA

The FPGA was programmed via JTAG (IEEE-Standard 1149.1). This interface is carried out as a 6-pin header on the board. Figure 27 shows the pin configuration for the interface.

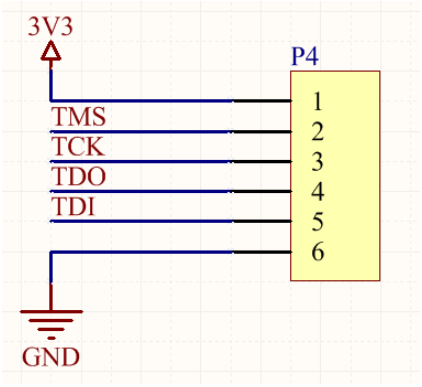


Figure 27: JTAG Interface

6 Overview of the Selected ICs

The figure below shows a list of the selected parts of the analog channel. This list includes all operational amps, switches, multiplexer, data converter and the used FPGA.

Type	Part	Channels				Characteristics
			Resolution	Conversion Rate		
DAC	AD9106	4	12 bit	180 MSPS		high-speed
DAC	AD5668	8	16 bit	95 kSPS		high resolution
ADC	AD9257	8	14 bit	65 MSPS		high-speed
			Bandwith	Slew rate	Settling time	
MUX	AD8182	2	750 MHz	750 V/µs	14 ns	2:1 MUX
OPAMP	AD8002	2	600 MHz	1200 V/µs	16 ns	CFB-AMP
OPAMP	THS4012	2	290 MHz	310 V/µs	37 ns	VV-AMP
OPAMP	THS4022	2	350 MHz	470 V/µs	40 ns	VV-AMP
OPAMP	ADA4938-2	2	1000 MHz	4700 V/µs	6.5 ns	Differential-AMP
OPAMP	AD8024	4	350 MHz	2400 V/µs	18 ns	CFB-AMP
			ON-Resistance	Time (ON)	Time (OFF)	
SWITCH	ADG1412	4	1.5 Ω	100 ns	90 ns	pos logic
SWITCH	ADG1413	4	1.5 Ω	100 ns	90 ns	pos & neg logic
			# I/O	#Logic Cells	# Gates	
FPGA	XC3S400		141	8064	400000	Spartan 3

Figure 28: Selected Parts

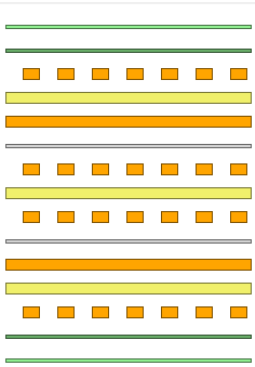
Further information can be found in the corresponding data sheets. One of the selection criteria was the package size. Most of these ICs are available in a QFN (**Q**uad **F**lat **N**o Leads) package. This package has the following advantages:

- Reduced board space
- Reduced electrical parasitics
- Reduced package height and package mass

7 Board Design (Altium Designer®)

The board design as well as the simulation of the analog circuit was done with *Altium Designer®*. For this reason it was necessary to create all required components within the designer. Hence a schematic as well as the associated footprint was created. The footprint was built with the Altium® tool *IPC Compliant Footprint Wizard*. The simulation was done with the integrated SPICE® simulator. Therefore also the simulation files were added to the created components. The simulation results can be found in chapter 3.

Another important tool of Altium® is the *Layer Stack Manager*. Information about the layer structure and the used materials can be found there. This is important for impedance matched traces, because knowledge of the used board materials is needed therefore. Figure 29 shows the layer structure of the *TestStation I/O Evalboard*.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Top Layer	Signal	Copper	1.4				Top
Dielectric 1	Dielectric	Core	12		4.2		
Internal Plane 1	Internal Plane	Copper	1.4			20	
Dielectric 2	Dielectric	Prepreg	5	FR-4	4.2		
Signal Layer 1	Signal	Copper	1.4				Not Allowed
Dielectric 5	Dielectric	Core	10		4.2		
Signal Layer 2	Signal	Copper	1.4				Not Allowed
Dielectric 4	Dielectric	Prepreg	5	FR-4	4.2		
Internal Plane 2	Internal Plane	Copper	1.417			20	
Dielectric 6	Dielectric	Core	12		4.2		
Bottom Layer	Signal	Copper	1.4				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 29: Layer Structure

This figure shows that the board design includes six layers. Whereas layer two and five are used as shielding layers which are connected to ground. The other layers are signal layers. In which the routing on top layer contains most of the high speed paths as well as the LVDS signals. Signal layer 1 (third layer) contains the digital control signals. Signal layer 2 (fourth layer) also includes high speed signals as well as SPI clock signals. The bottom layer includes the supply routing paths for the whole power management. The layer structure itself is symmetric. Further information about the layout can be found in the appendix.

8 Digital Design (Verilog)

The whole digital design was implemented in Verilog. This **H**ardware **D**escription **L**anguage (HDL) is used for a description of digital electrical systems. In general a HDL allows digital designs at different abstraction levels from switch level to gate level over register transfer level, up to behavioural level. Within a design the different modules are connected via ports with each other. The used design tool was *ISE Design Suite 14.2* from Xilinx®.

8.1 Verilog Design

Figure 30 shows the block diagram of the digital design. The memory interface directly interacts with the FPGA board, which handles the communication to the windows interface. In general this interface handles data from the FPGA board and stores this data in registers on the FPGA of the *TestStation Evalboard*. This is done within the *MemInterf* module. Hence signals for synchronisation of the data transfer are required. Therefore a clock signal is provided by the FPGA board as well as a chip select signal to notify the start of a data transmission. For a read operation, a read enable (RE) and a write enable (WE) signal for a write operation is used. All these signals are negative logic.
The data width of this interface is 16 bit and the address has a width of 8 bits.
This data is stored in registers which define the behaviour of the design. These registers are connected via wires to the related modules, which are:

- *dacAD5668:* Module for communication between the FPGA and AD5668
- *dacAD9106:* Module for communication between the FPGA and AD9106
- *adcAD9257:* Module for communication between the FPGA and AD9257
- *dacAD9257DataAc:* Module for data acquisition from the AD9257
- *switchADC1412:* Module for changing the switch state
- *muxAD8182:* Module for selecting the multiplexer state and the switching frequency
- *timer:* Module for providing a timer for the multiplexer switching

The data in the related registers determine the behaviour of these modules. In this design every IC has its own module. The modules for the data converters are very much the same. A strobe signal is signalizing that a new value was stored in a register. This strobe signal is the trigger for the next event. Inside these modules a case selector determines which register value has changed and starts the data transmission to the IC. This transmission is done via SPI. Therefore the transmission frame is built and via the SPI block the data is transmitted to the IC. This SPI block is not the same for every module because the SPI command differs from IC to IC. But in general the principle of a data transmission is similar for all of these modules.

The data stored inside the multiplexer registers define the switching states and the switching frequency of the multiplexer. The data in the switch registers defines the state of all the analog

switches on the evaluation board. A detailed description of all registers in this design can be found at figure 45, 46 and 47.

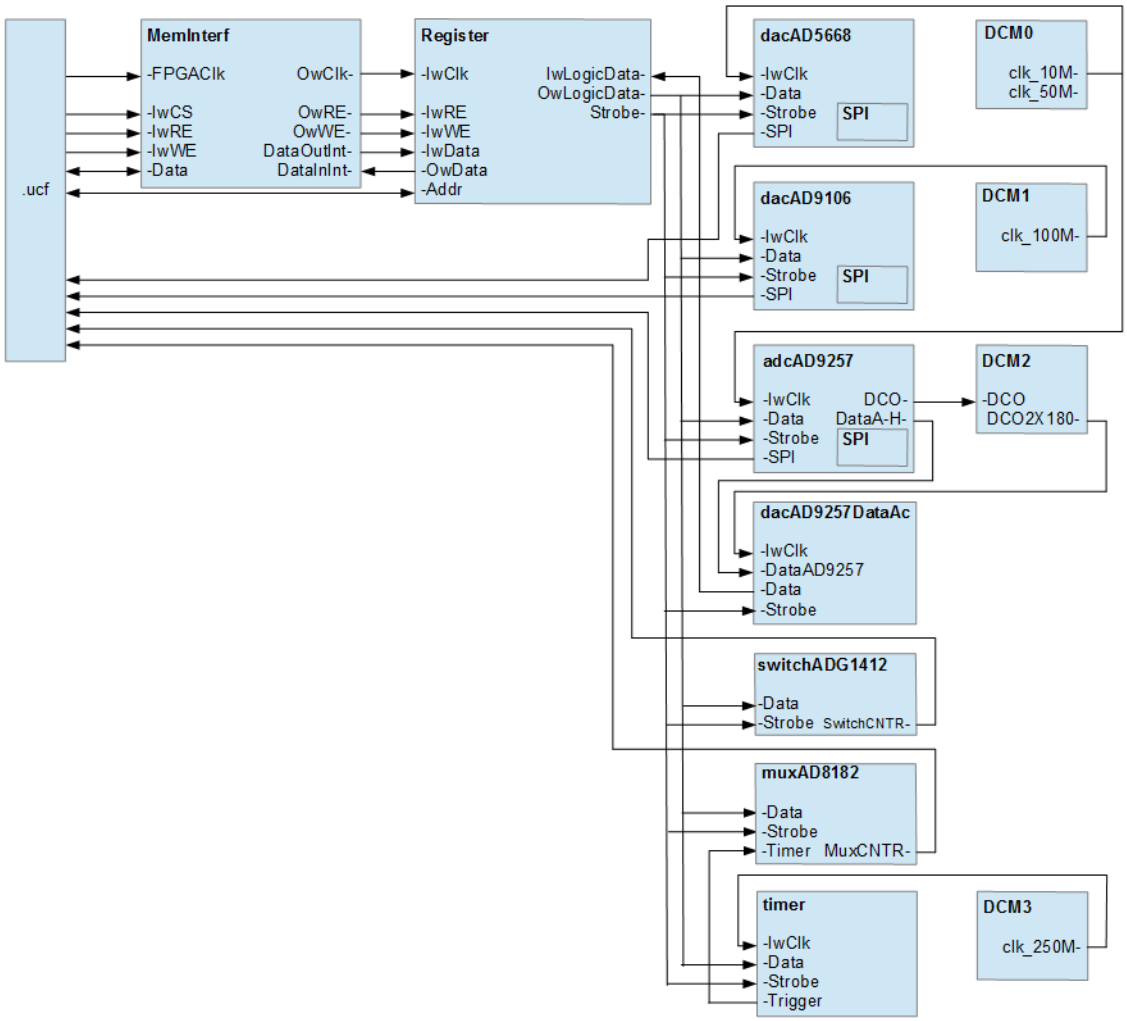


Figure 30: Digital Design - Block Diagram

8.1.1 Constraint File

This chapter shows the code of the constraints file (.ucf) and therefore all pin connections of the FPGA. The constraints file creates the connection between the physical I/O pins of the FPGA and the internal signals of the digital design. Thus it appears that also the I/O standard as well as other parameters are defined within this file.

```
NET "XD[0]" LOC = P205;
NET "XD[0]" IOSTANDARD = LVCMOS33;
NET "XD[0]" SLEW = FAST;
NET "XD[1]" LOC = P204;
NET "XD[1]" IOSTANDARD = LVCMOS33;
NET "XD[1]" SLEW = FAST;
NET "XD[2]" LOC = P203;
NET "XD[2]" IOSTANDARD = LVCMOS33;
NET "XD[2]" SLEW = FAST;
NET "XD[3]" LOC = P200;
NET "XD[3]" IOSTANDARD = LVCMOS33;
NET "XD[3]" SLEW = FAST;
NET "XD[4]" LOC = P199;
NET "XD[4]" IOSTANDARD = LVCMOS33;
NET "XD[4]" SLEW = FAST;
NET "XD[5]" LOC = P198;
NET "XD[5]" IOSTANDARD = LVCMOS33;
NET "XD[5]" SLEW = FAST;
NET "XD[6]" LOC = P197;
NET "XD[6]" IOSTANDARD = LVCMOS33;
NET "XD[6]" SLEW = FAST;
NET "XD[7]" LOC = P196;
NET "XD[7]" IOSTANDARD = LVCMOS33;
NET "XD[7]" SLEW = FAST;
NET "XD[8]" LOC = P194;
NET "XD[8]" IOSTANDARD = LVCMOS33;
NET "XD[8]" SLEW = FAST;
NET "XD[9]" LOC = P191;
NET "XD[9]" IOSTANDARD = LVCMOS33;
NET "XD[9]" SLEW = FAST;
NET "XD[10]" LOC = P190;
NET "XD[10]" IOSTANDARD = LVCMOS33;
NET "XD[10]" SLEW = FAST;
NET "XD[11]" LOC = P189;
NET "XD[11]" IOSTANDARD = LVCMOS33;
NET "XD[11]" SLEW = FAST;
NET "XD[12]" LOC = P187;
NET "XD[12]" IOSTANDARD = LVCMOS33;
NET "XD[12]" SLEW = FAST;
NET "XD[13]" LOC = P182;
NET "XD[13]" IOSTANDARD = LVCMOS33;
NET "XD[13]" SLEW = FAST;
NET "XD[14]" LOC = P178;
NET "XD[14]" IOSTANDARD = LVCMOS33;
NET "XD[14]" SLEW = FAST;
```

```
46 NET "XD[15]" LOC = P176;
47 NET "XD[15]" IOSTANDARD = LVCMOS33;
48 NET "XD[15]" SLEW = FAST;
49
50
51 //------LEDS------------------
52 NET "LED[0]" LOC = P139;
53 NET "LED[0]" IOSTANDARD = LVTTL;
54 NET "LED[0]" SLEW = SLOW;
55 NET "LED[1]" LOC = P138;
56 NET "LED[1]" IOSTANDARD = LVTTL;
57 NET "LED[1]" SLEW = SLOW;
58 NET "LED[2]" LOC = P137;
59 NET "LED[2]" IOSTANDARD = LVTTL;
60 NET "LED[2]" SLEW = SLOW;
61 NET "LED[3]" LOC = P135;
62 NET "LED[3]" IOSTANDARD = LVTTL;
63 NET "LED[3]" SLEW = SLOW;
64 NET "LED[4]" LOC = P144;
65 NET "LED[4]" IOSTANDARD = LVTTL;
66 NET "LED[4]" SLEW = SLOW;
67 NET "LED[5]" LOC = P143;
68 NET "LED[5]" IOSTANDARD = LVTTL;
69 NET "LED[5]" SLEW = SLOW;
70 NET "LED[6]" LOC = P141;
71 NET "LED[6]" IOSTANDARD = LVTTL;
72 NET "LED[6]" SLEW = SLOW;
73 NET "LED[7]" LOC = P140;
74 NET "LED[7]" IOSTANDARD = LVTTL;
75 NET "LED[7]" SLEW = SLOW;
76
77
78 //--------CLOCK SIGNALS---------
79 //----external oscillator-------
80 NET "clk_osc" LOC = P180;
81 NET "clk_osc" IOSTANDARD = LVCMOS33;
82 NET "clk_osc" PERIOD = 20 ns;
83
84 //----AD9106-------
85 NET "CLK9106_p" LOC = P79;
86 NET "CLK9106_p" IOSTANDARD = LVDS_25;
87 NET "CLK9106_n" LOC = P80;
88 NET "CLK9106_n" IOSTANDARD = LVDS_25;
89 //100MHz
90 NET "CLK9106_p" PERIOD = 10 ns;
91 NET "CLK9106_n" PERIOD = 10 ns;
```

```
92
93  //----AD9257-------
94  NET "CLK9257_p" LOC = P76;
95  NET "CLK9257_p" IOSTANDARD = LVDS_25;
96  NET "CLK9257_n" LOC = P77;
97  NET "CLK9257_n" IOSTANDARD = LVDS_25;
98
99
100 //-----ADDR-BUS-----------------
101 NET "ADDR[0]" LOC = P175;
102 NET "ADDR[0]" IOSTANDARD = LVTTL;
103 NET "ADDR[0]" SLEW = FAST;
104 NET "ADDR[1]" LOC = P172;
105 NET "ADDR[1]" IOSTANDARD = LVTTL;
106 NET "ADDR[1]" SLEW = FAST;
107 NET "ADDR[2]" LOC = P171;
108 NET "ADDR[2]" IOSTANDARD = LVTTL;
109 NET "ADDR[2]" SLEW = FAST;
110 NET "ADDR[3]" LOC = P169;
111 NET "ADDR[3]" IOSTANDARD = LVTTL;
112 NET "ADDR[3]" SLEW = FAST;
113 NET "ADDR[4]" LOC = P168;
114 NET "ADDR[4]" IOSTANDARD = LVTTL;
115 NET "ADDR[4]" SLEW = FAST;
116 NET "ADDR[5]" LOC = P167;
117 NET "ADDR[5]" IOSTANDARD = LVTTL;
118 NET "ADDR[5]" SLEW = FAST;
119 NET "ADDR[6]" LOC = P166;
120 NET "ADDR[6]" IOSTANDARD = LVTTL;
121 NET "ADDR[6]" SLEW = FAST;
122 NET "ADDR[7]" LOC = P165;
123 NET "ADDR[7]" IOSTANDARD = LVTTL;
124 NET "ADDR[7]" SLEW = FAST;
125
126
127 //--------BACKUP PINS------------
128 NET "backup1" LOC = P150;
129 NET "backup1" IOSTANDARD = LVTTL;
130 NET "backup2" LOC = P149;
131 NET "backup2" IOSTANDARD = LVTTL;
132 NET "backup4" LOC = P147;
133 NET "backup4" IOSTANDARD = LVTTL;
134 NET "backup5" LOC = P146;
135 NET "backup5" IOSTANDARD = LVTTL;
136 //------------------------------
137
```

```
138
139 //---------SPI-SIGNALS----------
140 //-----DAC5668----
141 NET "mo_5668" LOC = P100;
142 NET "mo_5668" SLEW = FAST;
143 NET "mo_5668" IOSTANDARD = LVCMOS25;
144 NET "ldac_5668" LOC = P102;
145 NET "ldac_5668" SLEW = FAST;
146 NET "ldac_5668" IOSTANDARD = LVCMOS25;
147 NET "clr_5668" LOC = P101;
148 NET "clr_5668" SLEW = FAST;
149 NET "spi_clk_5668" LOC = P181;
150 NET "spi_clk_5668" IOSTANDARD = LVCMOS33;
151 NET "spi_clk_5668" SLEW = FAST;
152 NET "sync_5668" LOC = P97;
153 NET "sync_5668" IOSTANDARD = LVCMOS25;
154 NET "sync_5668" SLEW = FAST;
155
156 //------AD9106-----
157 NET "TRIGGER9106" LOC = P111;
158 NET "TRIGGER9106" IOSTANDARD = LVCMOS33;
159 NET "TRIGGER9106" SLEW = FAST;
160 NET "RESET9106" LOC = P106;
161 NET "RESET9106" IOSTANDARD = LVCMOS33;
162 NET "RESET9106" SLEW = FAST;
163 NET "CS9106" LOC = P107;
164 NET "CS9106" IOSTANDARD = LVCMOS33;
165 NET "CS9106" SLEW = FAST;
166 NET "SDIO9106" LOC = P109;
167 NET "SDIO9106" IOSTANDARD = LVCMOS33;
168 NET "SDIO9106" SLEW = FAST;
169 NET "SDO9106" LOC = P108;
170 NET "SDO9106" IOSTANDARD = LVCMOS33;
171 NET "SDO9106" SLEW = FAST;
172 NET "SCLK9106" LOC = P183;
173 NET "SCLK9106" IOSTANDARD = LVCMOS33;
174 NET "SCLK9106" SLEW = FAST;
175
176 //------AD9257-----
177 NET "SCLK9257" LOC = P184;
178 NET "SCLK9257" IOSTANDARD = LVCMOS33 | DRIVE = 8;
179 NET "SCLK9257" SLEW = FAST;
180 NET "SDIO9257" LOC = P58;
181 NET "SDIO9257" IOSTANDARD = LVCMOS25;
182 NET "SDIO9257" SLEW = FAST;
183 NET "CS9257" LOC = P57;
```

```
184 NET "CS9257" IOSTANDARD = LVCMOS25;
185 NET "CS9257" SLEW = FAST;
186 NET "SYNC9257" LOC = P61;
187 NET "SYNC9257" IOSTANDARD = LVCMOS25;
188 NET "SYNC9257" SLEW = FAST;
189 //---------------------------------
190
191
192 //-------HANDSHAKE SIGNALS FOR-------
193 //---------MEMORY INERFACE-----------
194 NET "FPGA_CLK" LOC = P154;
195 NET "FPGA_CLK" IOSTANDARD = LVTTL;
196 NET "FPGA_CLK" SLEW = FAST;
197 NET "FPGA_CLK" CLOCK_DEDICATED_ROUTE = TRUE;
198 NET "FPGA_OE" LOC = P155;
199 NET "FPGA_OE" IOSTANDARD = LVTTL;
200 NET "FPGA_OE" SLEW = FAST;
201 NET "FPGA_WE" LOC = P152;
202 NET "FPGA_WE" IOSTANDARD = LVTTL;
203 NET "FPGA_WE" SLEW = FAST;
204 NET "FPGA_CS" LOC = P156;
205 NET "FPGA_CS" IOSTANDARD = LVTTL;
206 NET "FPGA_CS" SLEW = FAST;
207
208
209 //-----CONTROL SIGNALS---------------
210 //-----MUX1--------
211 NET "MUX1A" LOC = P94;
212 NET "MUX1A" IOSTANDARD = LVCMOS25;
213 NET "MUX1A" SLEW = FAST;
214 NET "MUX1B" LOC = P93;
215 NET "MUX1B" IOSTANDARD = LVCMOS25;
216 NET "MUX1B" SLEW = FAST;
217
218 //-----MUX2---------
219 NET "MUX2A" LOC = P90;
220 NET "MUX2A" IOSTANDARD = LVCMOS25;
221 NET "MUX2A" SLEW = FAST;
222 NET "MUX2B" LOC = P92;
223 NET "MUX2B" IOSTANDARD = LVCMOS25;
224 NET "MUX2B" SLEW = FAST;
225
226 //----OUTSWITCH------
227 NET "OUTSWITCH1" LOC = P64;
228 NET "OUTSWITCH1" IOSTANDARD = LVCMOS25;
229 NET "OUTSWITCH1" SLEW = FAST;
```

```
230 NET "OUTSWITCH2" LOC = P63;
231 NET "OUTSWITCH2" IOSTANDARD = LVCMOS25;
232 NET "OUTSWITCH2" SLEW = FAST;
233 NET "OUTSWITCH3" LOC = P65;
234 NET "OUTSWITCH3" IOSTANDARD = LVCMOS25;
235 NET "OUTSWITCH3" SLEW = FAST;
236 NET "OUTSWITCH4" LOC = P67;
237 NET "OUTSWITCH4" IOSTANDARD = LVCMOS25;
238 NET "OUTSWITCH4" SLEW = FAST;
239
240
241 //-----AD9257 DATA CHANNEL A-H-----
242 NET "AD9257CHA_p" LOC = P22;
243 NET "AD9257CHA_p" IOSTANDARD = LVDS_25;
244 NET "AD9257CHA_n" LOC = P24;
245 NET "AD9257CHA_n" IOSTANDARD = LVDS_25;
246 NET "AD9257CHB_p" LOC = P26;
247 NET "AD9257CHB_p" IOSTANDARD = LVDS_25;
248 NET "AD9257CHB_n" LOC = P27;
249 NET "AD9257CHB_n" IOSTANDARD = LVDS_25;
250 NET "AD9257CHC_p" LOC = P28;
251 NET "AD9257CHC_p" IOSTANDARD = LVDS_25;
252 NET "AD9257CHC_n" LOC = P29;
253 NET "AD9257CHC_n" IOSTANDARD = LVDS_25;
254 NET "AD9257CHD_p" LOC = P31;
255 NET "AD9257CHD_p" IOSTANDARD = LVDS_25;
256 NET "AD9257CHD_n" LOC = P33;
257 NET "AD9257CHD_n" IOSTANDARD = LVDS_25;
258 NET "AD9257CHE_p" LOC = P39;
259 NET "AD9257CHE_p" IOSTANDARD = LVDS_25;
260 NET "AD9257CHE_n" LOC = P40;
261 NET "AD9257CHE_n" IOSTANDARD = LVDS_25;
262 NET "AD9257CHF_p" LOC = P42;
263 NET "AD9257CHF_p" IOSTANDARD = LVDS_25;
264 NET "AD9257CHF_n" LOC = P43;
265 NET "AD9257CHF_n" IOSTANDARD = LVDS_25;
266 NET "AD9257CHG_p" LOC = P44;
267 NET "AD9257CHG_p" IOSTANDARD = LVDS_25;
268 NET "AD9257CHG_n" LOC = P45;
269 NET "AD9257CHG_n" IOSTANDARD = LVDS_25;
270 NET "AD9257CHH_p" LOC = P46;
271 NET "AD9257CHH_p" IOSTANDARD = LVDS_25;
272 NET "AD9257CHH_n" LOC = P48;
273 NET "AD9257CHH_n" IOSTANDARD = LVDS_25;
274
275 //---AD9257 DCO for data acquisition---
```

```
276 NET "AD9257DCO_p" LOC = P36;
277 NET "AD9257DCO_p" IOSTANDARD = LVDS_25;
278 NET "AD9257DCO_n" LOC = P37;
279 NET "AD9257DCO_n" IOSTANDARD = LVDS_25;
280 NET "AD9257FCO_p" LOC = P34;
281 NET "AD9257FCO_p" IOSTANDARD = LVDS_25;
282 NET "AD9257FCO_n" LOC = P35;
283 NET "AD9257FCO_n" IOSTANDARD = LVDS_25;
```

8.1.2 DCM

The **D**igital **C**lock **M**anager (DCM) is used for generating different clock signals within the design. In this case the different clocks are derived from an external oscillator. This 50 MHz oscillator is the input clock for every used DCM. The FPGA has got four DCMs located at the four corners of the chip. Figure 31 shows the *Xilinx Clocking Wizard* which can be used for generating the instantiation code for such a DCM.

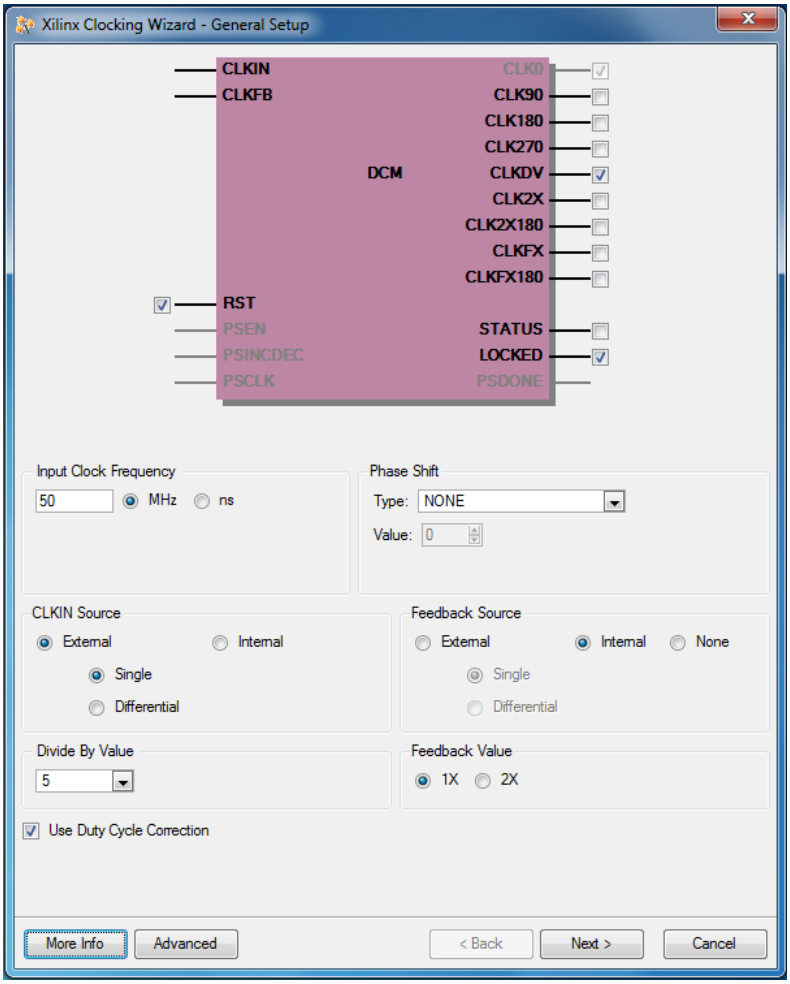


Figure 31: DCM Configuration

In this example a simple single ended 10 MHz clock signal is derived from the external oscillator. The generated instantiation code is shown below.

```
//DCM
DCM10M dcm_10M (
    .CLKIN_IN(clk_osc),
    .RST_IN(1'b0),
    .CLKDV_OUT(clk_10M),
    .CLKIN_IBUFG_OUT(),
    .CLK0_OUT(clk_50M),
    .LOCKED_OUT()
    );
```

8.1.3 SPI

SPI (**S**erial **P**eripheral **I**nterface) was developed by Motorola. This standard describes a synchronous serial bus which can be used for the communication to peripherals after the master slave principle. There are four signals which control the data transfer between the master and the slave. These signals are:

- **SCLK** (Serial Clock)
  Synchronizing signal, provided by the master.
- **MOSI** (**M**aster **O**ut, **S**lave **I**n)
  Output signal of the master.
- **MISO** (**M**aster **I**n, **S**lave **O**ut)
  Output signal of the slave.
- **CS** (**C**hip **S**elect)
  Active low signal, defines which slave is selected.

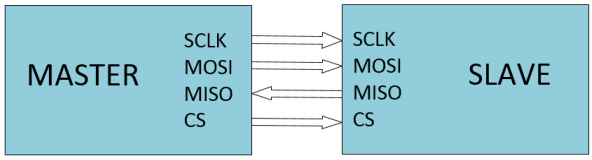


Figure 32: SPI Principle

The figure above shows the SPI principle with one slave. For every further slave, the master needs to provide another select signal to ensure a correct slave selection.

9 User Interface (LabVIEW®, TestStand®)

Figure 36 shows the GUI of the windows host. The whole interface was implemented with LabVIEW®. This LabVIEW® program ensures the data transmission from, or to the FPGA of the *TestStation Evalboard*.

9.0.4 LabVIEW® - Front Panel

Basically the GUI represents a tab control with four pages, which are:

- **INIT**

  The INIT tab includes all initial function for the two DAC's and the used ADC. This functions are necessary for generating a stable state of the ICs, as well as for configuring the SPI blocks.

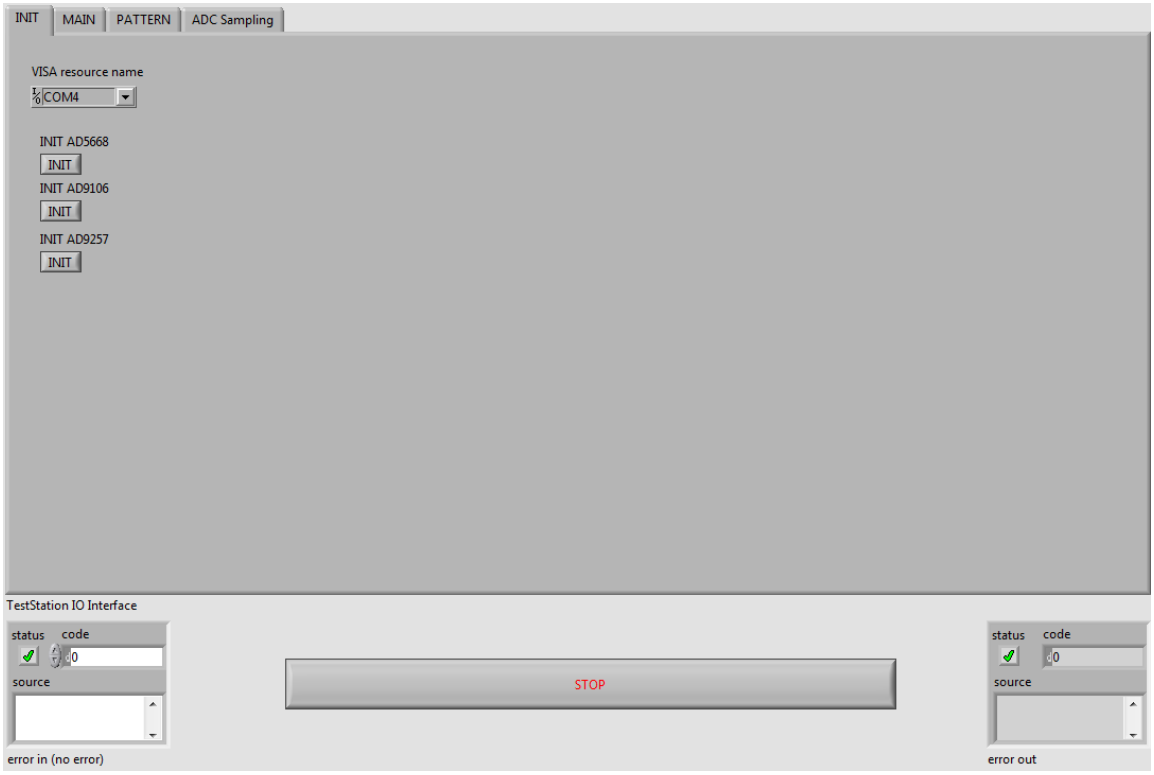


Figure 33: LabView® - INIT Tab

- **MAIN**

  On the left of the GUI (1), the user can select a register for writing data to the FPGA, or backwards. Next to that (2) it is possible to set the voltage level (AD5668) for the second reference voltage via a scroll bar. At section 3 the adjust voltage for the second converter (AD9106) can be set. On the right (4) the output voltage of the high speed converter can be defined. Sections 2, 3 and 4 are only for a better user handling. Basically the whole setup can be controlled via the registers in section 1.

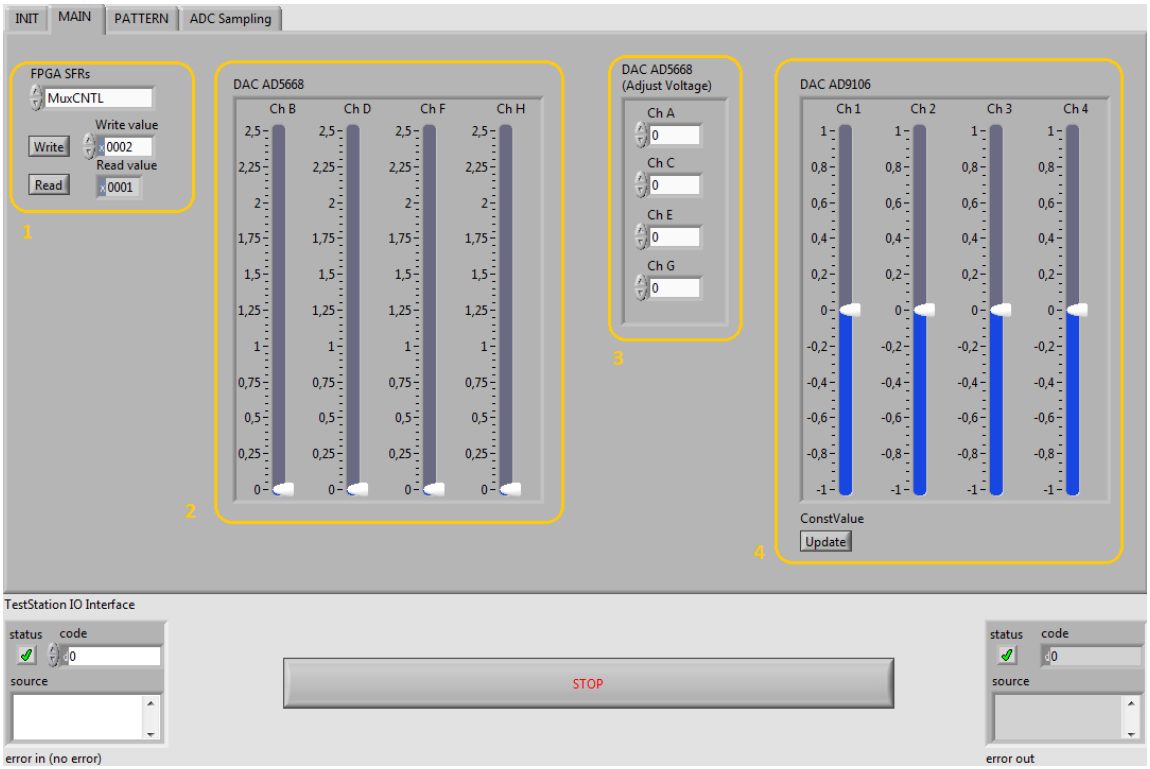


Figure 34: LabView® - MAIN Tab

- **PATTERN**

  In this tab the patterns of the high speed DAC (AD9106) are defined. These are in general a sin wave and different sawtooth types with a user defined frequency.

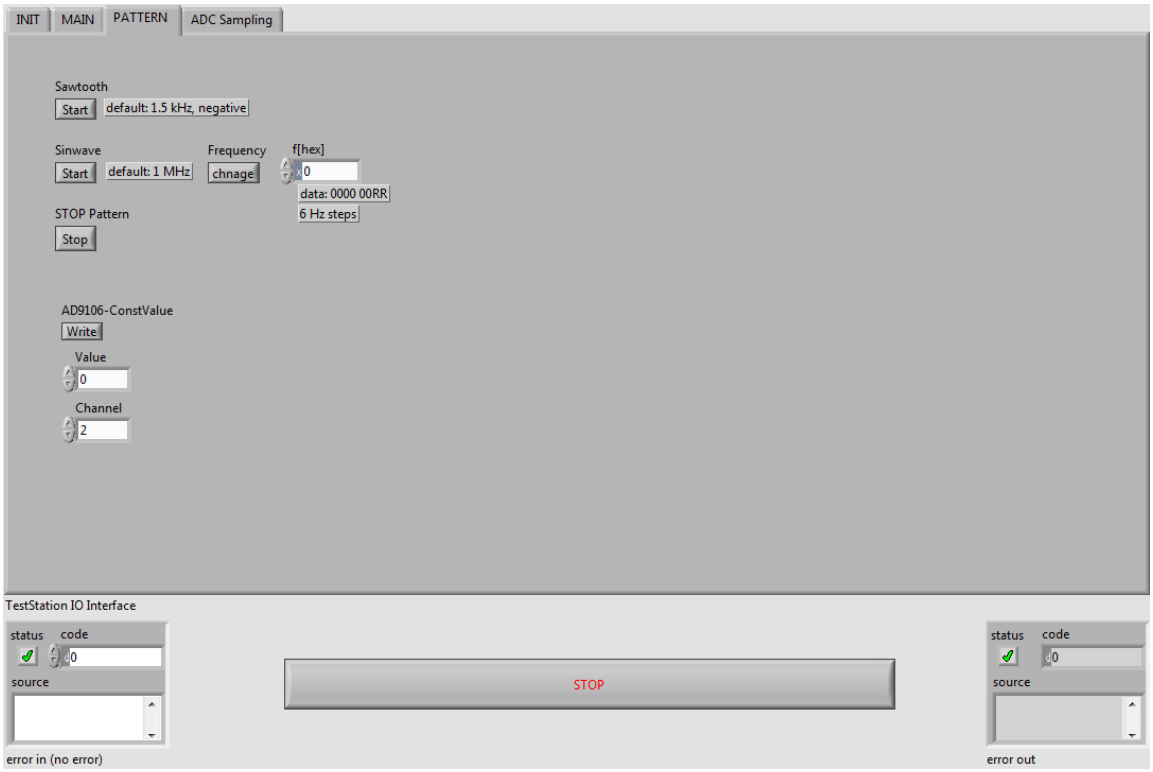


Figure 35: LabView® - PATTERN Tab

- **ADC SAMPLING**

  This tab uses the data stored in the FPGAs block ram to generate a FFT (**F**ast **F**ourier **T**ransformation) with the sampled measurement points.

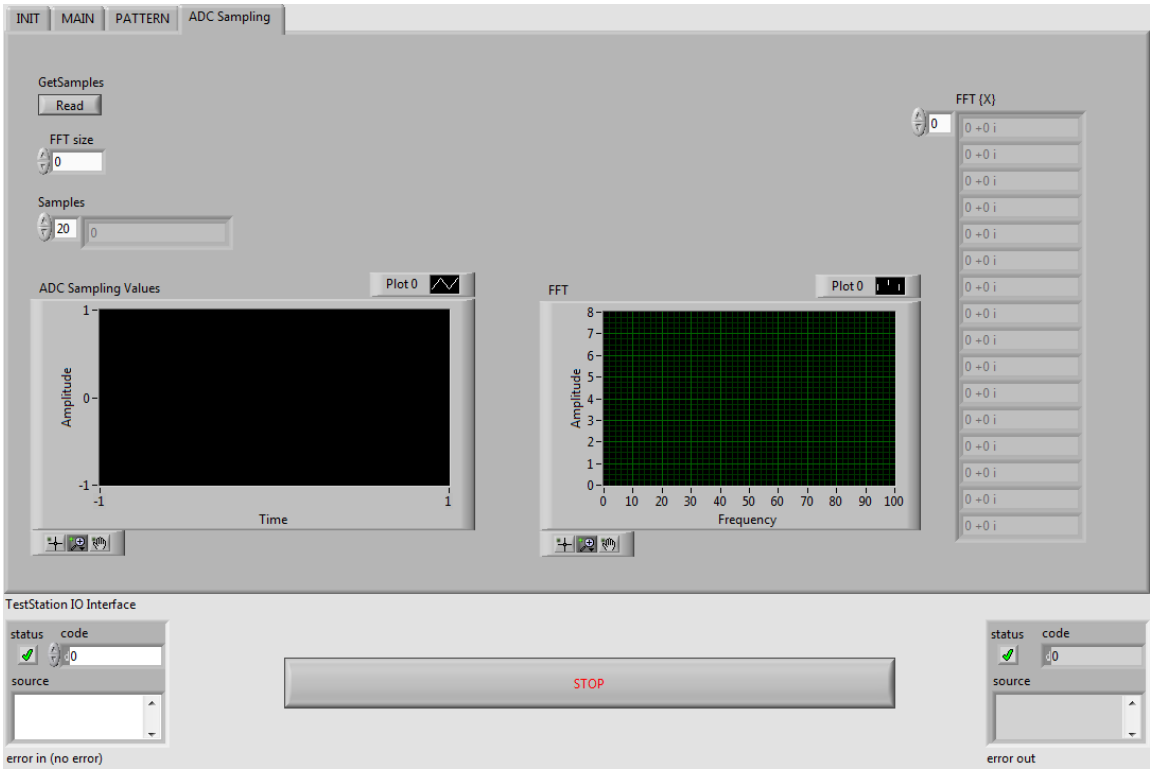


Figure 36: LabView® - ADC SAMPLING Tab

9.0.5 LabVIEW® - Block Diagram

In general the block diagram consists of an event handler within a while loop. This event handler handles events coming from the front panel (*Write* - button, *Read* - button, etc.). Figure 37 shows an example of sending a new adjust voltage level to the FPGA.

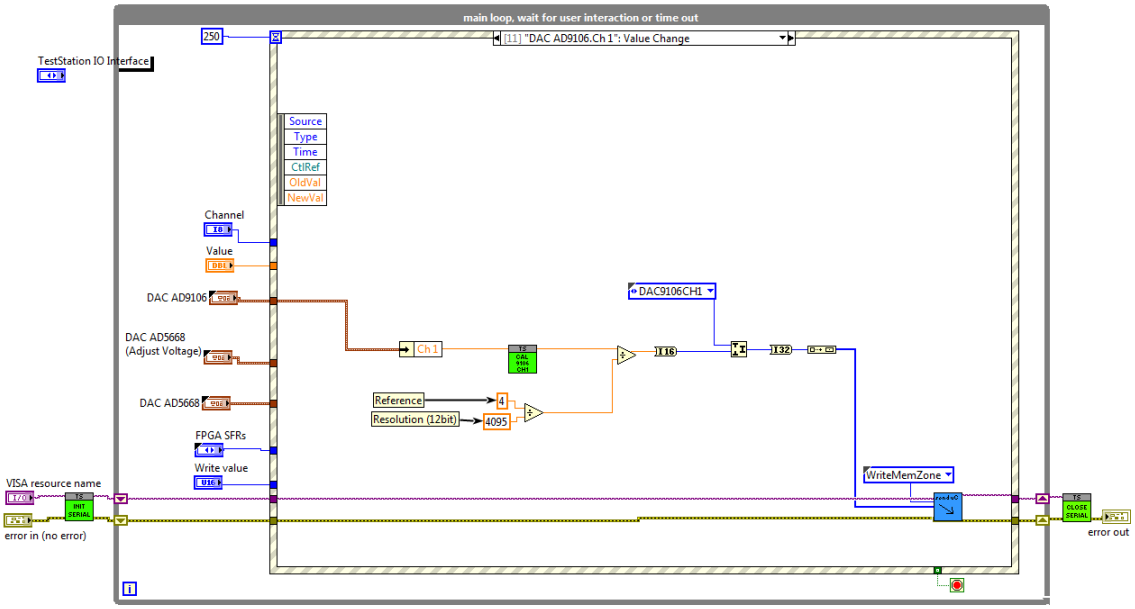


Figure 37: LabView® - Block Diagram

The value written in the *Adjust Voltage* window is scaled depending on the FSR and the resolution of the converter. This value is then merged with the corresponding address. The next block sends the data to the FPGA. This basic concept for sending data from the windows interface to the FPGA and backwards is the same for every data transmission. The whole program runs inside a while loop which can be stopped with the stop button at the front panel.

The included subVI handles the calibration of every channel, which was done for both DAC's (AD9106, AD5668), the multiplexer, as well as for the gain stage and the current to voltage stage. The principle of the calibration is the same for every stage. In general the offset is included, as well as approximated linear functions of the deviation. As an example the DAC9106 calibration is included below:

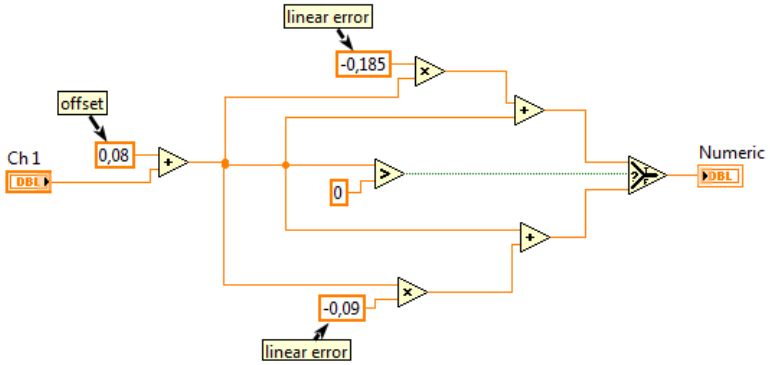


Figure 38: LabView® - Block Diagram, Calibration Funtion

Another example shows the pattern generation of a sin wave with the AD9106:

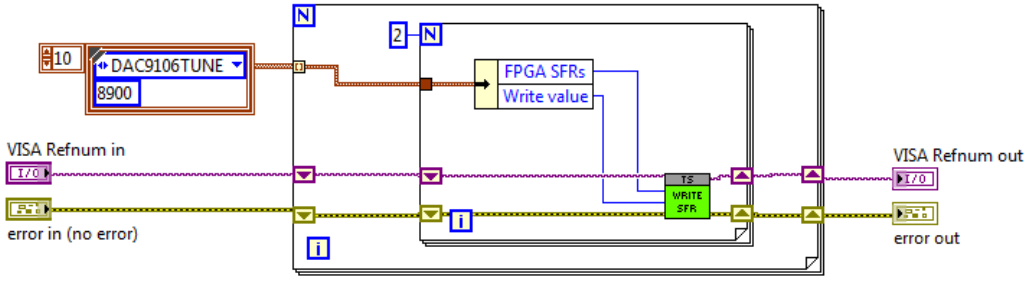


Figure 39: LabView® - Block Diagram, Pattern Generation

Basically this subVI consists of an while loop, which is auto indexed via an array. Therefore this loop is executed once for every element in this array. The array itself includes the required registers and necessary values for switching the internal multiplexer of the DAC9106 to generate a sin wave. This principle is the same for sawtooth generation and changing the frequency of a pattern.

9.0.6 TestStand®

For measuring the bode diagram, as well as for calibrating the different stages, TestStand® was used. With TestStand® different programming languages such as LabVIEW®, .NET, C/C++ DLL and many others can be included via adapters. To build an automated test, the already existing LabVIEW® functions were added. Therefore it is very important to encapsulate the functions in subVIs. The communication with the measurement equipment was done with the existing functions

in the HAL (**H**ardware **A**bstration **L**ayer). The HAL offers these functions, which can be used for the configuration of the measurement equipment. The figure bellow shows a TestStand® sequence for measuring a bode diagram.

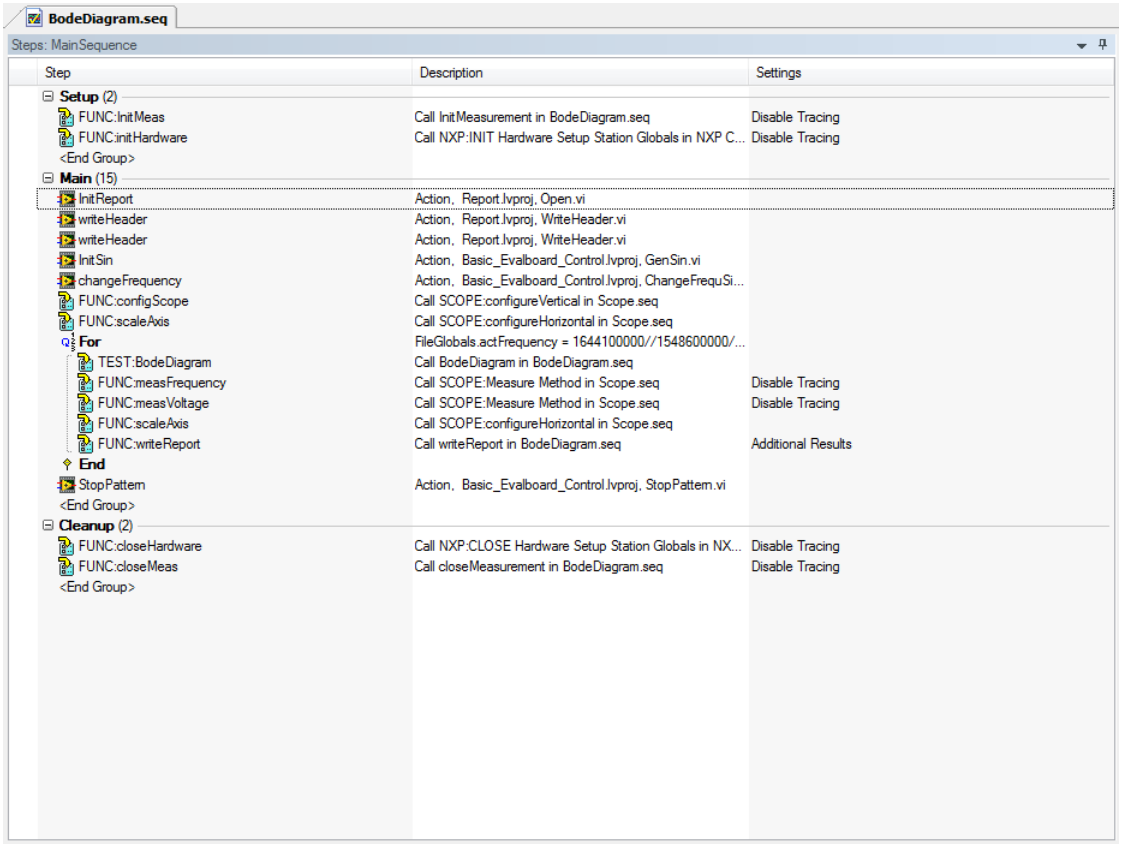


Figure 40: TestStand® Sequence - Bode Diagram

At first the whole measurement setup is initialized via an init function. In general this init function uses the HAL to get the object references of the whole measurement equipment. The other init function (InitMeas) initializes the analog channel of the evaluation board. After that a report function is called, for storing the measurement data. For measuring the bode diagram, a spi command is send to the DAC (AD9106) to change the frequency of the sin wave. This frequency, as well as the amplitude, is measured via an oscilloscope. These results are then stored in the report file. After reaching the final frequency, the pattern is stopped and the measurement hardware is closed. The big advantage of such an sequencer is that only the actual test function has to be replaced for different tests. The program structure itself can be the same for different measurements.

10 Measurements

10.1 Measurement Setup

Figure 41 shows the block diagram of the measurement setup. Where *TestStation Evalboard* represents the developed test pcb. The *FPGA Board* is used for converting the serial data stream from the windows host to a parallel data for the FPGA on the developed board. The *FPGA Board* was only used as a black box, which handles the serial communication to the windows interface.

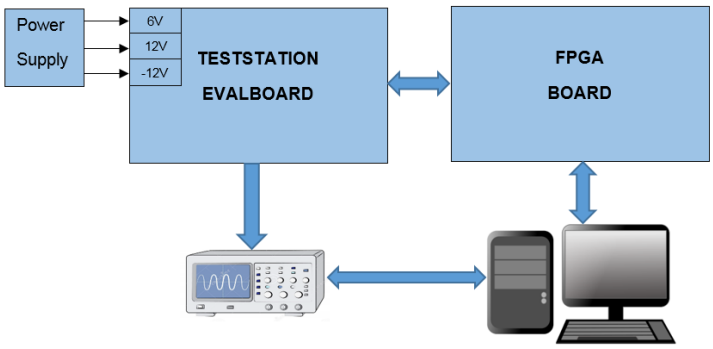


Figure 41: Measurement Setup - Block Diagram

Figure 42 shows the measurement setup in the lab. The green pcb shows the developed pcb and the pcb bellow represents the board for the serial communication with the windows interface.

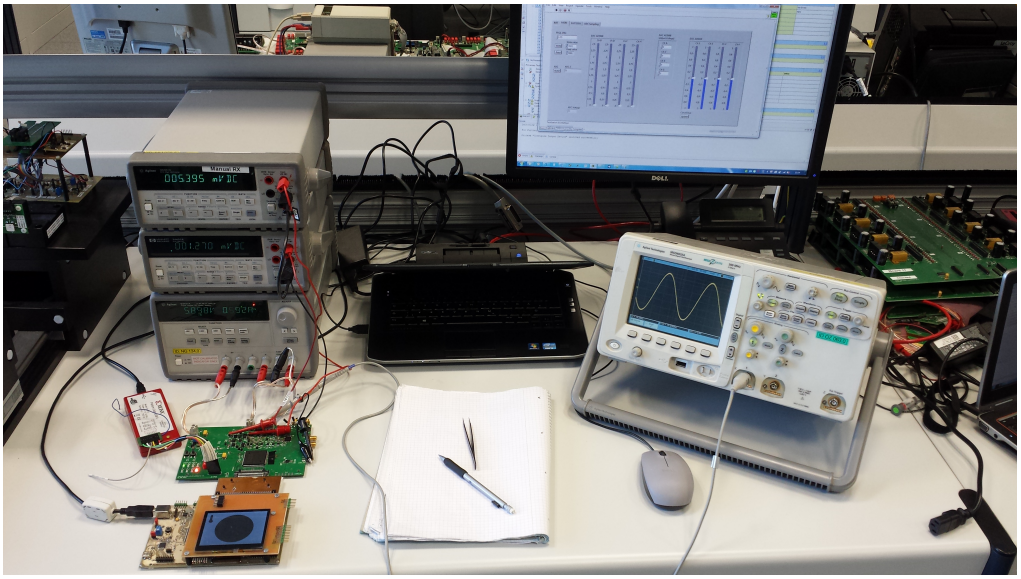


Figure 42: Measurement Setup - Lab

10.2 Testpoints

For the evaluation process, test points were added in the design. Figure 43 shows the location of these test points on the pcb. Figure 44 describes these test points.

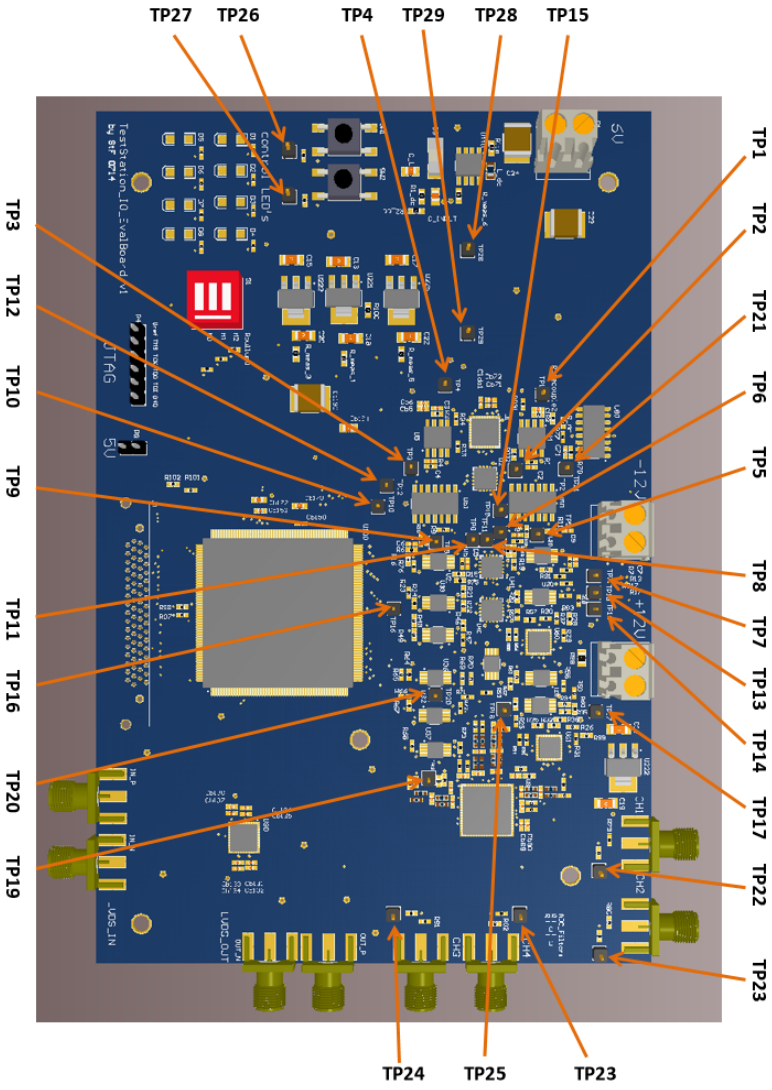


Figure 43: Testpoints for TestStation Evalboard

Testpoints for TestStation Evalboard	
Testpointnumber	**Description**
TP1	OUT CV Amp 1
TP2	OUT CV Amp 2
TP3	OUT CV Amp 3
TP4	OUT CV Amp 4
TP5	IN VV Amp 1
TP6	IN VV Amp 2
TP7	OUT VV Amp 1
TP8	OUT VV Amp 2
TP9	IN VV Amp 3
TP10	IN VV Amp 4
TP11	OUT VV Amp 3
TP12	OUT VV Amp 4
TP13	Diff_Scale 1
TP14	Diff_Scale 2
TP15	Diff_Scale 3
TP16	Diff_Scale 4
TP17	IN Diff_Scale 1
TP18	IN Diff_Scale 2
TP19	IN Diff_Scale 3
TP20	IN Diff_Scale 4
TP21	OUT CV Amp Test
TP22	OUT SMA CH1
TP23	OUT SMA CH2
TP24	OUT SMA CH3
TP25	OUT SMA CH4
TP26	Button 1
TP27	Button 2
TP28	-5V Filter 1
TP29	-5V Filter 2

Figure 44: Testpoints - Description

10.3 Register Description

This section shows a list of the whole register which are used in the digital design.

Register	Value	Description
AD8182		
MuxCNTL		
<MUX1>	0x0000	OUT 1: AD9106 - CH2
		OUT 2: AD5668 - CHD
	0x0001	OUT 1: AD5668 - CHB
		OUT 2: AD5668 - CHD
	0x0002	OUT 1: AD9106 - CH2
		OUT 2: AD9106 - CH1
	0x0003	OUT 1: AD5668 - CHB
		OUT 2: AD9106 - CH1
	0x0004	OUT1: Switching between AD9106 - CH2 and AD5668 - CHB
		with f defined in MUXFREQ
	0x0005	OUT2: Switching between AD9106 - CH1 and AD5668 - CHD
		with f defined in MUXFREQ
<MUX2>	0x0000	OUT 1: AD5668 - CHF
		OUT 2:AD5668 - CHH
	0x0010	OUT 1:AD9106 - CH3
		OUT 2: AD5668 - CHH
	0x0020	OUT 1: AD5668 - CHF
		OUT 2: AD9106 - CH4
	0x0030	OUT 1: AD9106 - CH3
		OUT 2: AD9106 - CH4
	0x0040	OUT1: Switching between AD9106 - CH3 and AD5668 - CHF
		with f defined inMUXFREQ
	0x0050	OUT2: Switching between AD9106 - CH4 andAD5668 - CHH
		with f defined in MUXFREQ
MUXFREQ		set switching frequency
AD5668		
DAC5668CNTL	0x8001	configure DAC for spi
DACA		set output voltage channel A (16 bit)
DACB		set output voltage channel B (16 bit)
DACC		set output voltage channel C (16 bit)

Figure 45: Register Description - Part 1

DACD		set output voltage channel D (16 bit)
DACE		set output voltage channel E (16 bit)
DACF		set output voltage channel F (16 bit)
DACG		set output voltage channel G (16 bit)
DACH		set output voltage channel H (16 bit)
DAC ALL		set otuput voltage of all channels
AD9106		
DAC9106SPI	0x4002	set 3-wire spi mode, MSB first
DAC9106WSEL1/2	0x0101	select constant value CH1, CH2
	0x1111	select sawtooth CH1, CH2
	0x3131	select sin CH1, CH2
DAC9106WSEL3/4	0x0101	select constant value CH3, CH4
	0x1111	select sawtooth CH3, CH4
	0x3131	select sin CH3, CH4
DACCH1AGAIN		set CH1 analog gain to [6:0] - twos complement
DACCH2AGAIN		set CH2 analog gain to [6:0] - twos complement
DACCH3AGAIN		set CH3 analog gain to [6:0] - twos complement
DACCH4AGAIN		set CH4 analog gain to [6:0] - twos complement
DACCH1DGAIN		set digital gain of +/-2 to [15:4] - CH1
DACCH2DGAIN		set digital gain of +/-2 to [15:4] - CH2
DACCH3DGAIN		set digital gain of +/-2 to [15:4] - CH3
DACCH4DGAIN		set digital gain of +/-2 to [15:4] - CH4
DACCH1SETR	0x8000	set Rref - CH1
DACCH2SETR	0x8000	set Rref - CH2
DACCH3SETR	0x8000	set Rref - CH3
DACCH4SETR	0x8000	set Rref - CH4
DAC9106OFFS1		set offset value to [15:4] - CH1
DAC9106OFFS2		set offset value to [15:4] - CH2
DAC9106OFFS3		set offset value to [15:4] - CH3
DAC9106OFFS4		set offset value to [15:4] - CH4
DAC9106PATSTART	0x0001	set RUN bit for pattern generation
DAC9106UPD	0x0001	update configuration registers

Figure 46: Register Description - Part 2

DAC9106SAW1/2		configures the sawtooth gernerator - CH1, CH2
		[15:10] - number of samples - CH1
		[9:8] - sawtooth type - CH1
		[7:2] - number of samples - CH2
		[1:0] sawtooth type - CH2
DAC9106SAW3/4		configures the sawtooth gernerator - CH3, CH4
		[15:10] - number of samples - CH3
		[9:8] - sawtooth type - CH3
		[7:2] - number of samples - CH4
		[1:0] sawtooth type - CH4
DAC9106PERIOD		set pattern period
DAC9106TIMEBASE		set timebase
DAC9106TUNEMSB		set sinus frequency - MSB
DAC9106TUNELSB		set sinus frequency - LSB
DAC9106CH1	0xX000	set constant output voltage in [15:4] - Ch1
DAC9106CH2	0xX000	set constant output voltage in [15:4] - Ch2
DAC9106CH3	0xX000	set constant output voltage in [15:4] - CH3
DAC9106CH4	0xX000	set constant output voltage in [15:4] - CH4
AD9257		
ADC9257CONFIG	0x0081	configure SPI, MSB first
ADC9257SEL1	0x000X	determine which channel receives the next write command
ADC9257SEL2	0x000X	determine which channel receives the next write command
ADC9257TRANSFER	0x0001	Set resolution/ sample rate override.
ADC9257OFF		8-bit device offset adjustment, twos complement
ADC9257ADJ		determines ouput properties
ADC9257REF		adjusts internal reference voltage
ADC9257RESOLUTION		sets resolution and sample rate
ADC9257PHASE		adjust output phase of DCO signal
ADC9257DATAA		data channel A
ADC9257DATAB		data channel B
ADC9257DATAC		data channel C
ADC9257DATAD		data channel D
ADC9257DATAE		data channel E
ADC9257DATAF		data channel F
ADC9257DATAG		data channel G
ADC9257DATAH		data channel H

Figure 47: Register Description - Part 3

10.4 Measurement Results

10.4.1 Gain Stage

At the gain stage some changes regarding the resistor values were made. Figure 6 shows the gain stage with the resistor values of R_{11} = 10 kΩ and R_7 = 100 kΩ. However the evaluation process showed, that better results were achieved with lower resistor values in the feedback path of the amplifier.

- **THS4012**

  As mentioned in chapter 3.5, two operational amps were selected for the evaluation process of the gain stage. First tests with the THS4012 showed that this amplifier could not fulfil the high requirements of the gain stage. Figre 48 shows the output signal of this amplifier with a gain of -3.7. The used resistor values for this configuration are R_{11} = 2k7 Ω and R_7 = 10 kΩ.

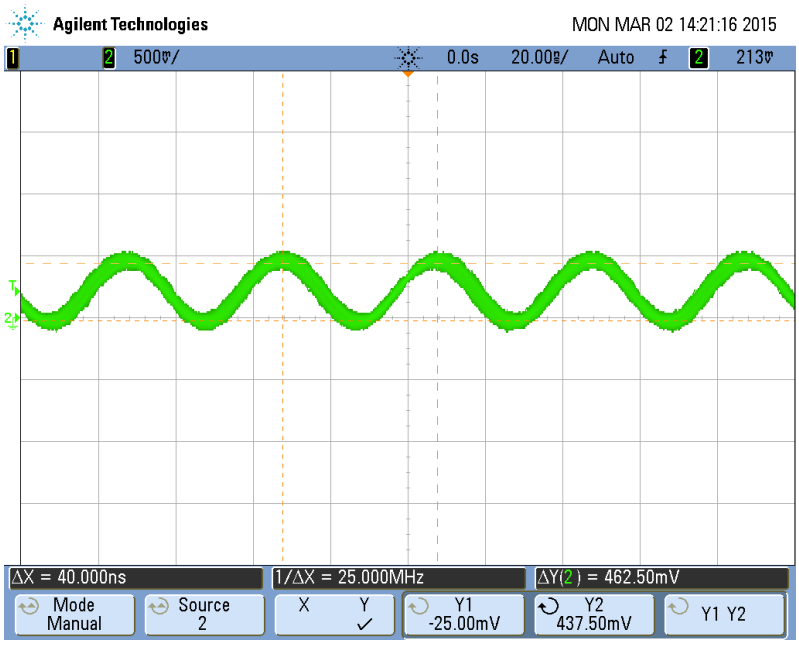


Figure 48: Multiplexer - Switching @ 25 MHz (THS4012)

It is obvious that this amplifier does not fulfil the requirements.

- **THS4022**

  The best results with this amplifier could be achieved with the resistor values as follows: R_{11} = 1 kΩ and R_7 = 10 kΩ. An additional 1 pF capacitor was added in the feedback loop of the amplifier. This results in an active filter with a cut off frequency of 15.9 MHz. The simulation

of this amplifier showed that the bode diagram has got a slight overshoot at higher frequencies. The filter compensates this overshoot. Therefore an attenuation of the amplitude, as well as a phase shift at this frequency is accepted, to achieve a better signal characteristic. Figure 62 shows the ouput signal of this amplifier at a switching frequency of 25 MHz. Thus it appears that the results are much better compared to the THS4012. Therefore all of the following measurement were done with the THS4022.

10.4.2 Shunt Resistor

As mentioned in chapter 10.4.1, the resistor values of the gain stage were decreased. This causes a lower shunt resistor inside the gain stage, to decrease the load of the amplifier. Therefore the 10 kΩ resistor was changed to 1 kΩ. The table bellow shows the new recommended measurement range for the shunt resistor.

Switch	Shunt [Ω]	Current Range [A]
OPEN	1k	10u - 10m
CLOSE	92,15	10m - 100m

Figure 49: Recommended Measurement Range - After Evaluation

10.4.3 CV Stage

The first measurements showed, that the output signal of the current to voltage stage is very noisy. The resistors in this configuration could not be changed, because of the required gain factor. Therefore different feedback capacitors were tested, with no satisfying result. Figure 50 illustrates this. Therefore the used amplifier (AD8002) was replaced. The new amplifier (AD8039) is pin compatible and has got a bandwidth of 350 MHz. The noise behaviour of this amplifier is much better. Figure 51 and 52 show the output signals of the current to voltage stage for a sin wave and a constant DC value with the new amplifier.

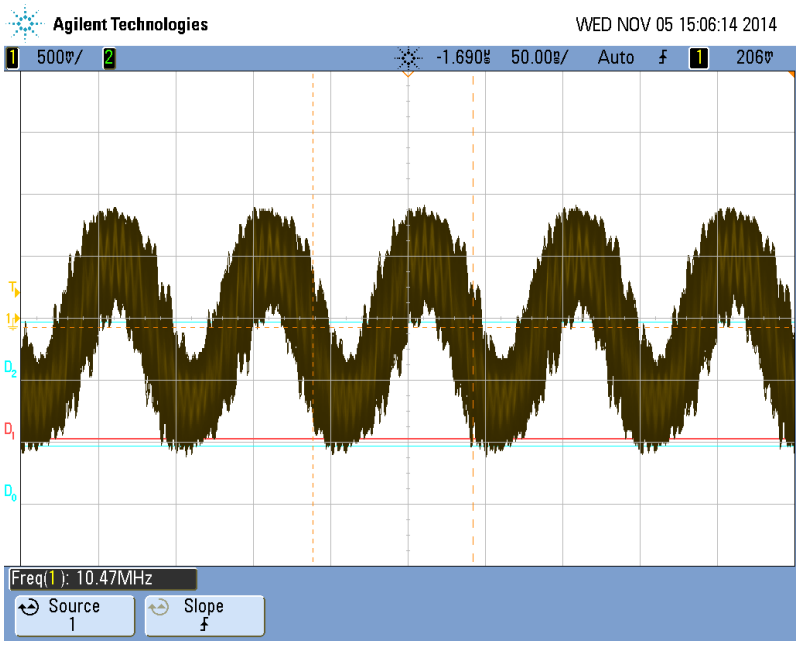


Figure 50: AD8002 - Sin Wave

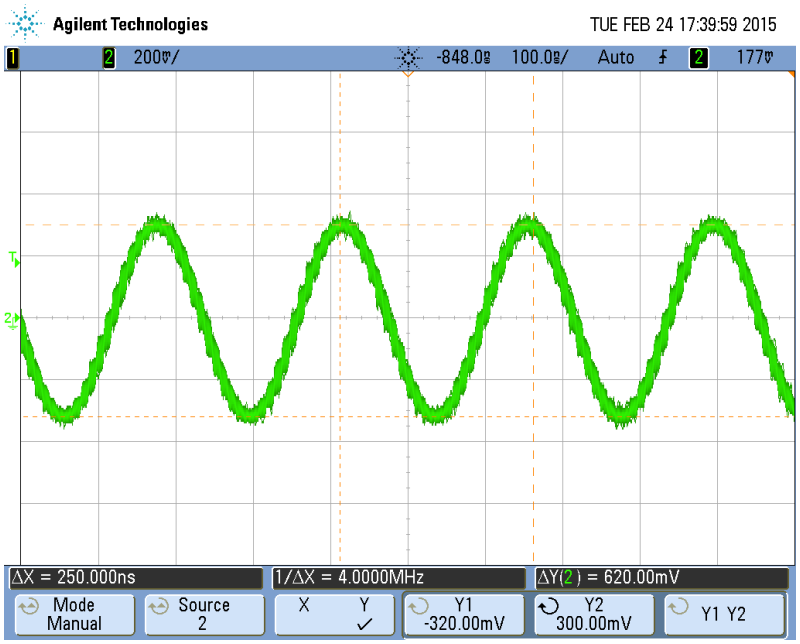


Figure 51: AD8039 - Sin Wave

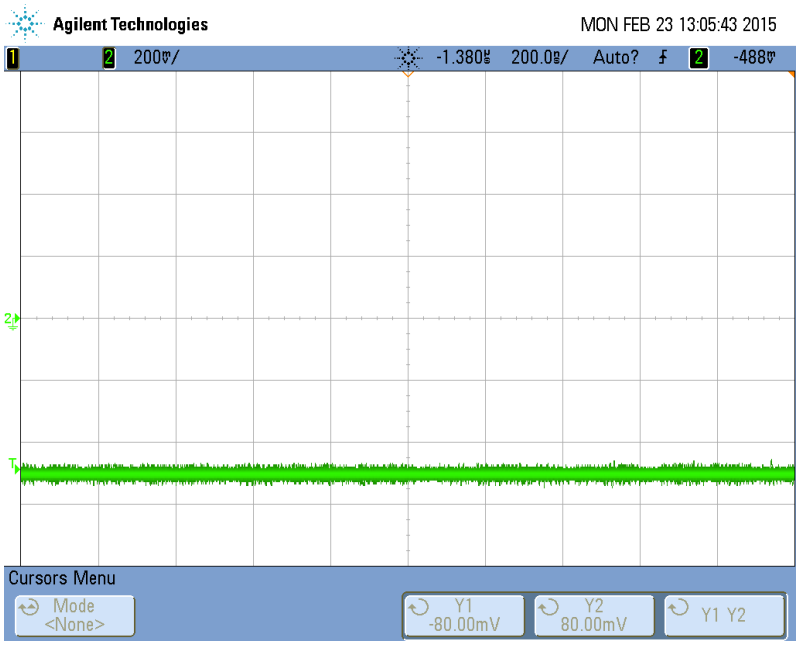


Figure 52: AD8039 - Constant Value

10.4.4 AD9106

The following pictures show different signals which were generated with the AD9106. All of these signals were measured at the output pin of the analog channel. The shunt value during the measurements was set to 1 kΩ and no load resistor was added at the output of the channel.

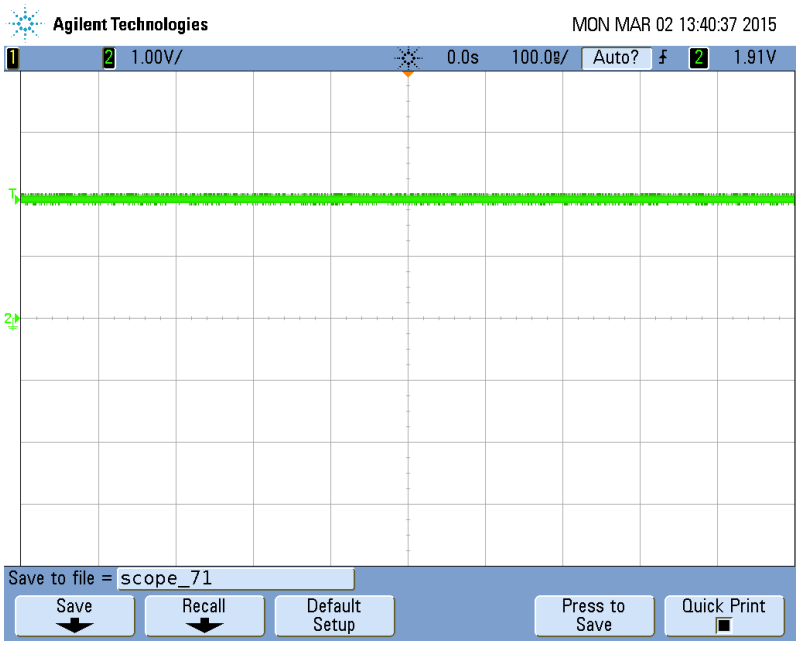


Figure 53: Constant Value

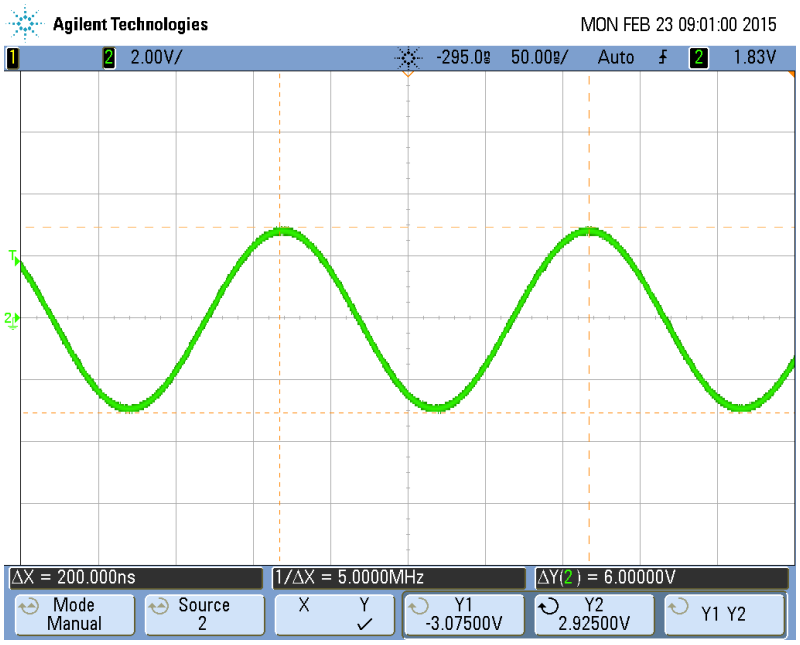


Figure 54: Sin Wave

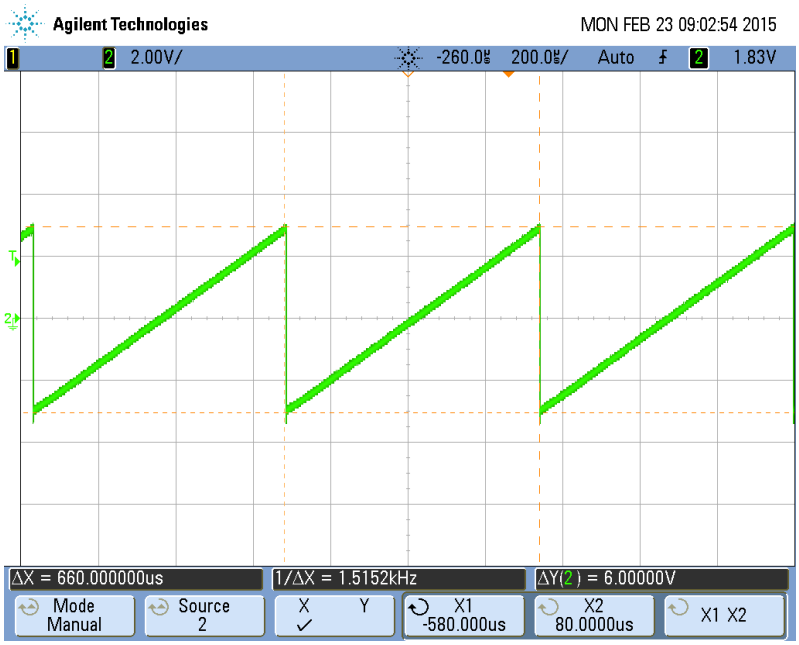


Figure 55: Positive Sawtooth Signal

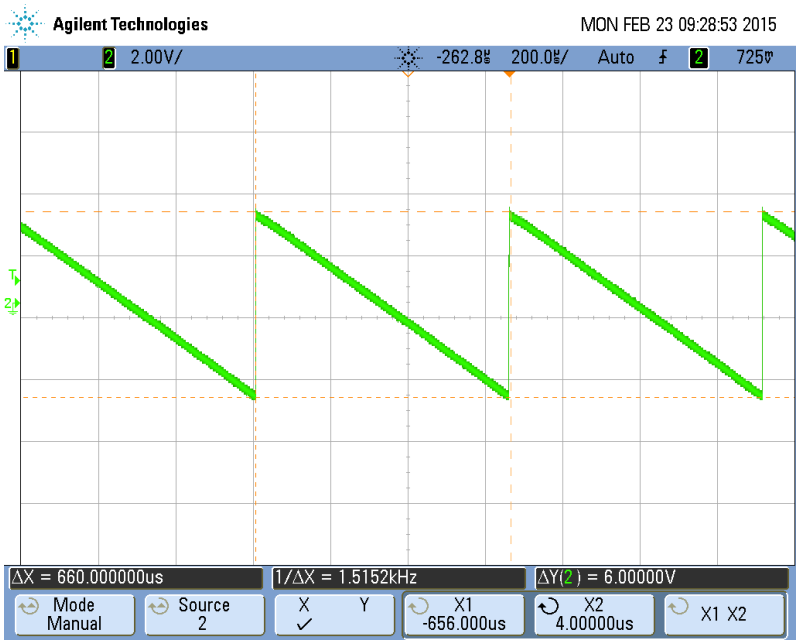


Figure 56: Negative Sawtooth Signal

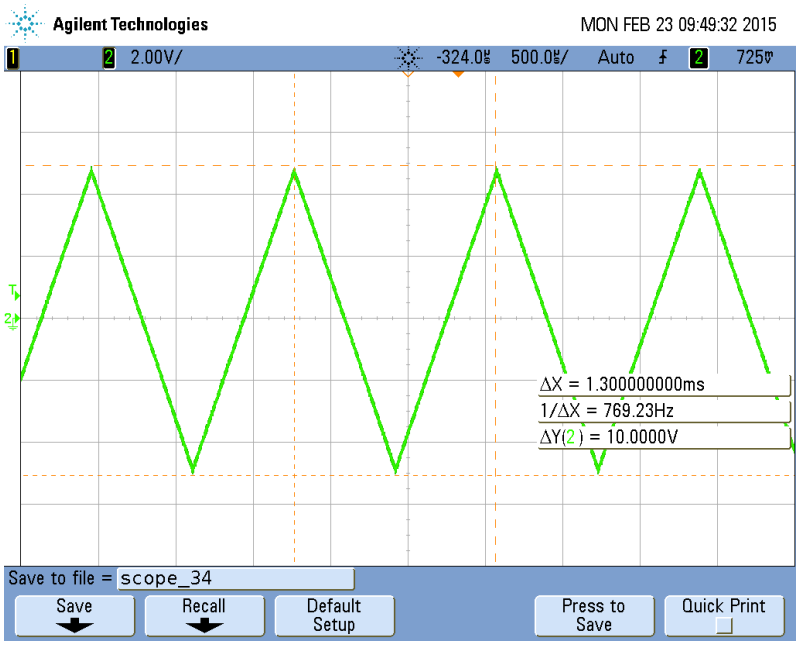


Figure 57: Triangle Wave

10.4.5 AD5668

Figure 58 shows a constant voltage level of -2 V, generated with the second DAC (AD5668). The level was measured again at the output pin. It can be seen that the signal characteristic of this DAC is very good.

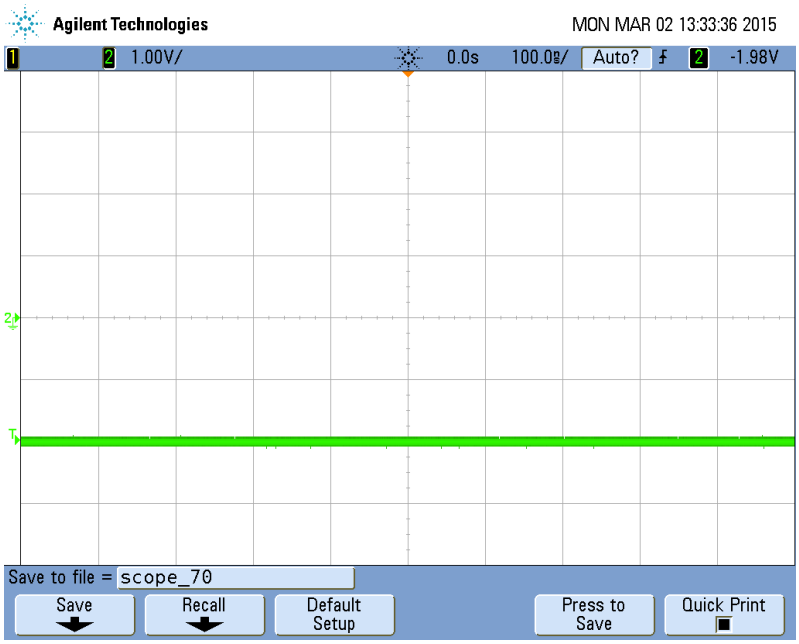


Figure 58: Constant Value

10.4.6 Multiplexer

The signals below were generated with the multiplexer, by switching between two voltage levels of the two DACs.

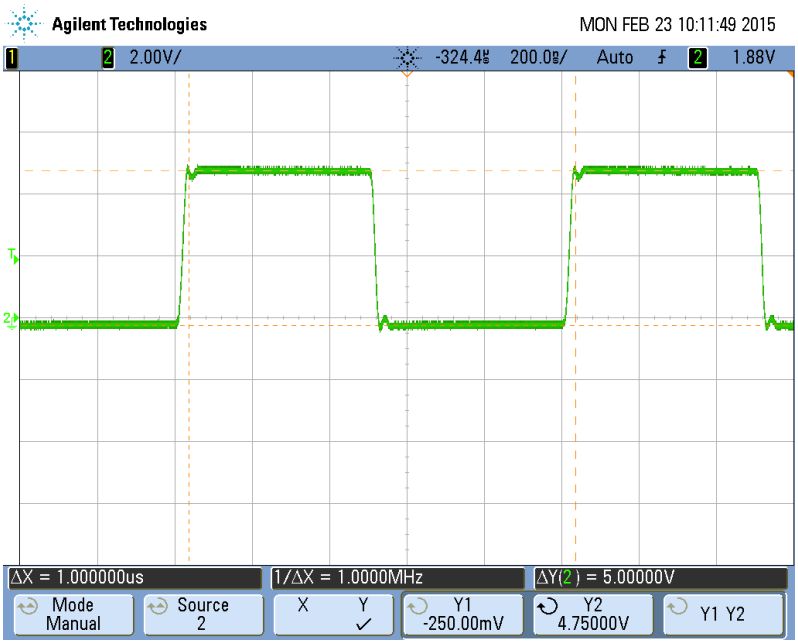


Figure 59: Multiplexer - Switching @ 1 MHz, Positive Voltage

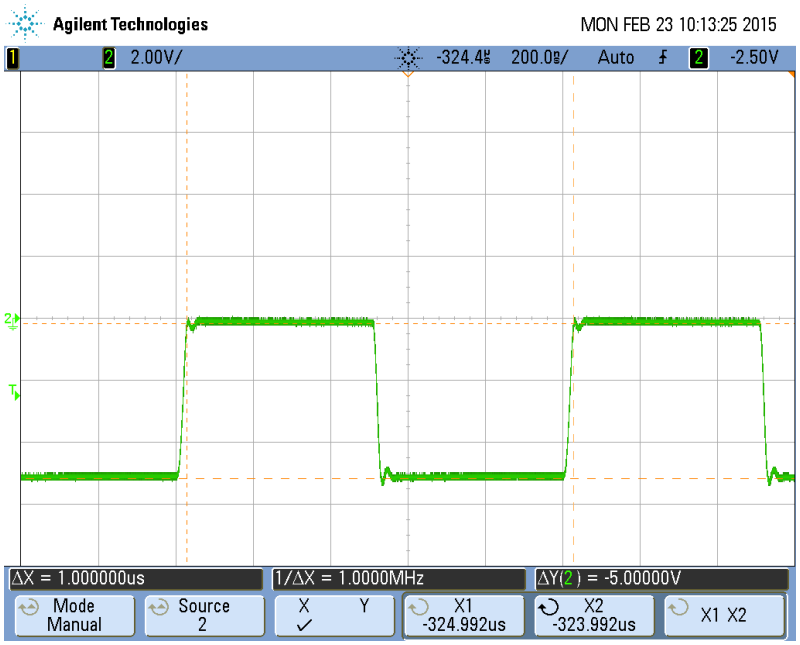


Figure 60: Multiplexer - Switching @ 1 MHz, Negative Voltage

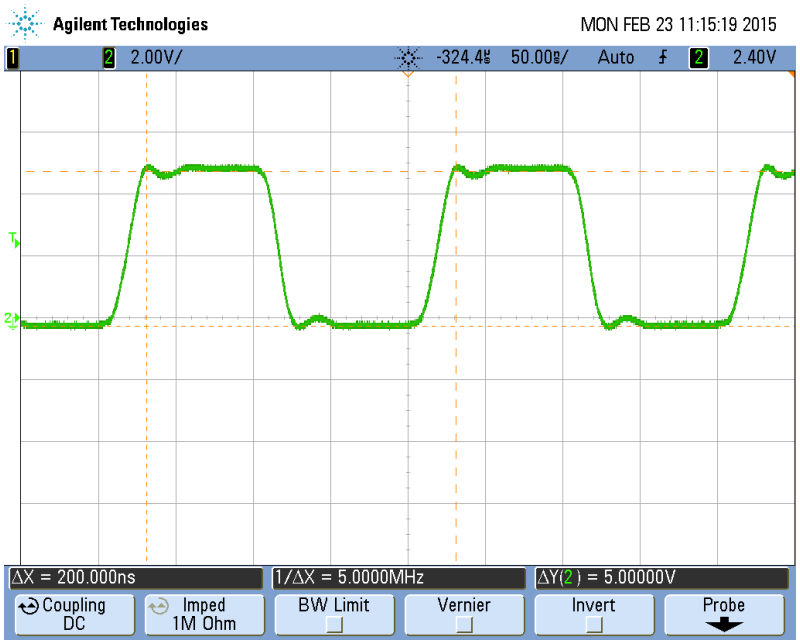


Figure 61: Multiplexer - Switching @ 5 MHz

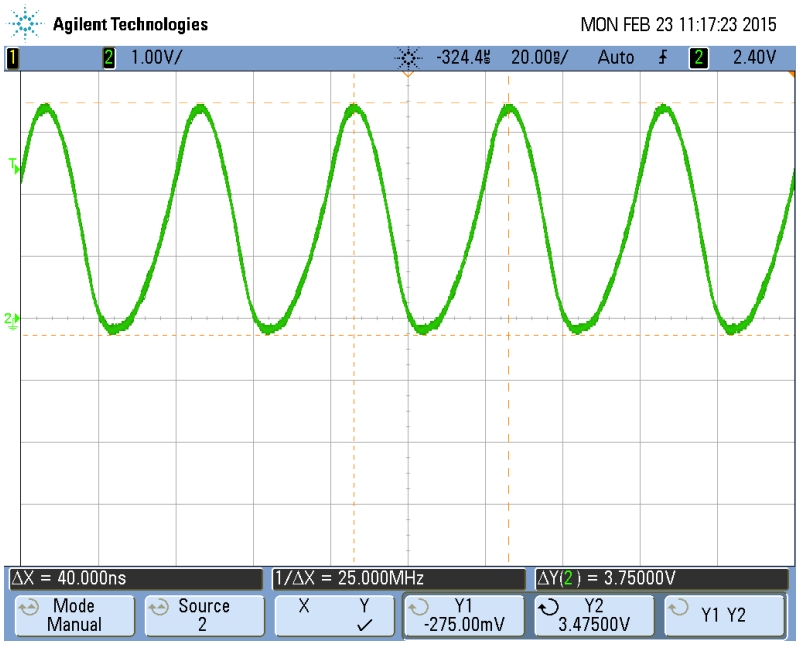


Figure 62: Multiplexer - Switching @ 25 MHz

10.4.7 Differential Stage

During the evaluation process of this stage a 140 MHz signal was measured. This swing was produced from the common mode voltage buffer (figure 20).

Figure 63 shows the swing of the common mode voltage after the buffer amp (THS4012). It represents the output signal of the amplifier, with a 100 Ω resistor in the feedback path (recommended configuration). Also other resistor values and additional parallel capacitors were tested, but without any satisfying result. This amplifier is also used with the same configuration in the differential stage. Figure 15 shows an example for that. But the 140 MHz swing occurs only after the buffer amplifier.

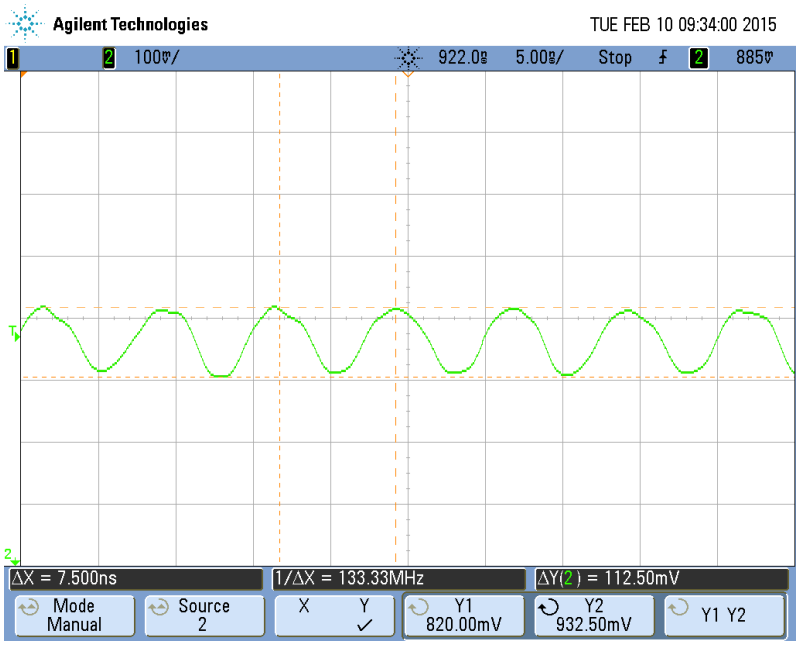


Figure 63: VCM - Buffer, 140 MHz Swing

The reason for this swing could be caused by the layout. Figure 64 shows the layout of this buffer amplifier. The signal *VCM CHIP* is here the input signal coming from the ADC. Potentially the capacitive coupling between the input and the feedback loop causes the mentioned 140 MHz swing at the output of the amplifier.

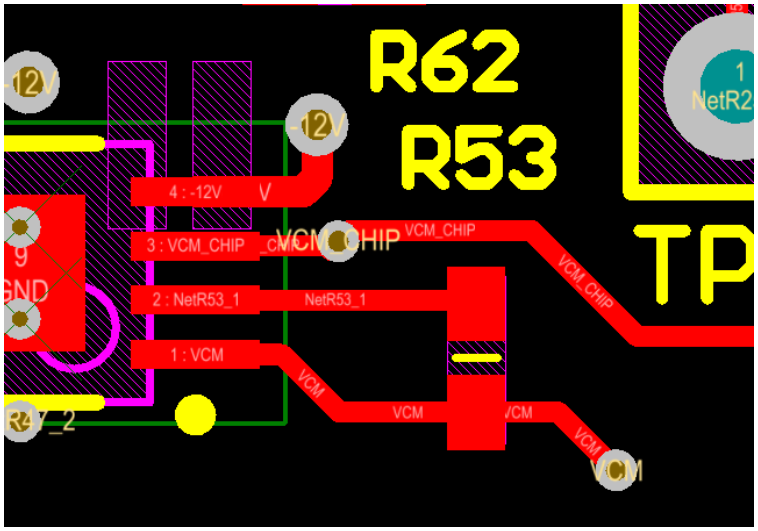


Figure 64: VCM - Buffer, Layout

Therefore the THS4012 was replaced by another pin compatible amplifier (AD8672). This amplifier has got a much lower bandwidth. With that action the swing at the output could be removed.

With the configuration in figure 17 the differential stage was at first evaluated regarding scaling the incoming signal. With the result that it is not necessary to include an amplifier for scaling the signal ahead the differential amplifier. The final circuit for that can be seen in figure 72.

The included filter after the differential stage can be seen bellow. Because of the good noise behaviour of the circuit, a low pass filter first order is sufficient to obtain a good signal characteristic at the input of the ADC.

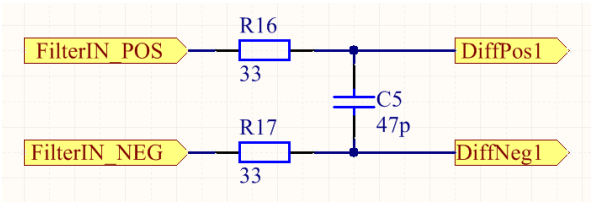


Figure 65: Used ADC Filter

The measurement results below represent the three different versions of the differential stage. All of these measurements were made under the same conditions. Also the test signal is identical for every variation to ensure a fair comparison of the different versions.

- **Version A**

  Version A uses a differential amplifier to generate the differential signal. This variation shows a very good signal characteristic at the input of the ADC, also at a frequency of 5 MHz.

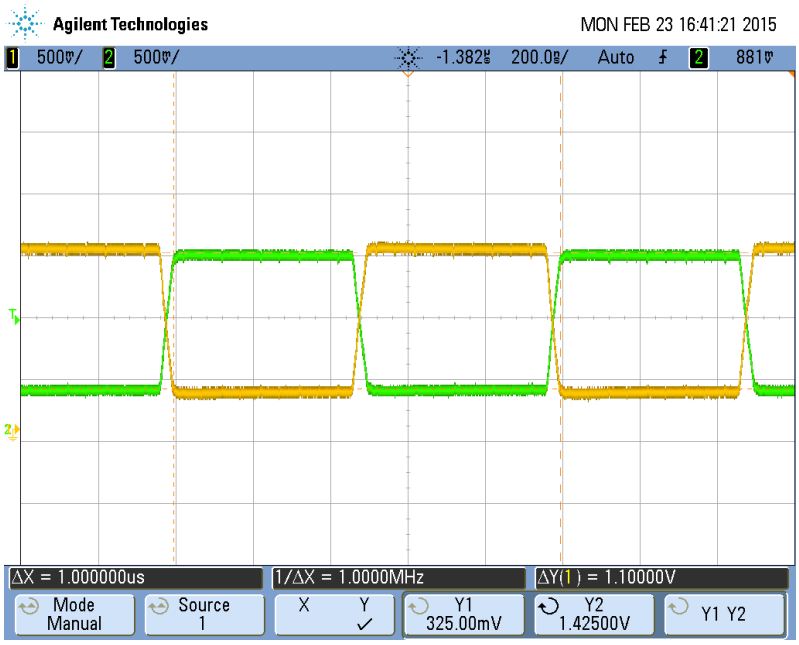


Figure 66: Differential Stage Version A - 1 MHz

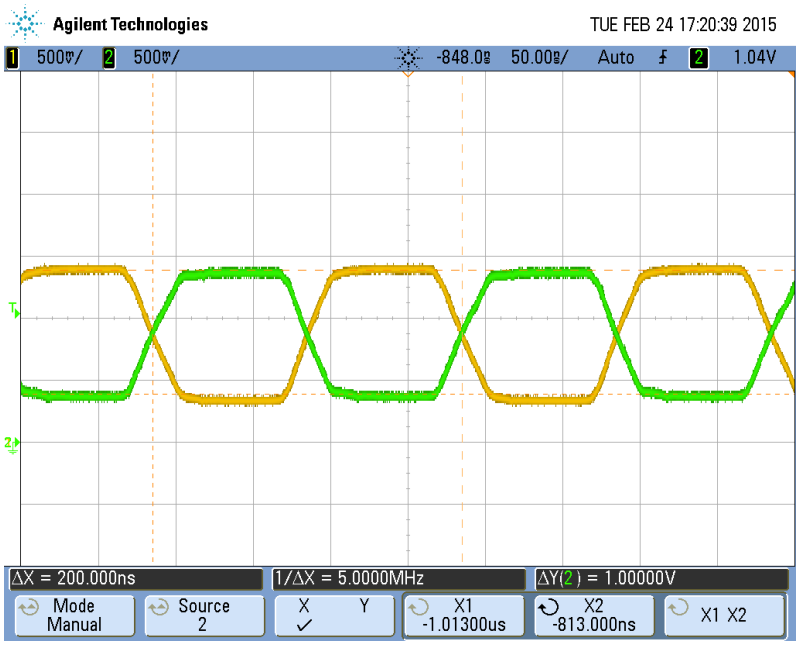


Figure 67: Differential Stage Version A - 5 MHz

- **Version B**

  This variation builds the differential signal with two operational amplifiers one after another. To scale and invert the signal, the THS4022 was at first tested to generate the first part of the differential signal. This amplifier is also used in the gain stage with a gain factor of -10. With this configuration and a gain factor of -1/10 the amplifier showed a bad noise characteristic. Therefore the THS4012 was used. The result was much better. However this amplifier has a lower bandwidth which can be seen in figure 69.

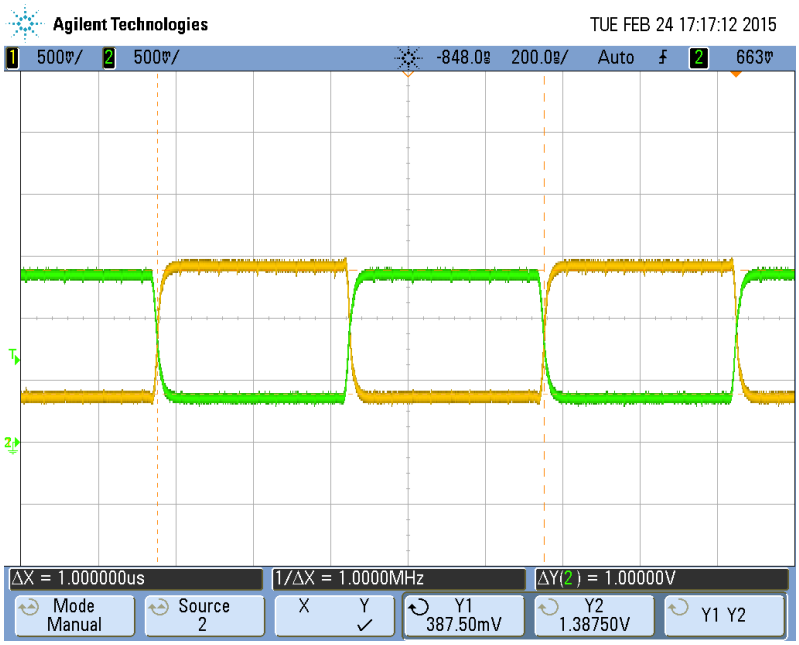


Figure 68: Differential Stage Version B - 1 MHz

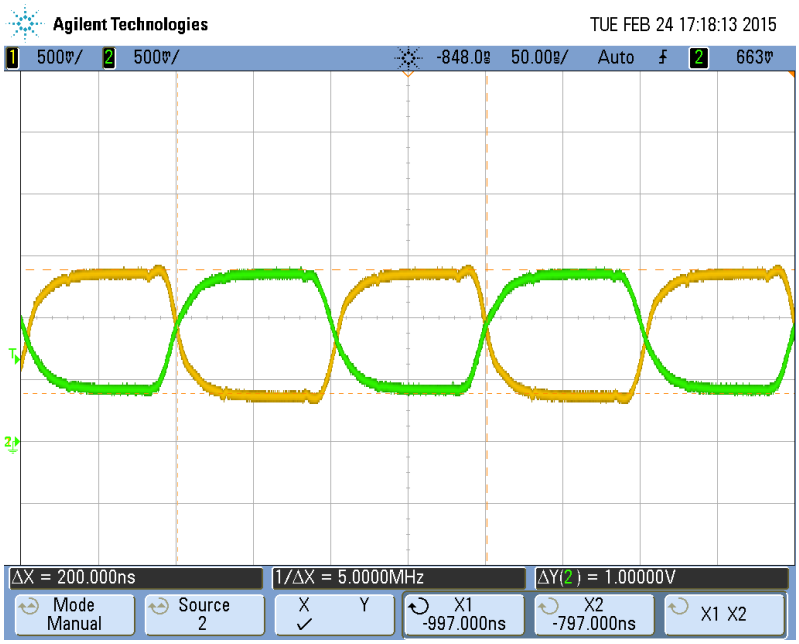


Figure 69: Differential Stage Version B - 5 MHz

- **Version C**

  The circuit for this configuration can be seen in figure 16. The 1 MHz signal shows an overshoot of the signal at every transition. At a frequency of 5 MHz this results in an unusable signal. The reason therefore could be the capacitive behaviour of the oscilloscope probe. This in combination with the shunt resistor results in an low pass first order at the output of the operational amplifier. Of course the amp tries to compensate this and therefore creates this overshoot at every transition. Potentially this could explain this signal characteristic.

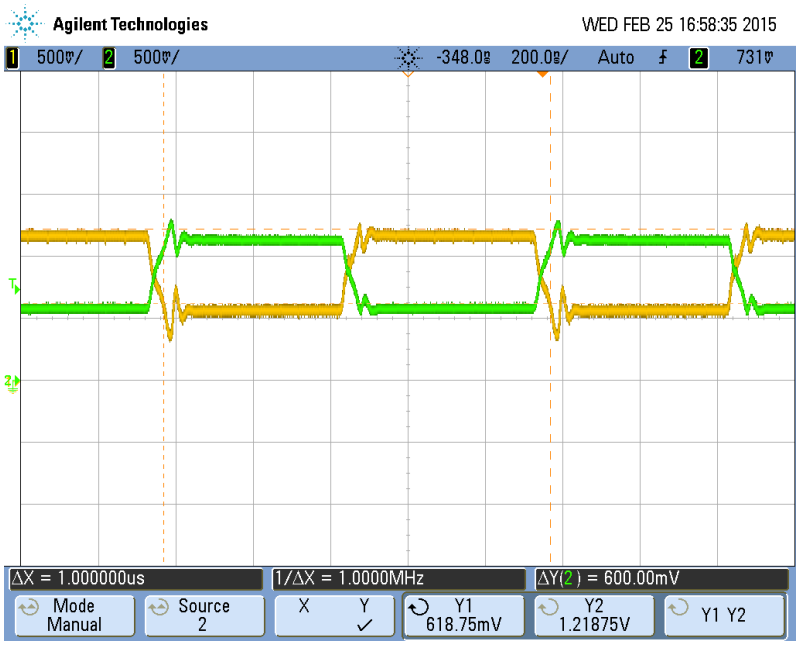


Figure 70: Differential Stage Version C - 1 MHz

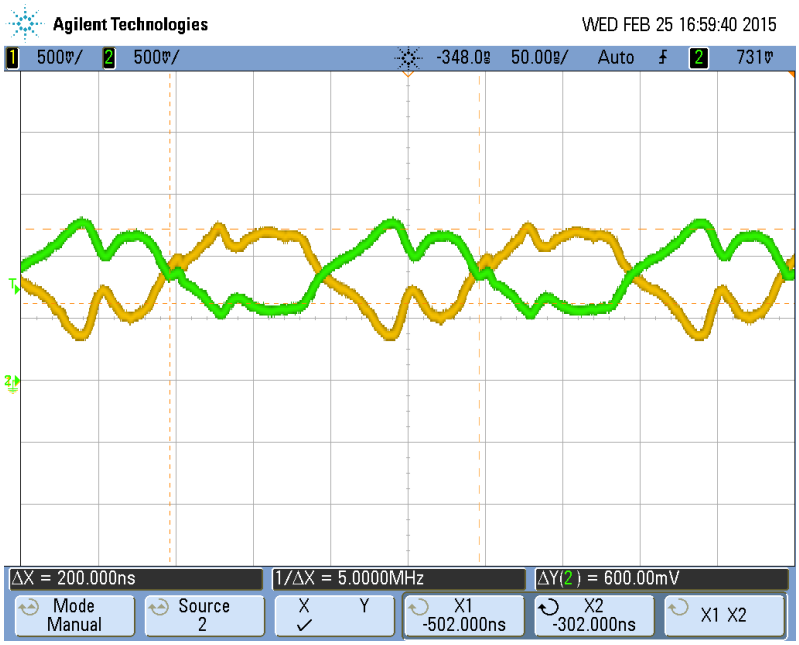
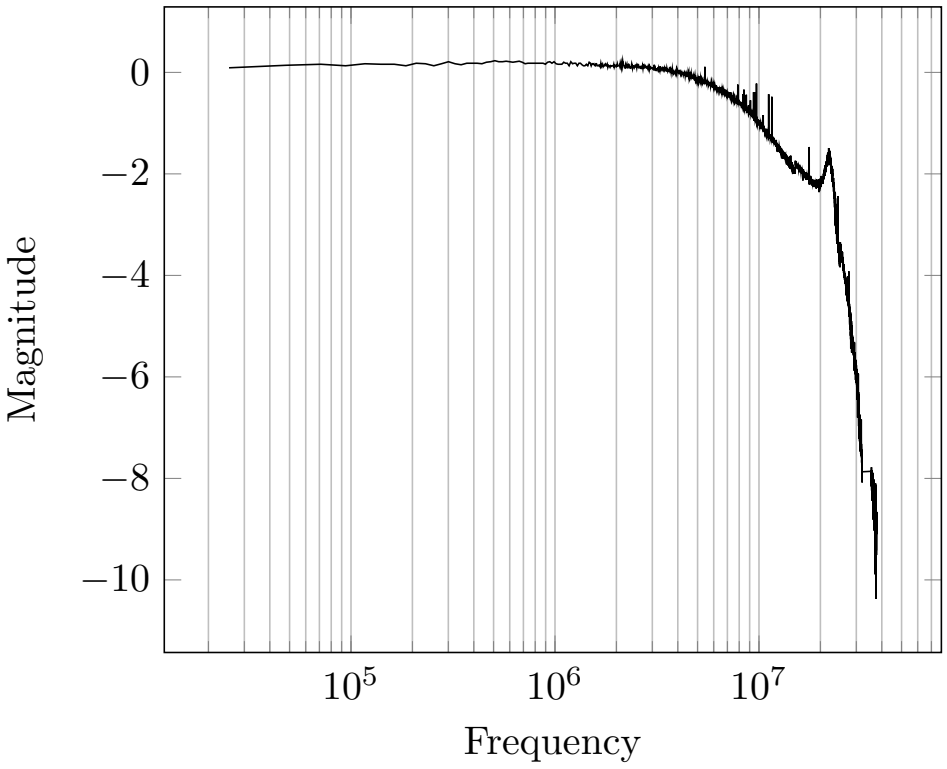


Figure 71: Differential Stage Version C - 5 MHz

10.4.8 Bode Diagram

The bode diagram of the analog channel was measured including the current to voltage stage, the multiplexer and the gain stage. The x axis represents the frequency in Hz (logarithmic scale) and the y axis the magnitude in dB. The diagram was measured with an automated TestStand® sequence as per description in chapter 9.0.6.



11 Conclusion

In the end the design of the analog channel fulfilled all of the requirements. Figure 72 shows the whole circuit of the new analog channel. This channel will then be duplicated and used in the future *TestStation*.

The first step was to create a concept for a new interface. One of the most important steps was to find the proper components for this design. Therefore the part selection was very important. It was not easy to find components which fulfilled the high requirements of the analog channel. The board design afterwards was much easier for me because of the experience of previous projects at the university. Also the fact that an Altium expert was in in my team was very useful for that. The next step was programming the FPGA which was probably the most challenging task for me. With nearly no experience in digital designs it was not easy to implement this design, which includes some thousand code lines. Also the behaviour of the FPGA during this development process was not always comprehensible. But finally the design was running very stable and most important of all, all functions could be included in the design. The user interface was one of the last steps in this thesis. Therefore LabVIEW® and TestStand® was used. With the internal National Instruments® expert in the team, the implementation of this interface could be done easier and faster than expected. The last step of the thesis was the actual evaluation of the analog channel and the different variations of it. After many hours in the lab, the final design could be presented with a satisfying result. Figure 72 shows the final circuit.

11.1 Improvements

This thesis achieved good results but of course also problems occurred during the project. Basically the data acquisition from the ADC to the FPGA was not easy. During the acquisition process the *FPGA Board*, which was used for the communication with the windows interface, influenced the measurements. This board interferes during the acquisition, because of the 75 MHz clock signal of the board. For measuring the analog signals at the output pin of the channel, this influence could be removed by simply unplugging the board after configuration and during the measurements at the pin. However during the data acquisition, the board was needed to start and control the data transmission form the ADC output to the BRAM of the FPGA. Hence occasionally bit errors occurred, which was probably caused by the influence of this board. The other improvement of the used measurement setup would be a bigger (more slices) and faster FPGA on the *TestStation Evalboard* itself. The utilization of the final digital design was above 50 percent. Therefore the routing effort inside the FPGA was very high and the routing of high speed signals barely sufficient. But this FPGA was only used for the evaluation process of the analog channel. The actual used *TestStation* FPGA offers much higher capacity and a better signal performance. Therefore this design will be used in exactly this configuration.

11.2 Outlook

As mentioned in chapter 72, the result of this thesis was very satisfying. The evaluated channel fulfilled the requirements and therefore this design will be used in the future *TestStation*. A new board design will be made, including the channel in figure 72. This channel will be duplicated as often as possible. The limiting factor therefore is the space on the future I/O board. It is very im-

portant to save space on the board to achieve a high number of channels for the future *TestStation*. Therefore the fact that most of the components have a QFN package is perfect for that. This new board will be designed by someone else, with my help and support.

Last but not least I want to thank everybody who helped and supported me during this whole project. It would be too many people to thank everybody personally. I just want to thank the whole V&V team in general, especially my mentor Harald Krepelka. Of course I also want to thank my whole family for the support during my study.

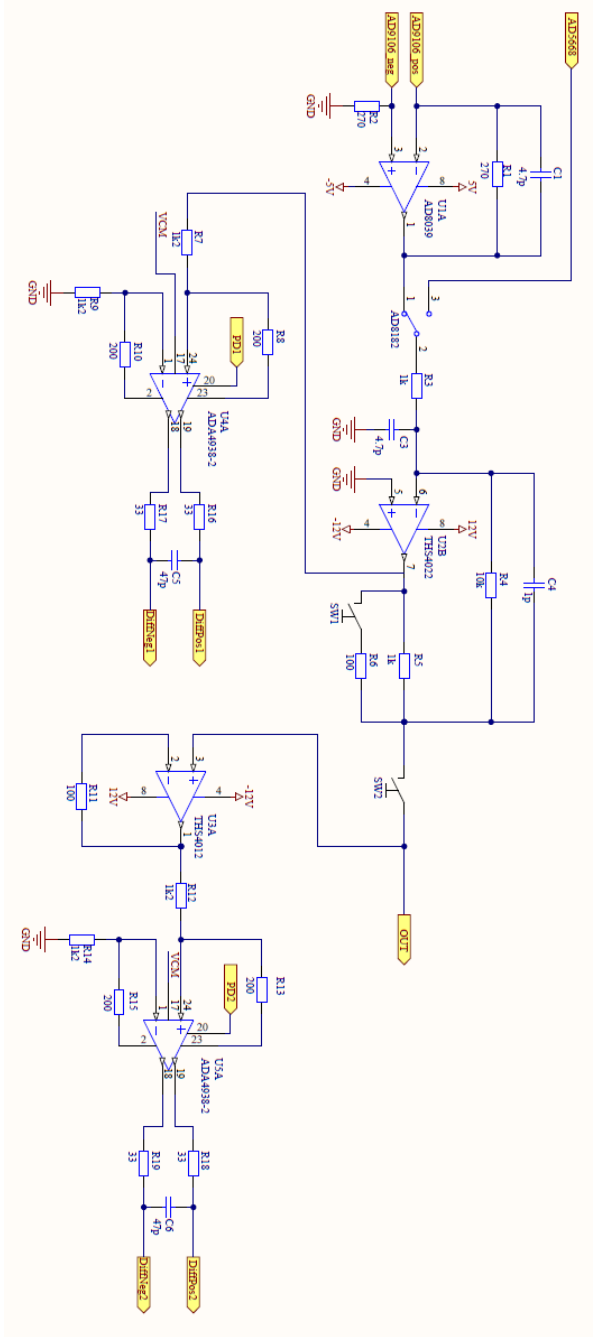


Figure 72: Final Circuit

References

[1] *The Verilog Golden Reference Guide*, August 1996.

[2] *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*, February 2005.

[3] *ADP1111 - Datasheet*, November 2009.

[4] *ISE In-Depth Tutorial*, March 2011.

[5] *Spartan-3 Generation FPGA User Guide - Extended Spartan-3A, Spartan-3E, and Spartan-3 FPGA Families*, June 2011.

[6] Wolfgang Kuerner Adolf J. Schwab. *Elektromagnetische Vertraeglichkeit*. Springer Verlag, 2011.

[7] Samir Palnitkar. *Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition*. Prentice Hall PTR, 2003.

[8] Robert Pease. *Analog Circuits - World Class Designs*. Elsevier, 2008.

[9] Etienne Sicard Sonia Ben Dhia, Mohamed Ramdani. *Electromagnetic Compatibility of Integrated Circuits: Techniques for low emission and susceptibility*. Springer Verlag, 2001.

A PCB

A.1 Schematic

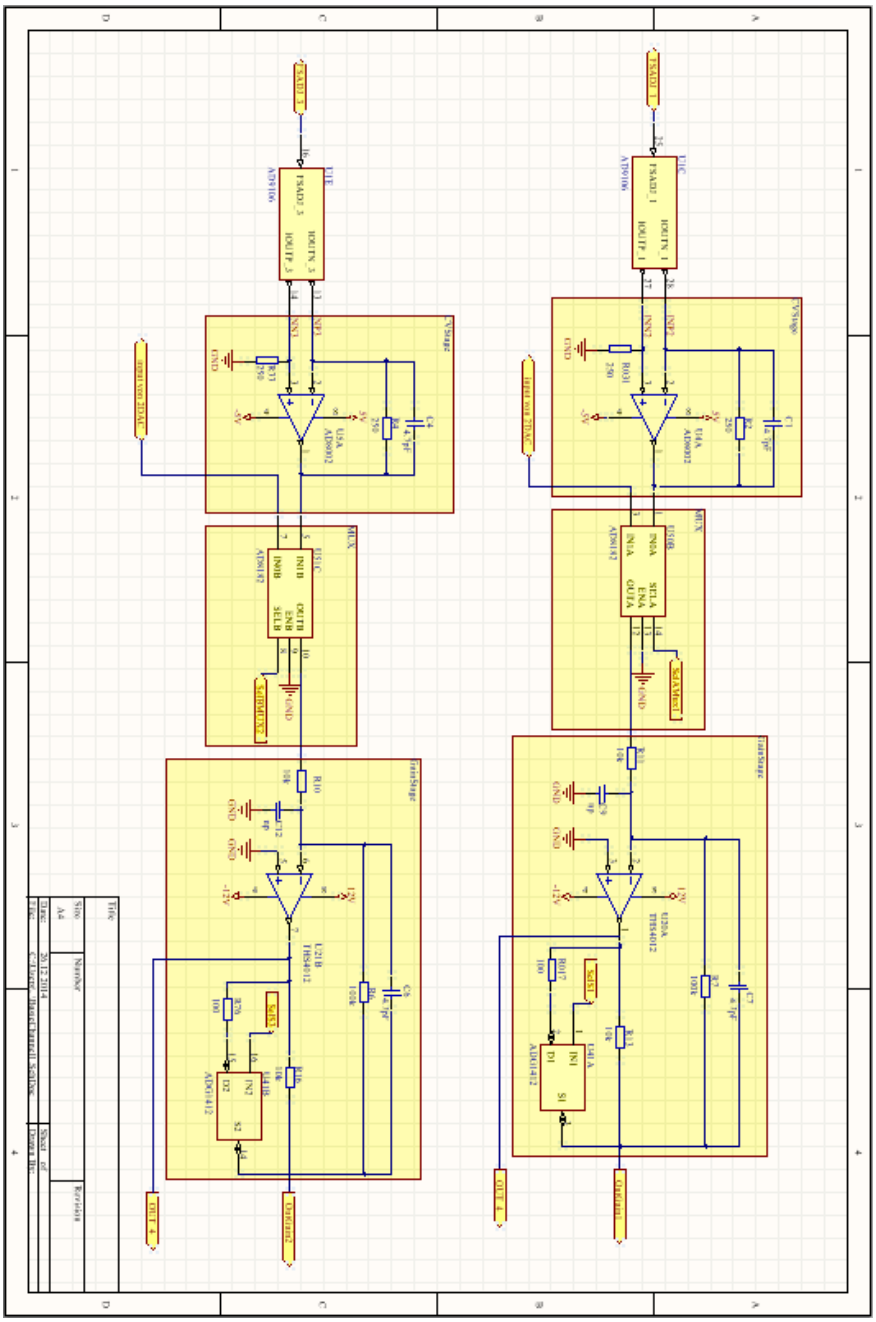


Figure 73: Schematic - Channel 1 and Channel 3, Part A

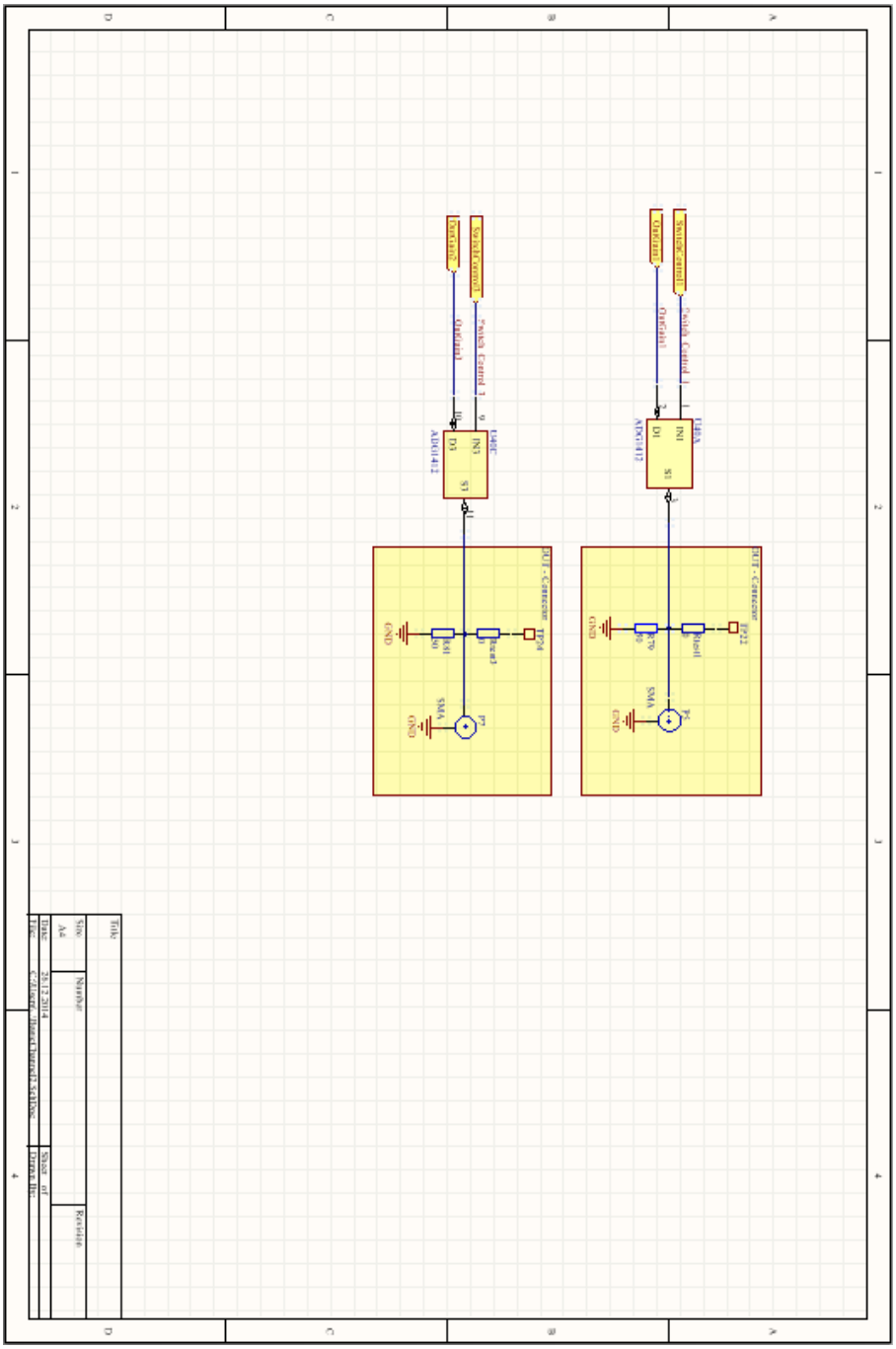


Figure 74: Schematic - Channel 1 and Channel 3, Part B

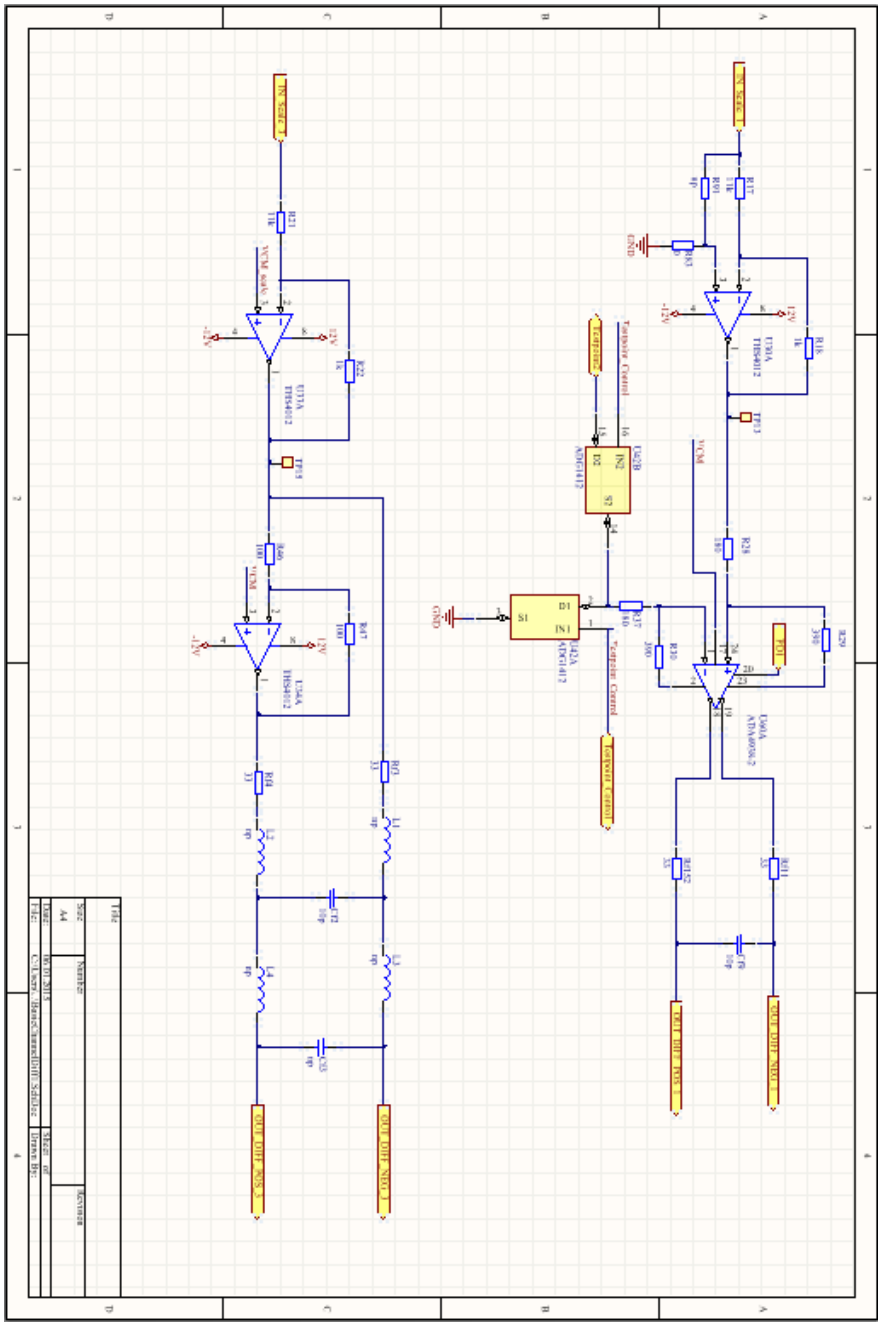


Figure 75: Differential Stage @ Gain Stage - Channel 1 and Channel 3, Part A

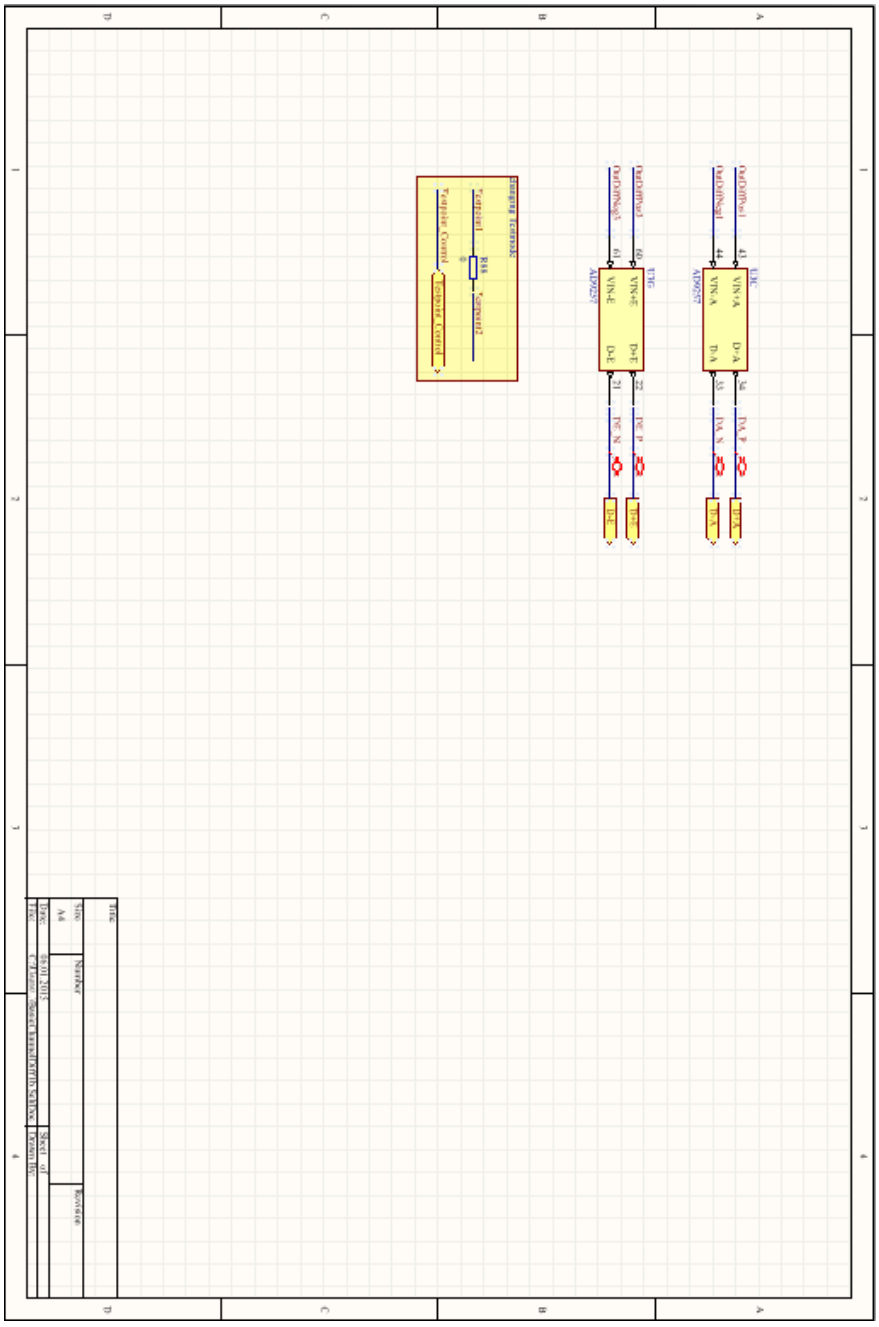


Figure 76: Differential Stage @ Gain Stage - Channel 1 and Channel 3, Part B

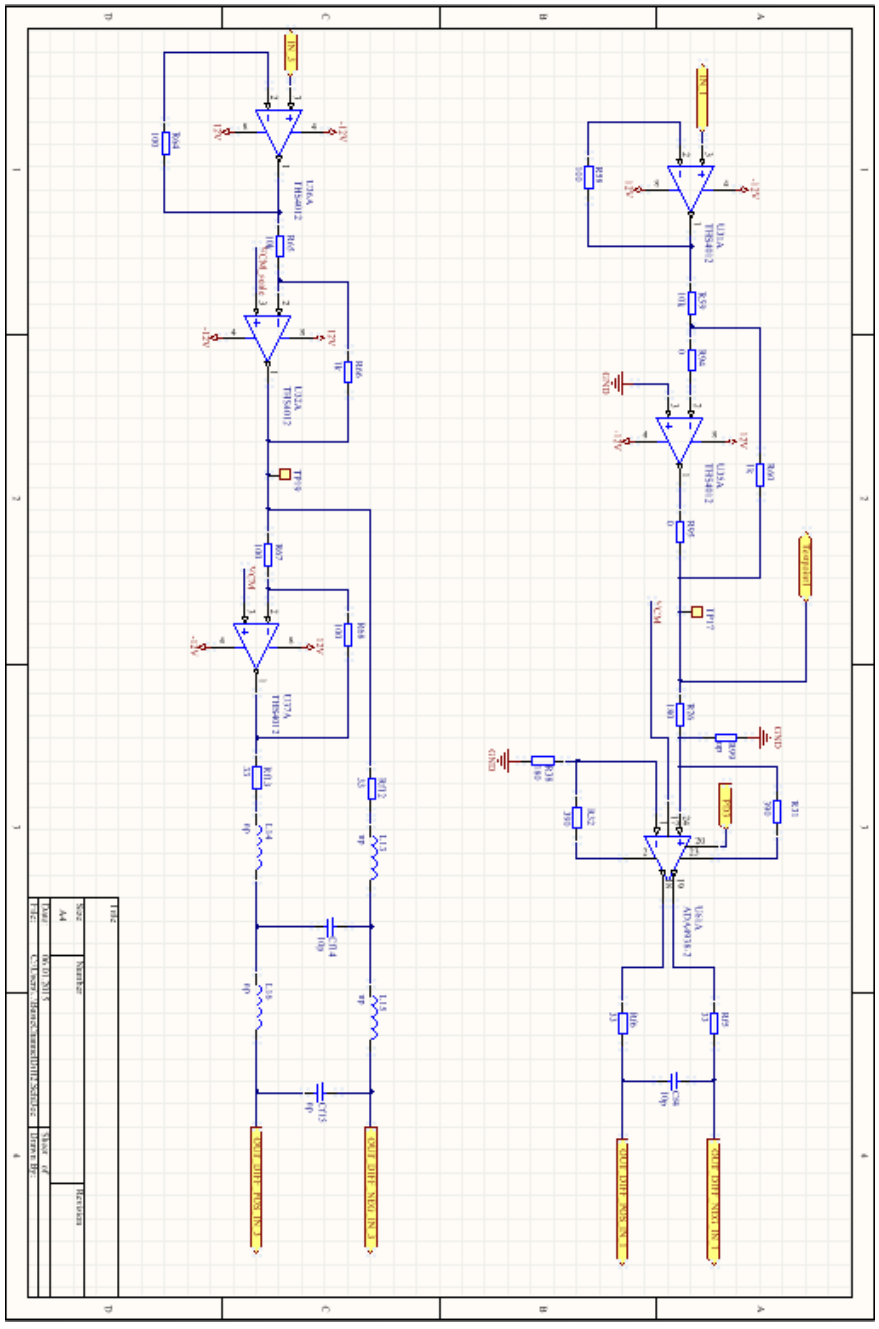


Figure 77: Differential Stage @ Output - Channel 1 and Channel 3, Part A

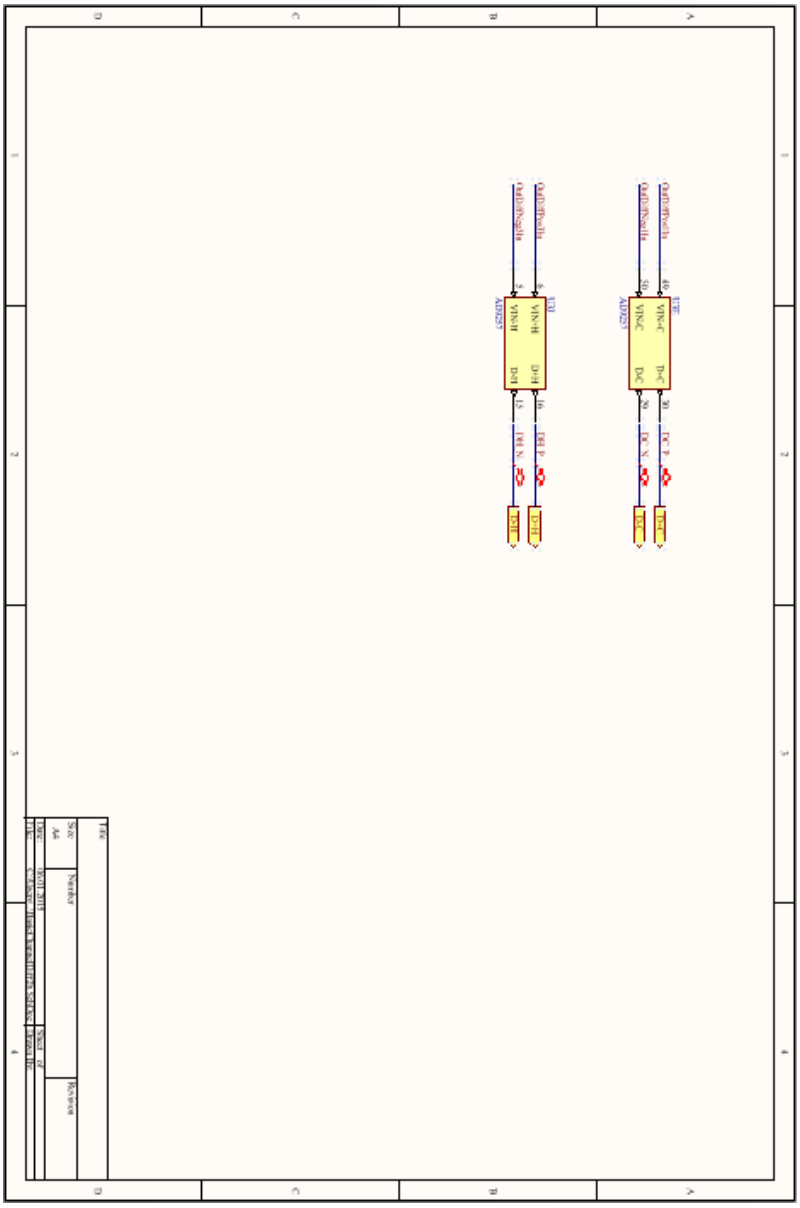


Figure 78: Differential Stage @ Output - Channel 1 and Channel 3, Part B

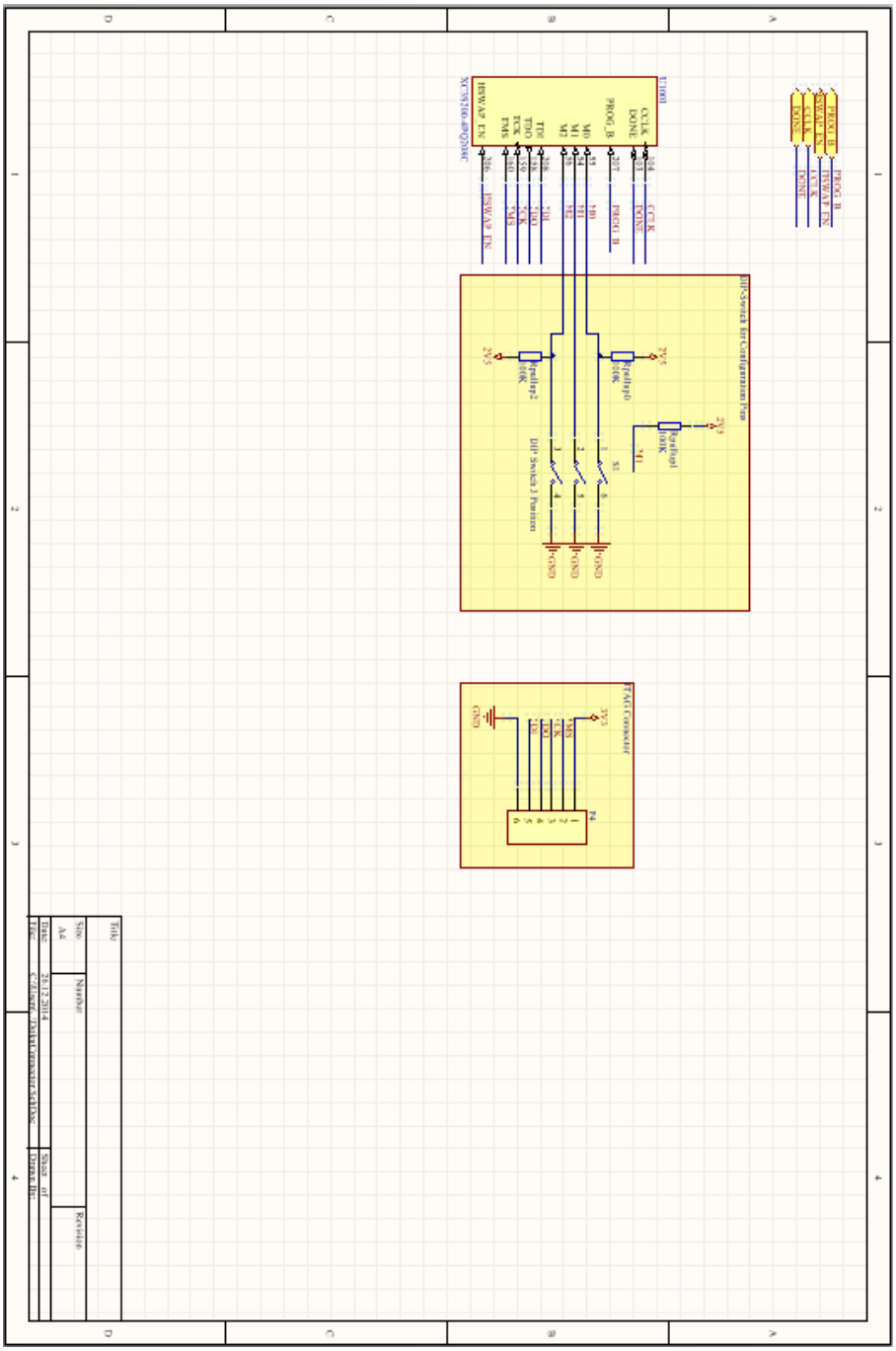


Figure 79: JTAG Connector and Configuration Pins

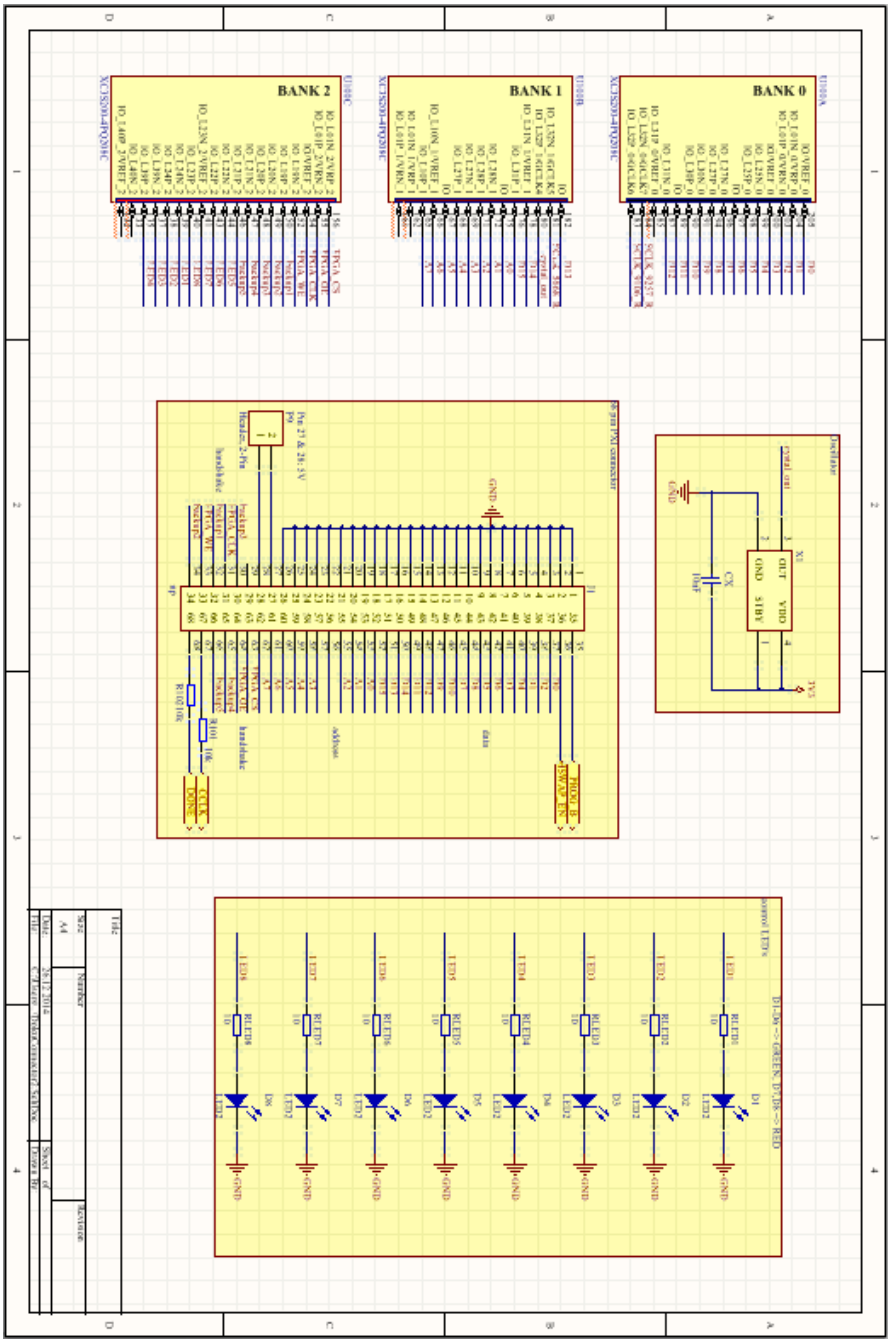


Figure 80: 68 Pin Connector, Oscillator and Testleds

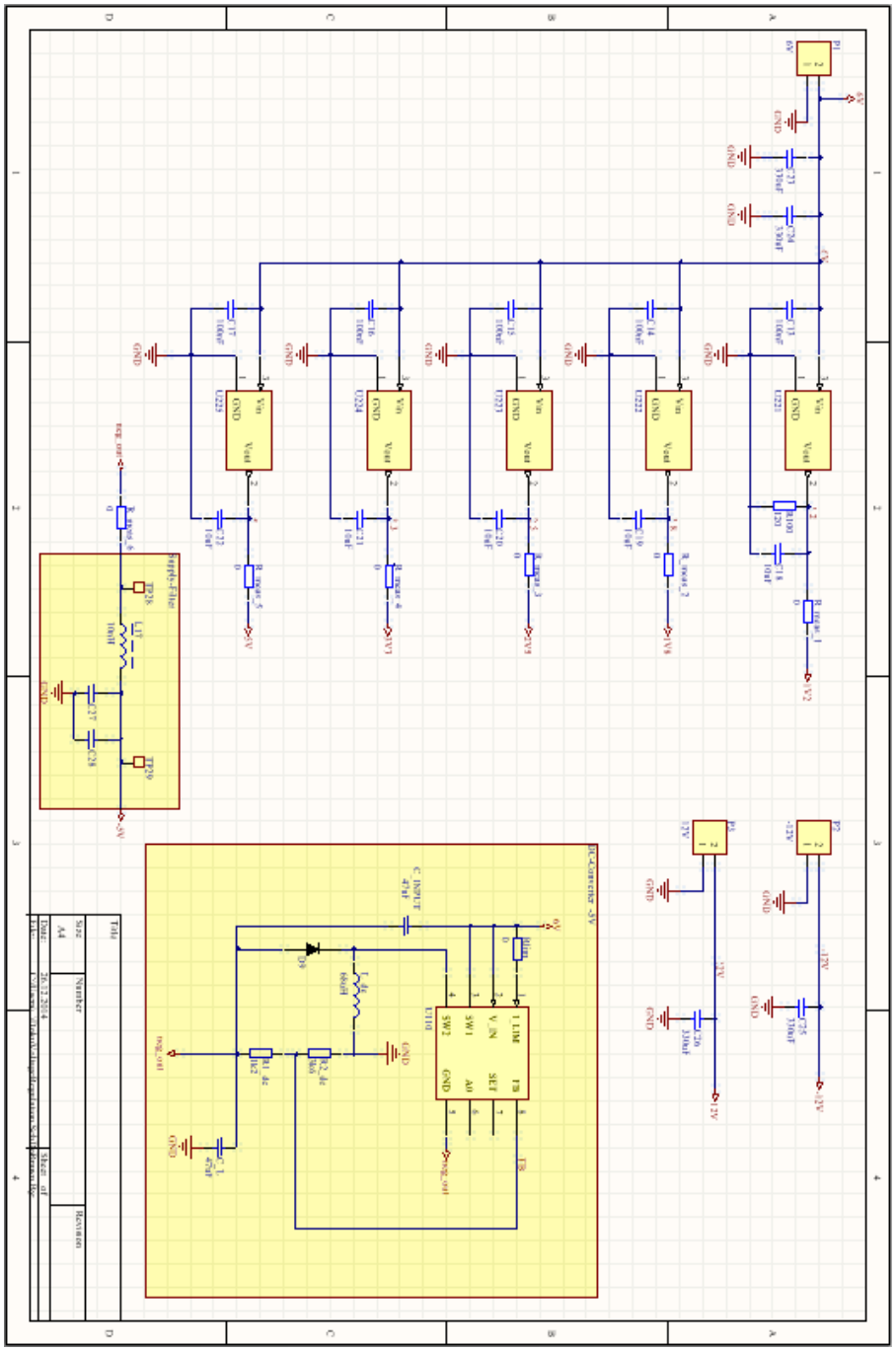


Figure 81: Voltage Regulators

A.2 Layout

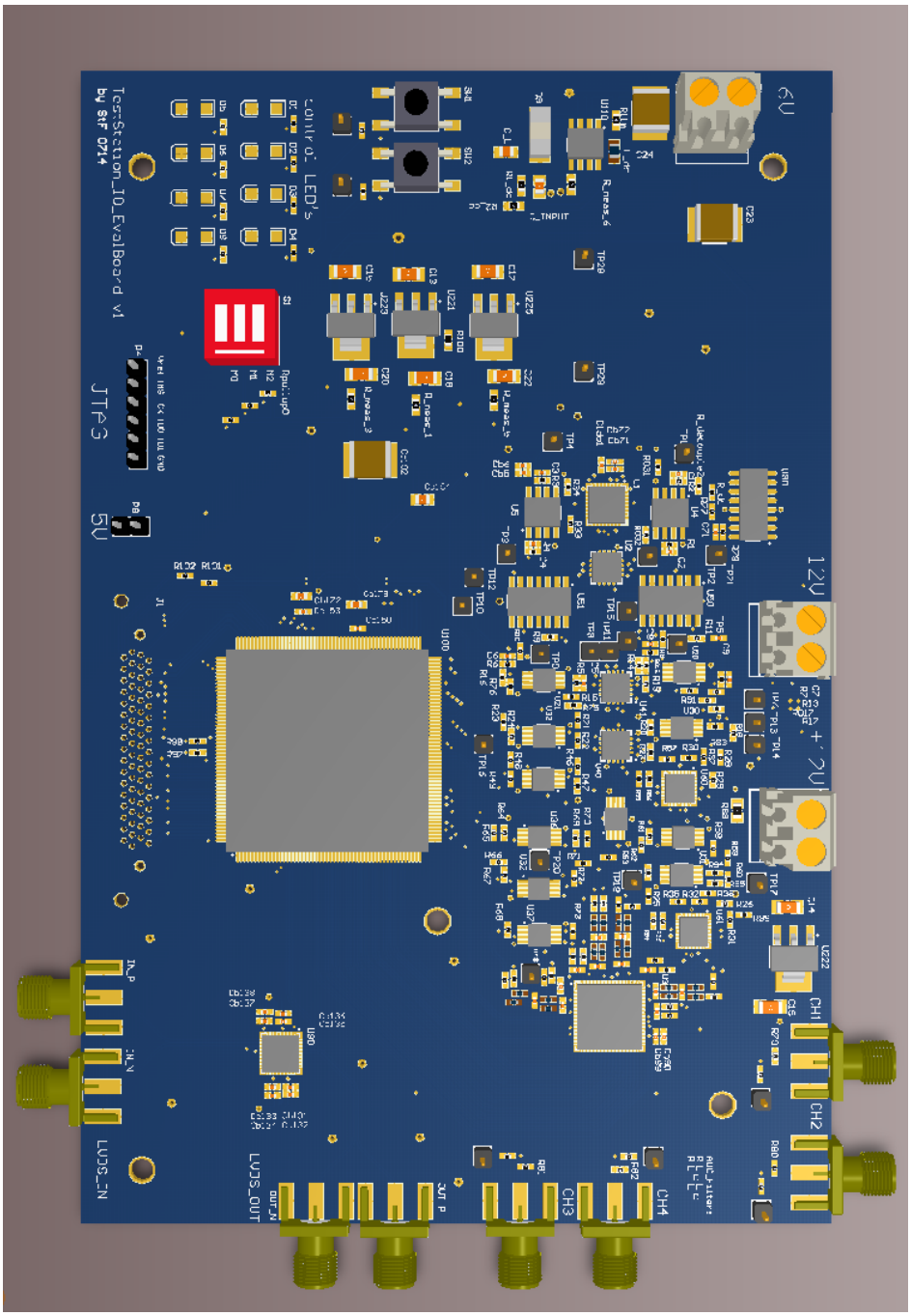


Figure 82: PCB - Top View

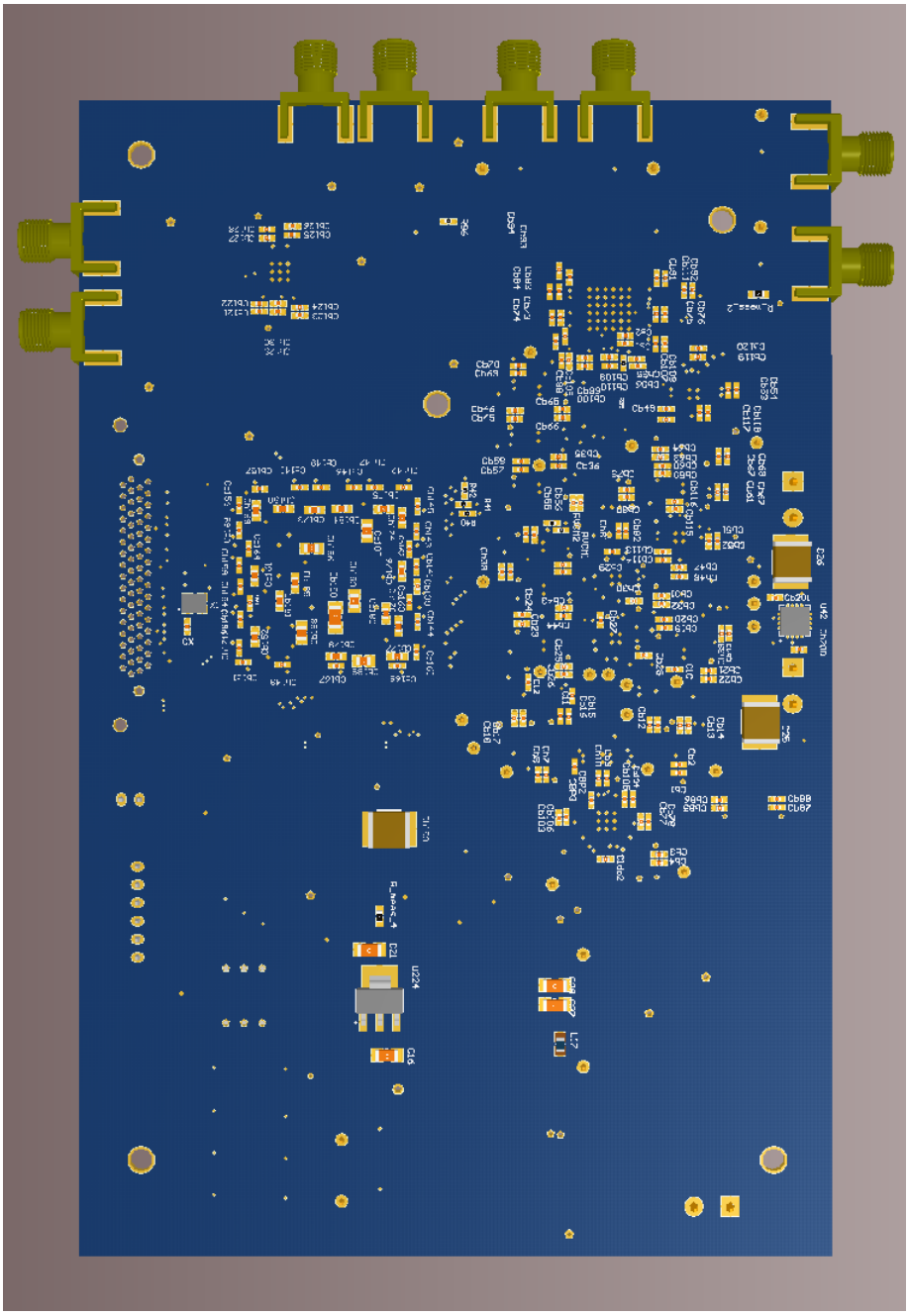


Figure 83: PCB - Bottom View

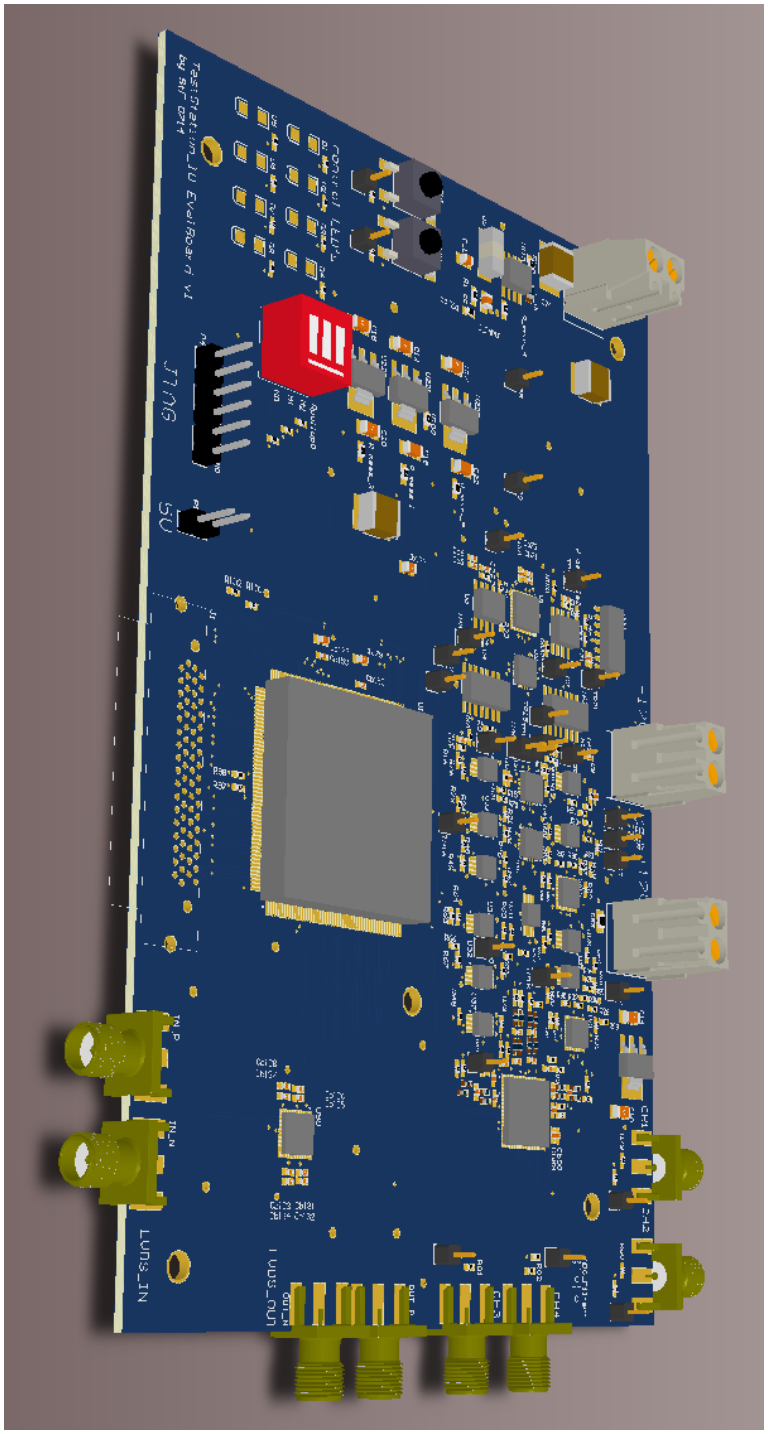


Figure 84: PCB - Side View

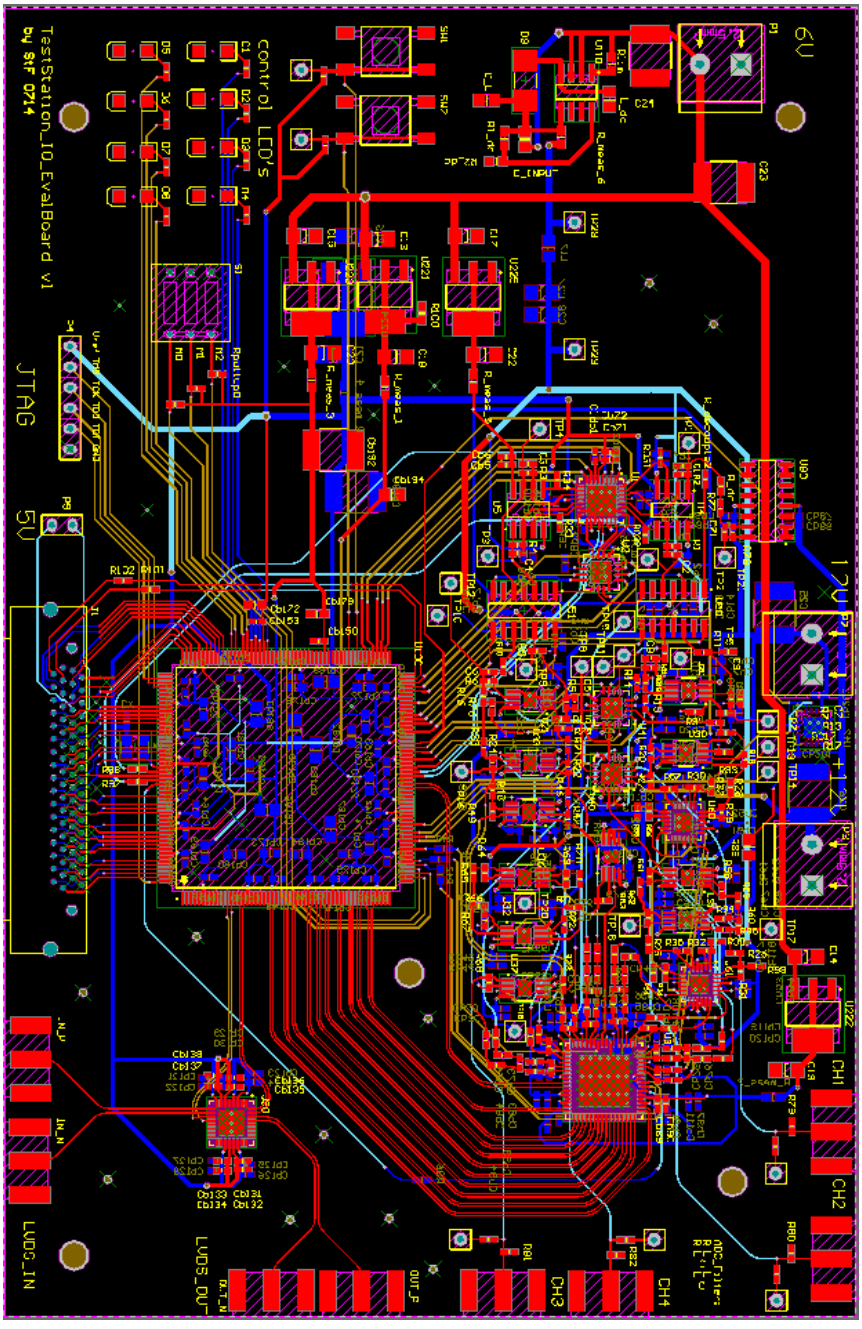


Figure 85: PCB Layout - all Layers

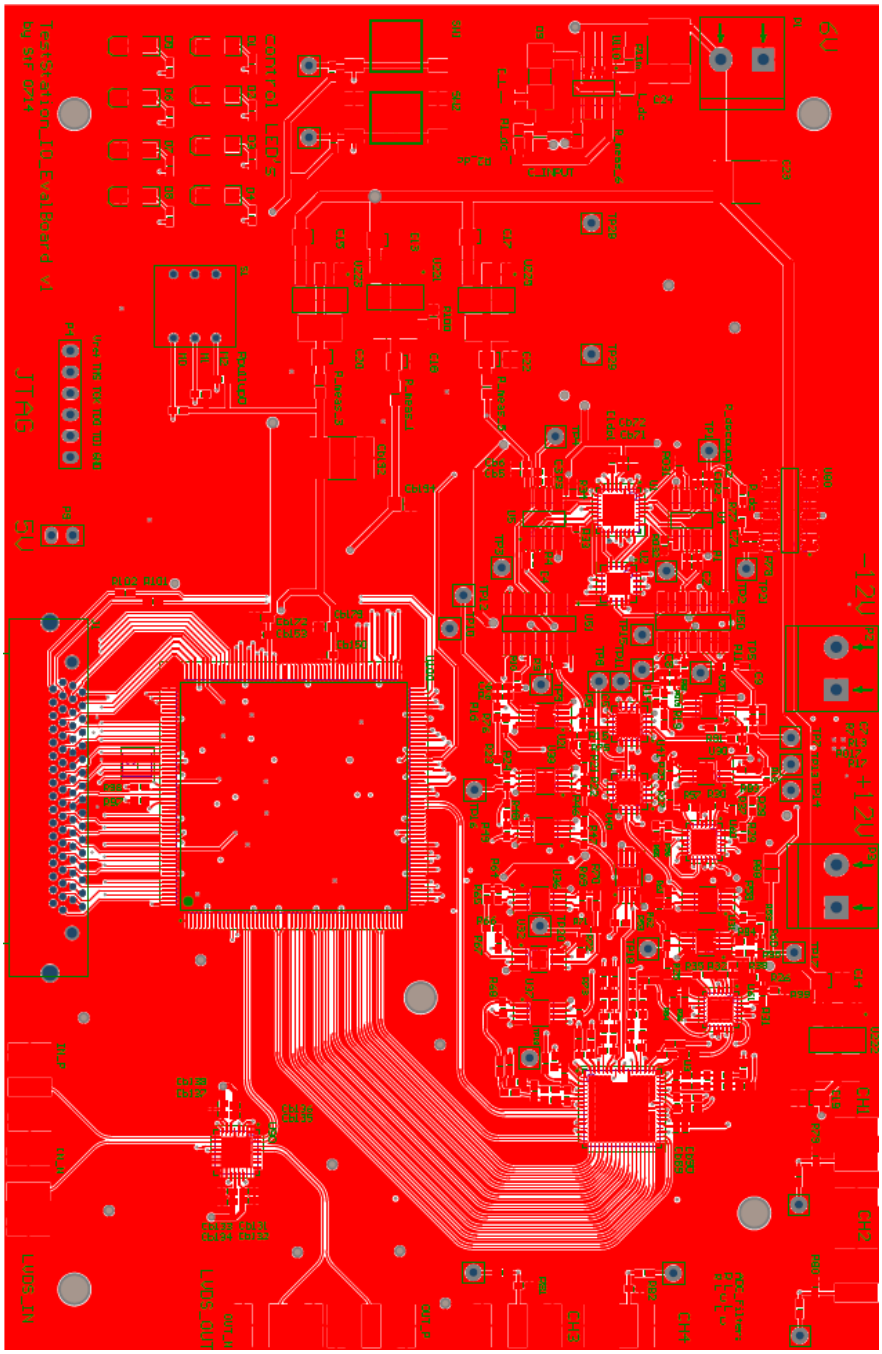


Figure 86: PCB Layout - Top Layer

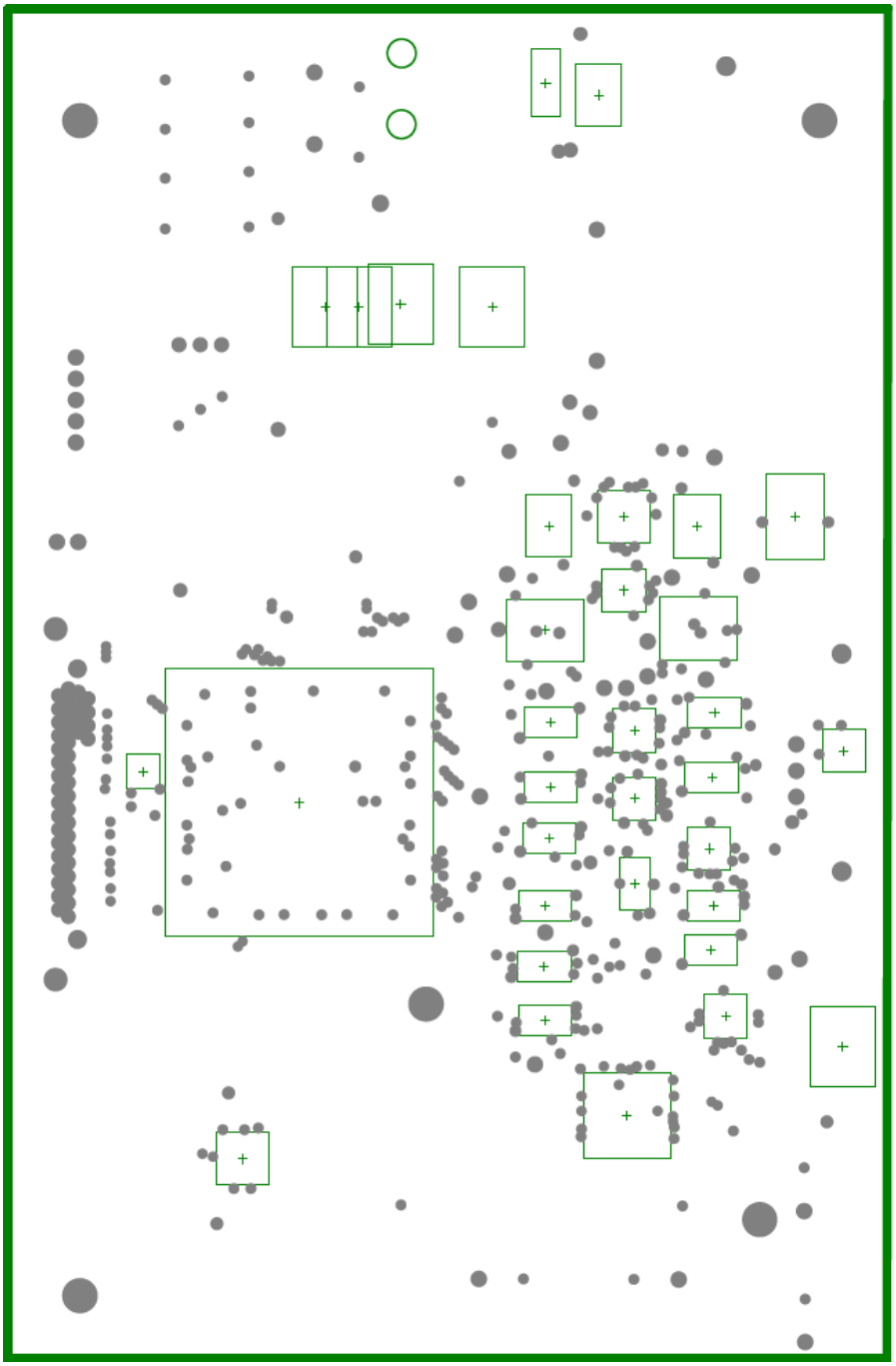


Figure 87: PCB Layout - Layer 2

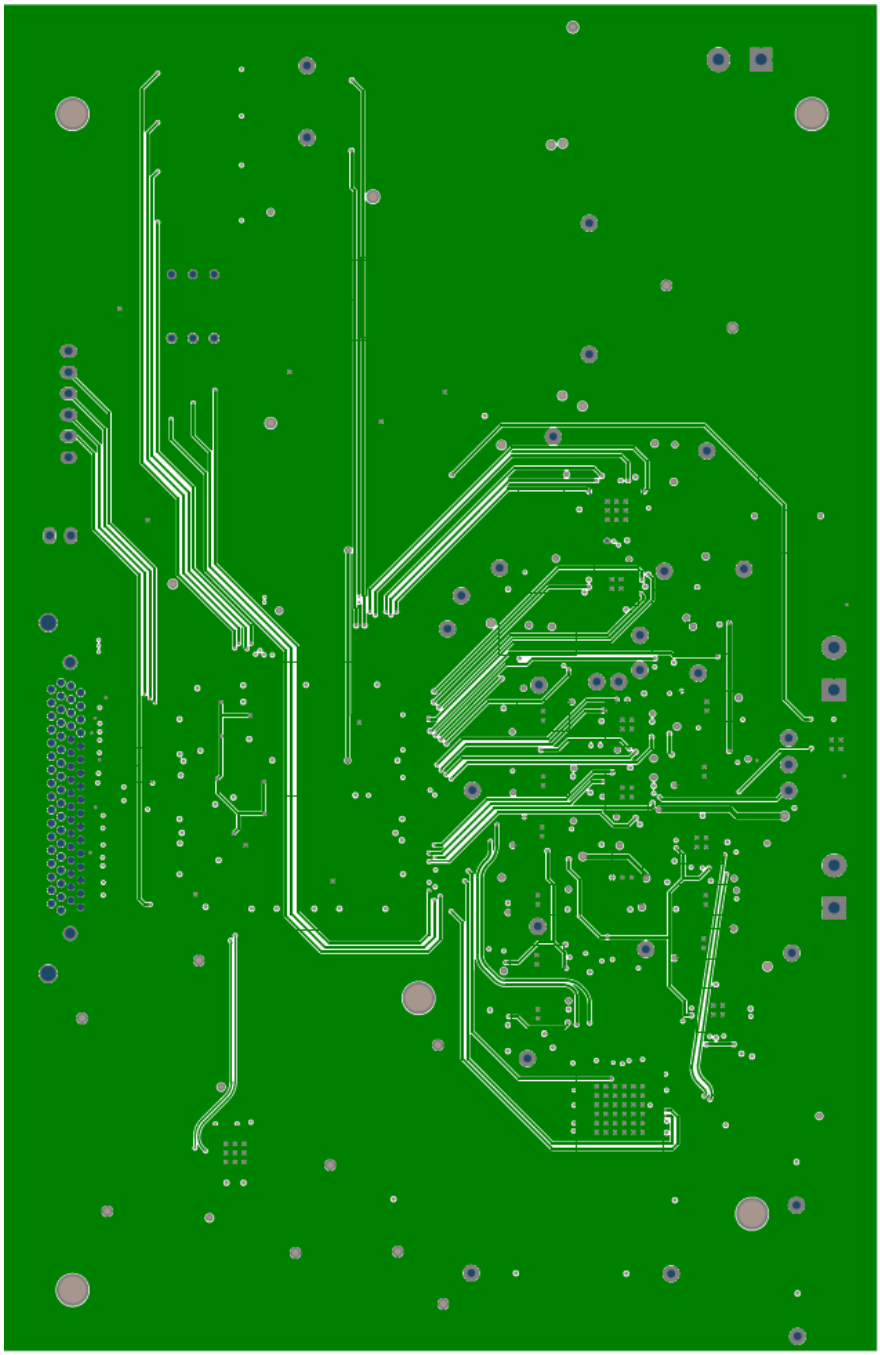


Figure 88: PCB Layout - Layer 3

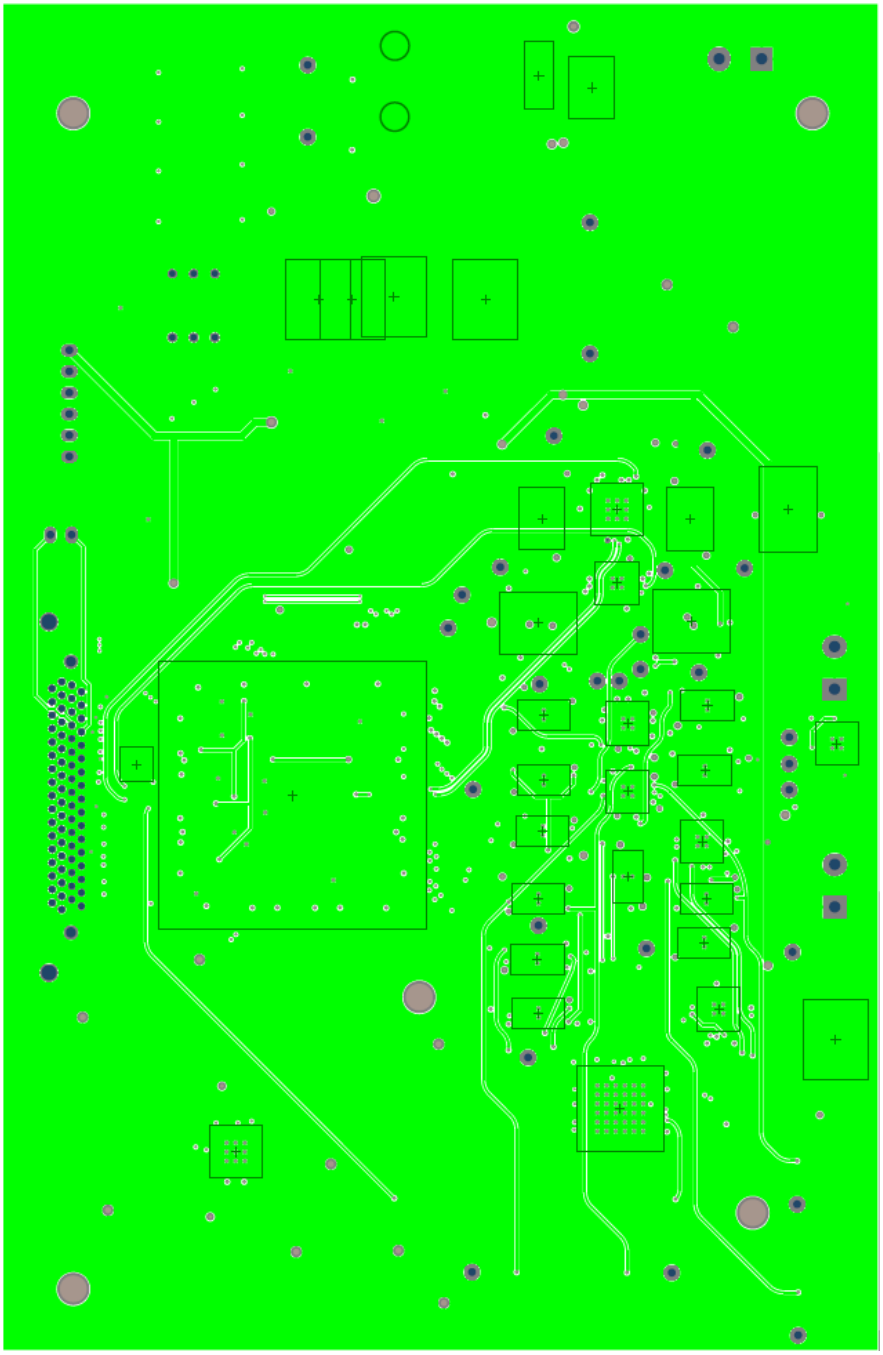


Figure 89: PCB Layout - Layer 4

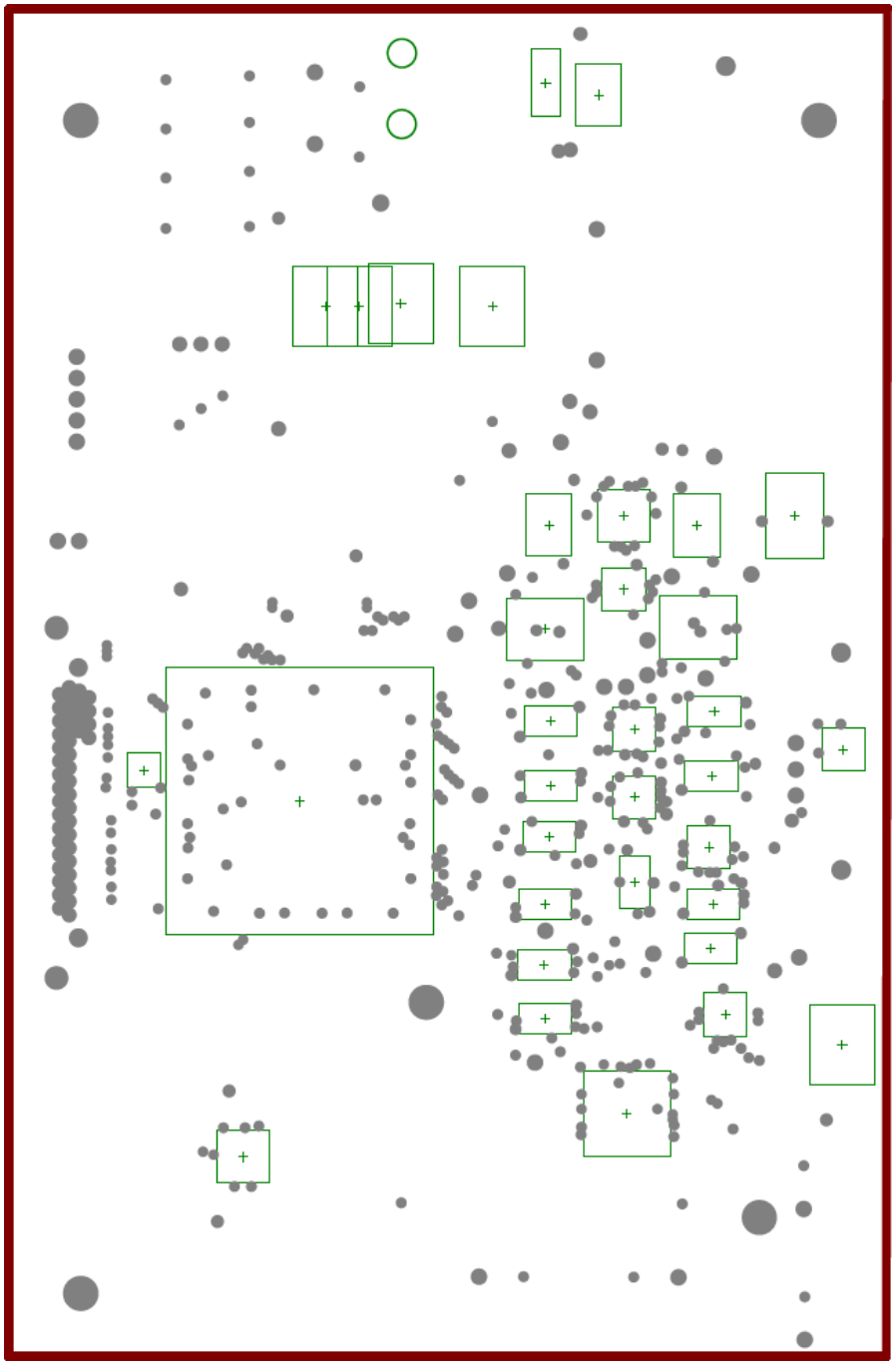


Figure 90: PCB Layout - Layer 5

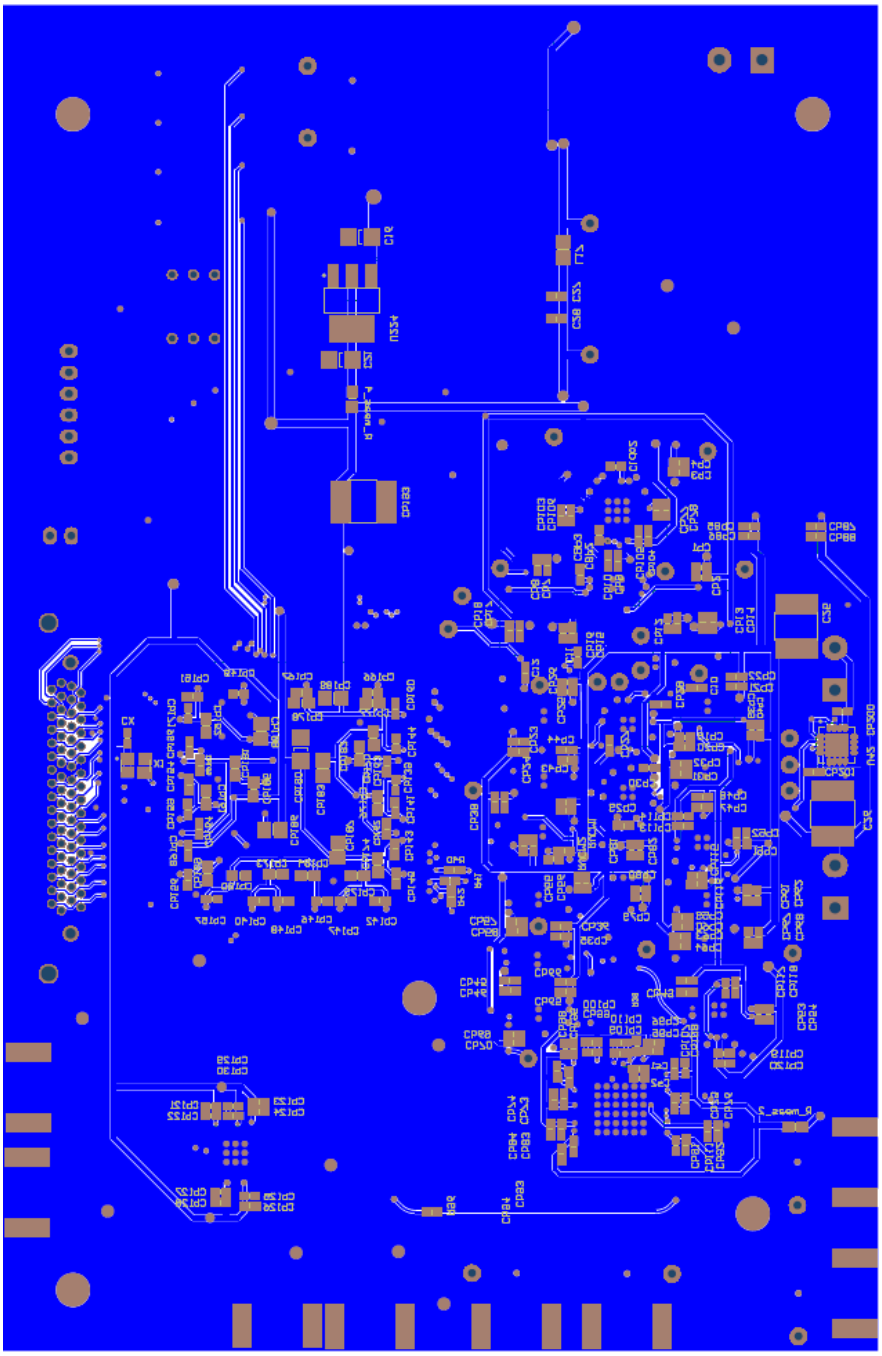


Figure 91: PCB Layout - Bottom Layer

B Bill Of Materials

Comment	Description	Designator	Footprint	LibRef	Quantity
4.7pF	Ceramic Chip Capacitor - C0G , X7R , 50V	C1, C2, C3, C4, C5, C6, C7, C8	cap0402	Capacitor	8
np	Ceramic Chip Capacitor - C0G , X7R , 50V	C9, C10, C11, C12, C71, Cf3, Cf6, Cf8, Cf15	cap0402	Capacitor	9
100nF	Ceramic Chip Capacitor - C0G , X7R , 50V	C13, C14, C15, C16, C17	cap1206	Capacitor	5
10uF	Ceramic Chip Capacitor - C0G , X7R , 50V	C18, C19, C20, C21, C22	cap1206	Capacitor	5
330uF	Ceramic Chip Capacitor - C0G , X7R , 50V	C23, C24, C25, C26, Cb192	2220	Capacitor	5
np	Ceramic Chip Capacitor - C0G , X7R , 50V	C27, C28	cap1206	Capacitor	2
0.1uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb1, Cb3, Cb5, Cb7, Cb9, Cb12, Cb13, Cb16,	cap0402	Capacitor	74
		Cb17, Cb19, Cb21, Cb23, Cb25, Cb27, Cb28,			
		Cb29, Cb30, Cb31, Cb33, Cb35, Cb37, Cb39,			
		Cb41, Cb43, Cb45, Cb47, Cb49, Cb51, Cb53,			
		Cb55, Cb57, Cb59, Cb61, Cb63, Cb65, Cb67,			
		Cb69, Cb71, Cb73, Cb75, Cb77, Cb79, Cb81,			
		Cb83, Cb85, Cb87, CCb200, Cb201, Cs1,			
		Cb89, Cb91, Cb93, Cb95, Cb97, Cb99, Cb103,			
		Cb105, Cb107, Cb109, Cb111, Cb113, Cb115,			
		Cb117, Cb119, Cb121, Cb123, Cb125, Cb127,			
		Cb129, Cb131, Cb133, Cb135, Cb137, Cb195,			
4.7uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb2, Cb4, Cb6, Cb8, Cb72, Cb74, Cb76, Cb78,	cap0402	Capacitor	21
		Cb84, Cb90, Cb92, Cb94, Cb96, Cb98, Cb100,			
		Cb104, Cb106, Cb108, Cb110, Cb198, Cb199			
10uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb10, Cb11, Cb14, Cb15, Cb18, Cb20, Cb22,	cap0402	Capacitor	44
		Cb24, Cb26, Cb32, Cb34, Cb36, Cb38, Cb40,			
		Cb42, Cb44, Cb46, Cb48, Cb50, Cb52, Cb54,			
		Cb56, Cb58, Cb60, Cb62, Cb64, Cb66, Cb68,			
		Cb70, Cb80, Cb82, Cb114, Cb116, Cb118,			
		Cb122, Cb124, Cb126, Cb128, Cb130, Cb132,			
		Cb134, Cb136, Cb138			
1uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb86, Cb88, Cs2	cap0402	Capacitor	3
0.047uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb139, Cb140, Cb141, Cb142, Cb143, Cb144,	cap0402	Capacitor	27
		Cb145, Cb146, Cb147, Cb148, Cb149, Cb150,			
		Cb151, Cb152, Cb153, Cb154, Cb156, Cb157,			
		Cb159, Cb160, Cb162, Cb163, Cb164, Cb165,			
		Cb166, Cb167, Cb196			
0.47uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb161, Cb169, Cb170, Cb171, Cb172, Cb173,	cap0603	Capacitor	17
		Cb174, Cb175, Cb176, Cb177, Cb178, Cb179,			
		Cb180, Cb181, Cb182, Cb184, Cb185			

Figure 92: Bill Of Materials - Part 1

0. 47uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb168	cap0402	Capacitor	1
4.7uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb183, Cb186, Cb187, Cb188, Cb189, Cb194	cap0805	Capacitor	6
330uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb190	cap1206	Capacitor	1
47uF	Ceramic Chip Capacitor - C0G , X7R , 50V	Cb193	2220	Capacitor	1
100nF	Ceramic Chip Capacitor - C0G , X7R , 50V	CBP2, CBP3, CIdo1, CIdo2	cap0402	Capacitor	4
10p	Ceramic Chip Capacitor - C0G , X7R , 50V	Cf1, Cf2, Cf4, Cf5, Cf7, Cf9, Cf14, Cf16	cap0402	Capacitor	8
10nF	Ceramic Chip Capacitor - C0G , X7R , 50V	CX	cap0402	Capacitor	1
47uF	Ceramic Chip Capacitor - C0G , X7R , 50V	C_INPUT, C_L	cap0805	Capacitor	2
LED2	Typical RED, GREEN, YELLOW, AMBER LED	D1, D2, D3, D4, D5, D6, D7, D8	3.2X1.6X1.1	LED2	8
MBRS130T3G	Surface Mount Schottky Diode	D9	Schottky Diode	MBRS130T3G	1
SMA	SMA Connector	IN_N, IN_P, OUT_N, OUT_P, P5, P6, P7, P8	SMA_H-RJ45 Flanged	SMA	8
np	68-Pin Connector	J1	68-Pin Connector	68-Pin Conn	1
np	Chip Inductor - Murata LQW Serie	L1, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, L12,	ind0402	Inductor	16
		L13, L14, L15, L16			
np	Chip Ferrite Bead - Standard	L17	ind0805	Ferrite Bead	1
68uH	Chip Inductor - Murata LQW Serie	L_dc	ind0805	Inductor	1
6V	KLEMME LEITERPL	P1	RCC-2	Klemme 2 pol	1
-12V	KLEMME LEITERPL	P2	RCC-2	Klemme 2 pol	1
12V	KLEMME LEITERPL	P3	RCC-2	Klemme 2 pol	1
Header 6	Header, 6-Pin	P4	HDR1X6	Header 6	1
Header, 2-Pin	Header, 2-Pin	P9	HDR1X2	Header 2	1
250	Chip Resistor - Dickschicht 50V, MC Serie	R1, R2, R3, R4, R031, R032, R33, R34	res0402	Resistor	8
1k2	Chip Resistor - Dickschicht 50V, MC Serie	R1_dc	res0603	Resistor	1
3k6	Chip Resistor - Dickschicht 50V, MC Serie	R2_dc	res0603	Resistor	1
100k	Chip Resistor - Dickschicht 50V, MC Serie	R5, R6, R7, R8	res0402	Resistor	4
10k	Chip Resistor - Dickschicht 50V, MC Serie	R9, R10, R11, R12, R13, R15, R16, R019,	res0402	Resistor	16
		R39, R59, R62, R65, R70, R96, R101, R102			
100	Chip Resistor - Dickschicht 50V, MC Serie	R14, R017, R46, R47, R48, R49, R53, R58,	res0402	Resistor	17
		R61, R64, R67, R68, R69, R72, R73, R75, R76			
11k	Chip Resistor - Dickschicht 50V, MC Serie	R17, R19, R21, R23	res0402	Resistor	4
1k	Chip Resistor - Dickschicht 50V, MC Serie	R18, R20, R22, R24, R60, R63, R66, R71	res0402	Resistor	8
180	Chip Resistor - Dickschicht 50V, MC Serie	R25, R26, R27, R28, R37, R38, R54, R55	res0402	Resistor	8
390	Chip Resistor - Dickschicht 50V, MC Serie	R29, R30, R31, R32, R35, R36, R56, R57	res0402	Resistor	8
6k2	Chip Resistor - Dickschicht 50V, MC Serie	R40	res0402	Resistor	1
620	Chip Resistor - Dickschicht 50V, MC Serie	R41, R42	res0402	Resistor	2
10	Chip Resistor - Dickschicht 50V, MC Serie	R77, RLED1, RLED2, RLED3, RLED4, RLED5,	res0402	Resistor	9
		RLED6, RLED7, RLED8			

Figure 93: Bill Of Materials - Part 2

220	Chip Resistor - Dickschicht 50V, MC Serie	R78	res0402	Resistor	1
50	Chip Resistor - Dickschicht 50V, MC Serie	R79, R80, R81, R82	res0402	Resistor	4
0	Chip Resistor - Dickschicht 50V, MC Serie	R83, R94, R95, R97, R98, R_dc, R_decouple2,	res0402	Resistor	11
		Rtest1, Rtest2, Rtest3, Rtest4			
0	Chip Resistor - Dickschicht 50V, MC Serie	R88	res0805	Resistor	1
np	Chip Resistor - Dickschicht 50V, MC Serie	R91, R99	res0402	Resistor	2
120	Chip Resistor - Dickschicht 50V, MC Serie	R100	res0603	Resistor	1
33	Chip Resistor - Dickschicht 50V, MC Serie	Rf1, Rf2, Rf3, Rf4, Rf5, Rf6, Rf7, Rf8, Rf9,	res0402	Resistor	16
		Rf10, Rf11, Rf12, Rf13, Rf14, Rf15, Rf152			
Resistor	Chip Resistor - Dickschicht 50V, MC Serie	Rpullup0, Rpullup1, Rpullup2,	res0402	Resistor	5
		Rpullup3, Rpullup4			
750	Chip Resistor - Dickschicht 50V, MC Serie	RVCM1	res0402	Resistor	1
6k8	Chip Resistor - Dickschicht 50V, MC Serie	RVCM2	res0402	Resistor	1
0	Chip Resistor - Dickschicht 50V, MC Serie	R_meas_1, R_meas_2, R_meas_3, R_meas_4,	res0603	Resistor	7
		R_meas_5, R_meas_6, Rlim			
DIP Switch 3	GRAYHILL - 76SB03T - SCHALTER, 3 POLIG	S1	DIP 3	DIP_SW_3	1
Switch SMD	Switch SMD Schurter 1301.9315	SW1, SW2	Schurter_Switch	Switch_SMD	2
TestPoint	Testpoint for Probing	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8,	HDR1X	TestPoint	29
		TP9, TP10, TP11, TP12, TP13, TP14, TP15,			
		TP16, TP17, TP18, TP19, TP20, TP21, TP22,			
		TP23, TP24, TP25, TP26, TP27, TP28, TP29			
AD9106	Quad, Low Power, 12-Bit, 180 MSPS, DAC	U1	LFCSP_WQ_32_round	AD9106	1
AD5668	Octal, 16-Bit SPI Voltage Output DAC	U2	LFCSP_WQ-16	AD5668	1
AD9257	Octal, 14-Bit, 40/65 MSPS, LVDS, 1.8 V ADC	U3	LFCSP - 64	AD9257	1
AD8002	Dual 600 MHz, 50 mW CFA	U4, U5	SOIC SO8	AD8002	2
THS4012	OP AMP DUAL 290MHZ	U20, U21, U30, U31, U32, U33, U34,	DGN (R-PDSO-G8)	THS4012	11
		U35, U36, U37, U70			
ADG1412	High Voltage - CMOS - Quad Switch	U40, U41, U42	LFCSP_VQ-16 Lead	ADG1412	3
AD8182	2:1 MUX; 10 ns Switching Time	U50, U51	SOIC - R-14	AD8182	2
ADA4938-2	Ultralow Distortion Differential ADC Driver	U60, U61	LFCSP_VQ-24	ADA4938-2	2
AD8024	Quad 350 MHz Current Feedback Amplifier	U80	SOIC16N	AD8024	1
DS90LV804	4-Channel 800 Mbps LVDS Buffer/Repeater	U90	WQFN 32 Lead	DS90LV804	1
XC3S200	Spartan-3 FPGA, 141 User I/Os, 208-Pin	U100	PQ208_N	XC3S200	1
ADP1111	Step-Up/Step-Down Regulator	U110	SOIC SO8	ADP1111	1
LD1117	Voltage Regulator, LDO 5V, SMD	U221, U222, U223, U224, U225	SOT-223-DB3_M	LD1117	5
Value	Oscillator - 4 pin	X1	Crystall 4 Port	Oscillator	1

Figure 94: Bill Of Materials - Part 3

C Shortcuts

Shortcut	Description
ADC	analog to digital converter
CV Stage	current to voltage stage
DAC	digital to analog converter
DCM	digital clock manager
Diff Stage	differential stage
FPGA	field programmable gate array
LVDS	low voltage differential signal
MUX	multiplexer
SPI	serial peripheral interface

Figure 95: Shortcuts