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Investigation on Resistive Switching of Metal-Organic-Metal Thin Film Devices

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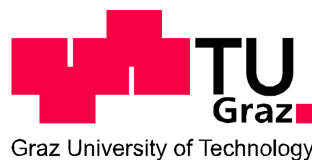

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Abstract

Memory is one of the most basic and most important components in the age of ubiquitous computing. The performance of memory technology has been continuously increased over the past decades by downscaling the physical dimensions of its constitutive components, namely capacitors and transistors. Downscaling has led to a doubling of the integration density roughly every 18 months, an observation that is known as Moore's law.

Approaching the fundamental lower limit of electronic circuitry has kindled research into next generation's memory technology. A promising class of emerging research device are resistive switches. They are known to be fast, non-volatile and can be integrated as two-terminal devices in high-density crossbar arrays. Using organic dielectric and semiconducting material has produced very reliable high-performance memory cells, however the poor understanding of the fundamental switching mechanism has hampered further development.

In this light a set of experimental data is presented that reveals clear evidence that the resistive switching effect in metal/organic/metal devices is based on the formation and rupture of filaments. The process of filament formation and resistive switching is illustrated by time-of-flight secondary-ion mass spectroscopy. The simple device structure suggests that this mechanism is solely accountable for unipolar resistive switching in a wide class of devices with equivalent structure, ruling out a variety of previously proposed theories.

To substantiate the switching theory the influence of the reactive species oxygen and water on the switching behaviour is studied. Alternative fabrication methods are developed to demonstrate that switching is largely independent from fabrication. By the fabrication of nano-sized memory cells the potential for downscaling is explored.

Kurzfassung

Computer sind in der heutigen Zeit beinahe allgegenwärtig. Das Speichersystem eines Computers ist ein kritisches Element, welches die Performance maßgeblich beeinflusst. Die derzeit verwendete Speichertechnologie vertraut auf kontinuierliche Miniaturisierung zur Leistungssteigerung. Das führte dazu, dass bisher etwa alle 2 Jahre eine Verdoppelung der Integrationsdichte in integrierten Schaltungen beobachtet wurde, ein Zusammenhang, der auch als das Moor'sche Gesetzt bekannt ist. Die Größenordnungen, die notwendig wären um diesen Trend über 2020 hinaus aufrecht zu erhalten liegen jedoch in einem Bereich, in dem quantenmechanische Prozesse zu dominieren beginnen.

Daher wird seit Jahren intensiv an neuen Speichertechnologien geforscht. Eine sehr vielversprechende Klasse innerhalb einer Vielzahl von in Frage kommenden Systemen sind sogenannte resistive Speicher (resistive switches). Diese haben hohe Schaltgeschwindigkeiten, sind nichtflüchtig und können als Passiv-Matrix hoher Speicherdichte integriert werden.

Die Verwendung von organischen Halbleitern und Isolatoren hat bereits hoch-performante Speicher hervorgebracht. Jedoch fehlt bisher ein umfassendes und fundiertes Modell um den eigentlichen Schaltvorgang zwischen hoch-leitfähigem und isolierendem Zustand zu beschreiben.

In dieser Arbeit wird eine Reihe von Experimenten vorgestellt, anhand derer der Schaltvorgang in Metall/Isolator/Metall Dünnschichtbauelemente eindeutig der Formierung und teilweise Auflösung von metallischen Brücken, sogenannte Filamente, zugeschrieben werden kann. Die einzelnen Zustände werden anhand von Flugzeit Sekundärionen Massenspektroskopie untersucht. Der prototypische Charakter des Referenzdesigns ermöglicht es, diesen Schaltmechanismus auf eine breite Klasse von äquivalenten organischen schaltbaren Widerständen anzuwenden.

Durch alternative Fabrikationsmethoden wird gezeigt, dass der Schaltmechanismus eine intrinsische Eigenschaft von Metall/Isolator/Metall Dünnschichtbauelementen ist und nicht maßgeblich durch die Fabrikationsmethode beeinflusst wird. In diesem Licht wird auch die Stabilität der Speicher unter Sauerstoff und Wasserdampf untersucht. Die Speicher wurden zudem in Nanometerskalen gefertigt und charakterisiert um das Miniaturisierungspotential dieser Technologie zu untersuchen.

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1 Introduction

We live in an age of ubiquitous computing. Computers have interfused almost every aspect of our life and have to some extend evolved from primitive calculators to connected entities forming a global network – the internet.

The success of modern computers was aided by what is now known as Moore's law[1] describing the doubling of the number of transistors in an integrated circuit at approximately the same cost and size every two years. It has not only served as a keen observation of the past but furthermore acted as a driving force for industry and research to come up with new ideas to fabricate memory and logic in the sizes demanded by Moore's Law.

Owing to the complexity of today's circuits downsizing is not always a straight-forward process. As long as the work-horse of lithography is the 193 nm wavelength excimer laser there are physical limits to the smallest feature size that can be obtained. The follow-up technologies extreme ultra-violet (EUV) and electron beam (e-beam) are not ready in an industrial scale[2] and companies still rely on refined methods like double patterning[3] to reach the next generation of critical dimension. The end of Moore's Law has been predicted in regular intervals, but in a collective effort scientists and engineers have continuously kept on schedule with downsizing integrated circuits. However, a slow-down of miniaturization can be observed at the current stage[4].

The international technology roadmap for semiconductors (ITRS) has outlined two strategies named "More than Moore" and "More Moore" in 2010 to sustain the success story of integrated circuit development.

More-than-Moore (MTM) represents a diversification approach, where, for example, micromechanical machines, sensors or actuators or microfluidic devices are implemented on a chip without, per se, increasing packing density but instead adding new functionality[5]. In this sense MTM is not competing with the miniaturization trend of Moore's law. Instead a heterogeneous integration of digital and non-digital functionalities might create a new industrial trend that is independent from and not hampered by the physical limits of Moore's law.

In contrast *More Moore* (MM) aims to extend the life-time of established CMOS technology by exploring new implementations, e.g. materials or 3-D stacking[6]. One especially intriguing aspect is the implementation of analogue memory units in digital circuits that have worked on Boolean logic, i.e. with states represented by "0" (OFF) and "1" (ON). We can envision, for

example, a new kind of memory that stores not two but more logic states (so called multi-bit cells). For ten states at the same size such a kind of memory would represent a significant increase in memory density without the limitations imposed by Moore's Law.

It has been further realized that much of the advantages that a brain possesses over binary logic stems from its analogue character and a switching behaviour that has been termed "all or nothing threshold switching" or spiking behaviour[7] of neurons. In the late 70s of the 20th century it was discovered that this switching behaviour can be realized by the means of a fourth basic, passive, non-linear two-terminal electrical circuit element: the memristor[8,9].

The development of the actual working memristive devices turned out to be a greater challenge than expected and it took over 40 years until the connection between non-volatile resistive switching metal/insulator/metal (MIM) thin-film devices and the memristor was established[10].

In recent years this particular class of memristive devices have increasingly gained attention from both, the scientific community and industry alike. The current focus of research lies on the application of resistive switching devices in memory where Moore's law might soon limit the advance in currently established memory technology and new materials, methods and devices are in dire need.

After over four decades the physics that drive resistive switching in MIM devices is still poorly understood and hampers technological progress in this area.

The aim of this work is to contribute to the understanding of the switching mechanism in metal/insulator/metal devices, where it will focus on devices with organic insulating (and semiconducting) materials.

The **second chapter** lays out the current standing of the memory landscape as well as introduce promising candidates for next generation memory. For established memory technologies the functional principles are explained to understand their specific advantages and drawbacks.

The **third chapter** introduces the concept of a unified memory and storage device. It focuses prototypical and emerging memory technologies which, in theory, are capable to replace current technology. In the **fourth chapter** the use of organic insulating materials in resistive memory is introduced as a promising material class. Its structure and working principles as well as performance related figures of merit are presented by means of a reference device in **chapter five**. The switching mechanism will be investigated in detail by means of time-of-flight

secondary ion mass spectroscopy, impedance spectroscopy, electrical characterization and by studying the influence of the reactive gasses oxygen and water vapour on the switching. In **chapter six** and **seven** two alternative fabrication methods, namely metal transfer printing and lamination are presented to study the influence of the fabrication route on the memory's properties. In **chapter eight** the use of a flexible, lightweight and ultra-thin substrate is demonstrated. **Chapter nine** explores the potential for downsizing and nanometre-scale memory elements are fabricated and characterized. In the final **chapter ten** the work is summarized and a conclusion is drawn.

2 Current Memory Architecture

In today's computer architecture four distinctively different memory technologies are usually implemented in a system. They can be roughly divided into memory and storage as is schematically displayed in figure 2.1. Memory is volatile, i.e. it loses its memory state when external power is switched off. Memory is usually associated with random access, meaning that each cell (bit) can be addressed in random order. This class contains static random access memory (SRAM) and dynamic RAM (DRAM).

Storage is non-volatile and sustains its memory state without external power supply, in an ideal case infinitely. The most common technology in this class is FLASH.

For storage of big amounts of data hard-disk drives are usually employed as they feature high data capacity at low cost but suffer from relatively low speed.

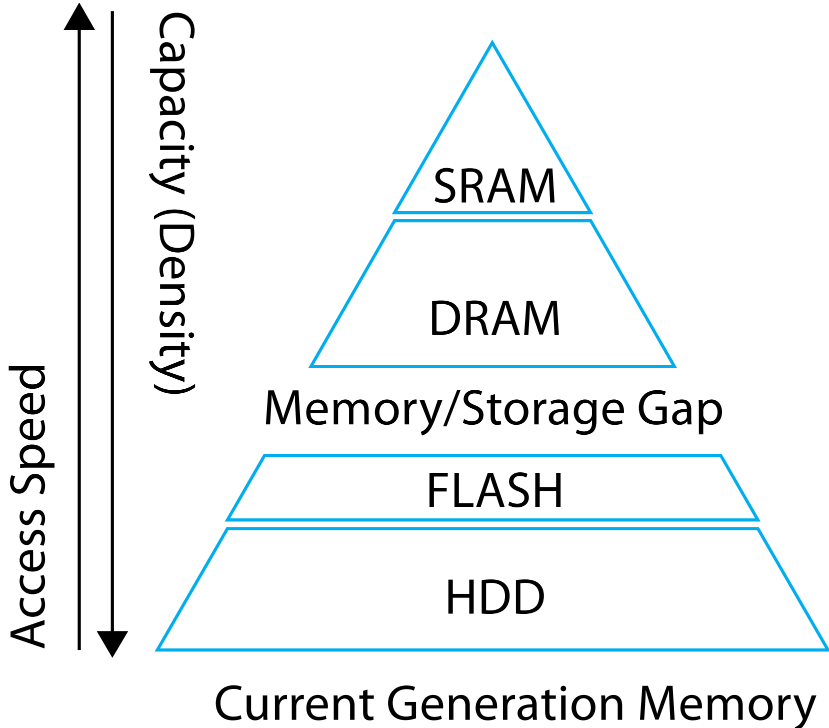


Figure 2.1 A schematic of current memory/storage segmentation. SRAM and DRAM is usually employed where fast switching speed is necessary and limited memory capacity and volatile behaviour are acceptable, e.g. the fast cache in a computer. FLASH and HDD form the non-volatile storage segment. They offer considerably higher capacity but are slow in comparison to SRAM and DRAM.

2.1 Static Random Access Memory

In static random access memory (SRAM) data storage is achieved using a bistable latch also called a flip-flop where each state of the latch represents either “1” or “0”. It is temporarily stable (i.e. does not need periodical refreshing) but it still volatile as data is lost without external power supply. A typical (“stand alone”) SRAM usually consists of 6 transistors. The high number of transistors limits the integration density of SRAM however it is, generally speaking, the fastest memory. A schematic showing the flip-flop and access transistors is shown in figure 2.2.

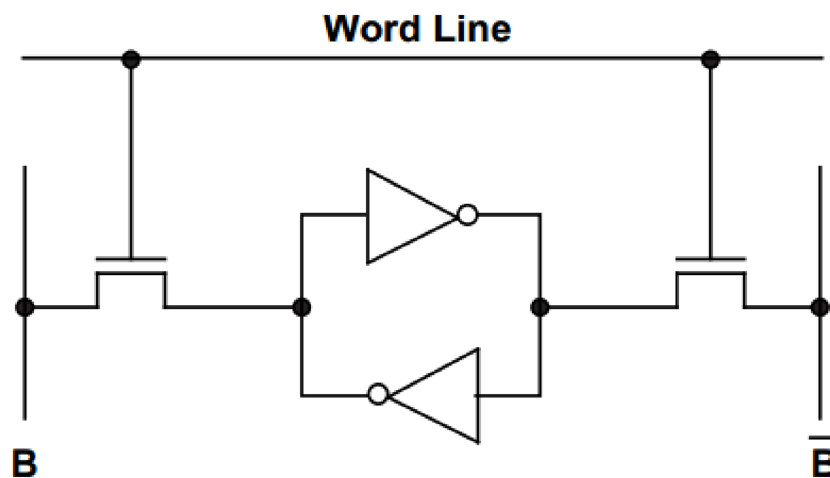


Figure 2.2 Schematic of an SRAM cell, represented by a bistable latch ("flip-flop"), two access transistors and the principal external connection by bitlines (B,$\overline{B}$) and the word-line. The memory states are formed by the two stable states of the centre flip-flop. The complex structure is a drawback as it limits the integration density of SRAM. Taken from[11]

2.2 Dynamic Random Access Memory

In dynamic RAM data is stored in a capacitor, where charged and discharged state represent 1 and 0, respectively. Compared to SRAM, where the memory state is temporarily maintained by bistable latches, DRAM needs periodical refreshes to keep the capacitor charged due to leakage in form of sub-threshold current of the transistor or to the oxide. Since only one storage capacitor and one access transistor are necessary for a DRAM cell (figure 2.3) the density is significantly higher than SRAM.

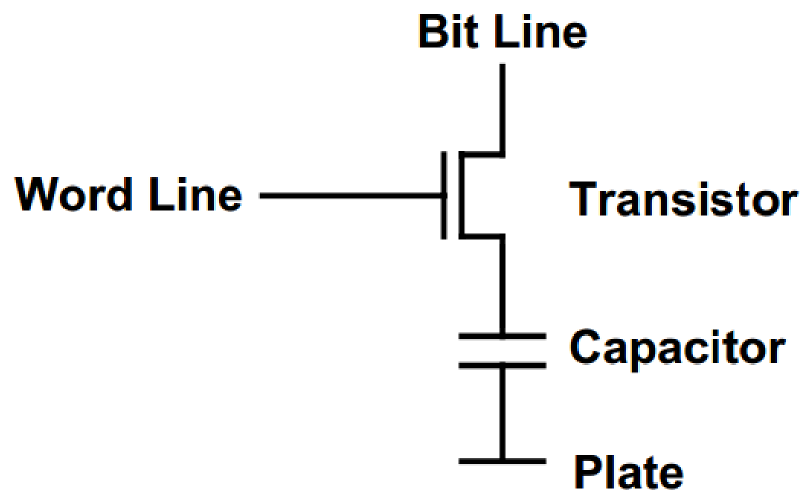


Figure 2.3 Schematic of a DRAM cell. The data is stored in form of a charge on the capacitor ("1" charged, "0" uncharged state). Due to constant leakage of the stored charge DRAM requires periodical refresh. As can be expected from the simple structure of the cell integration density of DRAM is high. Taken from[12]

Periodical refresh and the required external circuitry limit the speed of DRAM which is considerably slower than SRAM.

2.3 FLASH

FLASH is implemented in storage devices. A FLASH cell is a transistor with an additional, isolated gate, called floating gate (figure 2.4). In FLASH memory the bit information is stored in form of charges on the floating gate that change the threshold voltage of the FET channel. This shift is interpreted as "1" or "0". Electrons are placed in the floating gate via tunnelling from the source-drain channel ("hot injection") or the control gate ("cold injection") and remain there for some time (retention time is expected to be at least years).

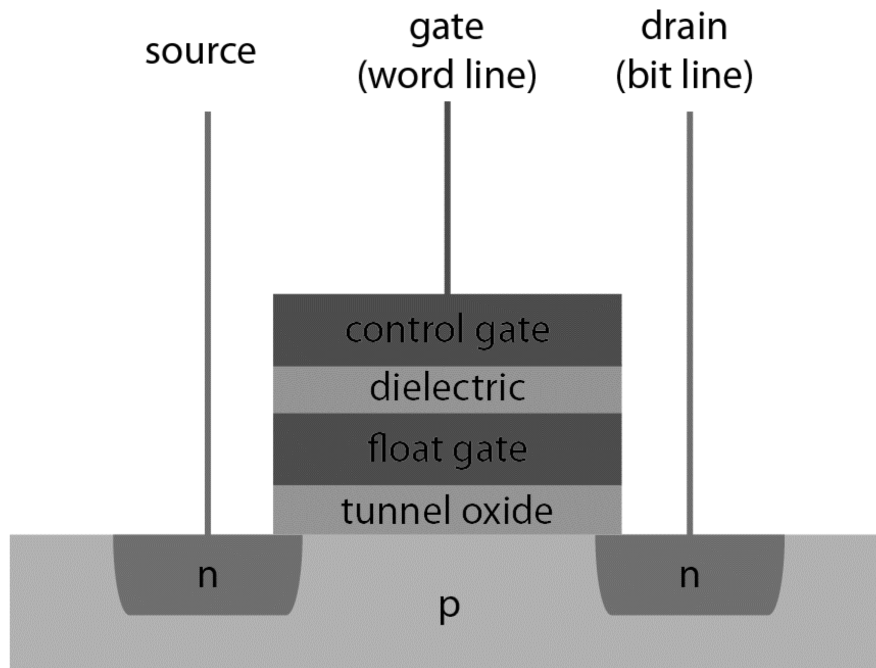


Figure 2.4 Schematic cross-section of a FLASH memory cell. The cell basically forms a CMOS transistor with an additional, isolated, floating gate. Charge stored in this floating gate partially shield the electric field from the control gate, resulting in a shift in the threshold voltage for the transistor. This shift represents the binary states "0" and "1". Adapted from[13]

One significant disadvantage of FLASH is the limited amount of write/read cycles due to gate oxide stress induced by the high voltages necessary for write operation leading to program disturb or oxide defects[14].

2.4 Hard Disk Drive

Nowadays hard disk drives (HDD) are the most common storage system. A HDD uses rotating magnetic disks as storage media and data is written and read sequentially by a magnetic head. HDD offer a high density per area by utilizing quantum mechanical tunnelling, namely the giant magnetoresistance (GMR) and tunnel magnetoresistance (TMR) effect[15]. The tunnel current through a thin non-magnetic layer is a function of the relative orientation of the ferromagnetic layers. This can be understood by means of a so-called spin-valve depicted in figure 2.5. A ferromagnetic layer (FM) with pinned polarization and a FM with variable direction of polarization are separated by a non-magnetic isolator (TMR) or non-ferromagnetic metal

(GMR). The tunnelling current now depends on the relative orientation of the two layers. In case of parallel orientation of the two FM layers the tunnel current is high, in case of antiparallel orientation the current is significantly reduced. Utilizing this effect has drastically increased the storage area density that approaches $2*10^3$ Gigabits per square inch[16].

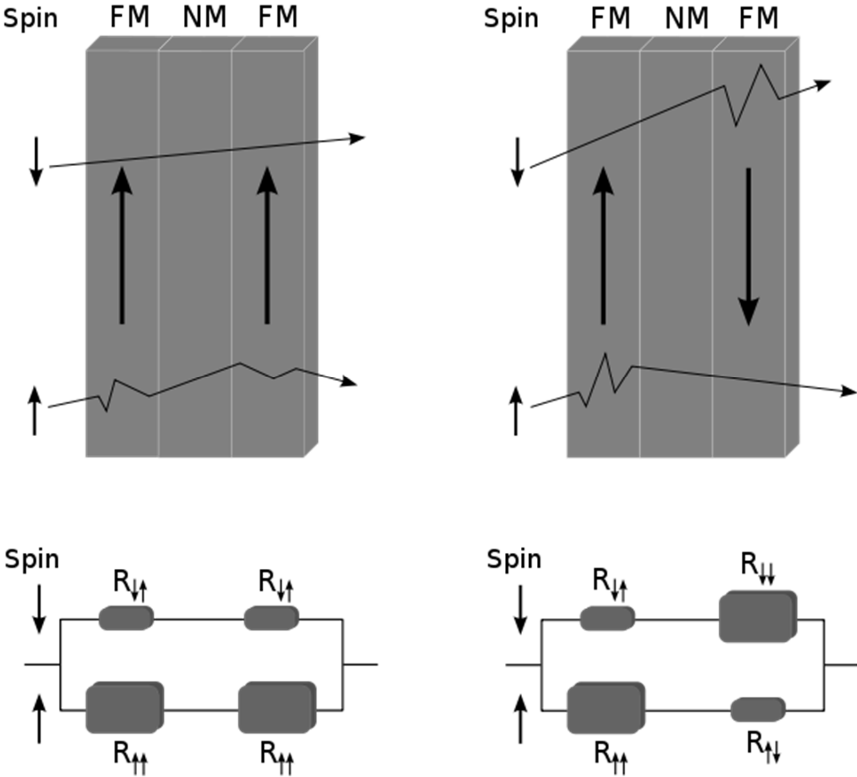


Figure 2.5 Schematic explanation of the GMR effect on the basis of spin-dependent scattering of electrons depending on the relative magnetization of two ferromagnetic layer (FM). The tunnel current through the non-magnetic layer (NM) is interpreted as states “0” and “1”. Taken from[17]

As a mature technology the HDD features high data density, long retention and other features, e.g. the unpatterned bits that offer a tremendous cost advantage. As such the bits are sub-lithographic[18].

HDD also has significant drawbacks as it features mechanical components to rotate the disk and position the head for read and write operation. All mechanical components are prone to failure, the mean time before failure of a modern HDD is around 1.2 million hours[19].

2.5 Figures of Merit for Current Memory and Storage Technology

The above presented memory and storage devices present mature technologies and a billion dollar market[20]. Since all presented memory technologies rely on downsizing to increase its performance it is expected that they will face serious issues with the end of Moore's law approaching[21]. Given a fabrication process the smallest feature size obtainable is denoted F. The area footprint of a device is then expressed in multiples of F^2, where smaller values of F^2 mean a higher area density.

Any technology that hopes to replace current memory technology, so-called next generation memory (NGM), will be evaluated under that aspect. In order to lay out the performance parameters expected for next generation memory the current generation's figure of merit are summarized in the following table 1. The best-in-class features are summarized in the last column as target for NGM.

Table 1 Figures of merit for currently commercialized memory technology. Best-in-class values are in italics and summarized in the last column as expected performance features of next generation memory. Adapted from[22]

	SRAM	**DRAM**	**FLASH**	**HDD**	**NGM**
Footprint (F^2)	140	6-12	*1-4*	2/3	**1-4**[1]
Energy per bit written (pJ)	$5x10^{-4}$	$5x10^{-3}$	*$2x10^{-5}$*	$1\text{-}10x10^{9}$	**$2x10^{-5}$**
Read time (ns)	*10^{-1}*	10^{1}	10^{5}	$5\text{-}8x10^{6}$	***10^{-1}***
Write time (ns)	*10^{-1}*	10^{1}	10^{5}	$5\text{-}8x10^{6}$	***10^{-1}***
Retention	As long as voltage applied	ms	*Years*	Years	**Years**
Endurance cycles	*$>10^{16}$*	$>10^{16}$	10^{4}	10^{4}	**$>10^{16}$**

[1] numbers smaller than 4 represent multi-bit ability, i.e. a single cell can represent more than two memory states.

3 Storage Class Memory

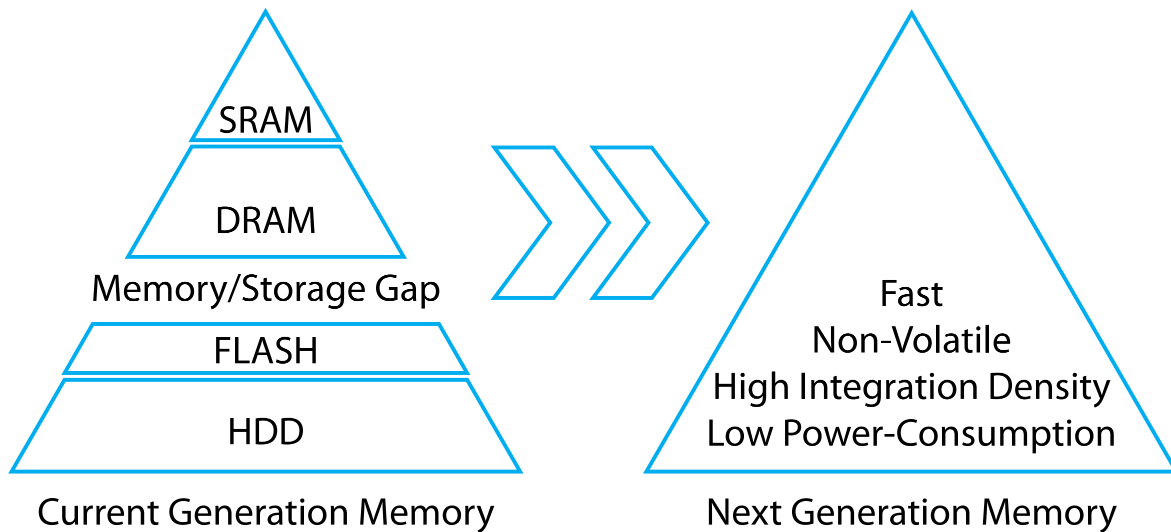


Figure 3.1 Transition from current memory and storage segmented architecture to a unified storage class memory utilizing next generation memory

Traditionally there has been a technological gap between memory and storage in digital systems (refer to figure 3.1). Whereas first aim for high write/read/erase speed the second one emphasizes density. For NGM expected performance parameters are outlined in the last column of table 1.

Combining the best of these features in one class of device is the driving force behind storage class memory (SCM). SCM need to be, for obvious reasons, non-volatile. Random access, i.e. addressing, reading and writing on bite level ("per cell") is a requirement. Cross-bar arrays are generally believed to be the most promising architecture to achieve high density ($4F^2$) and random access[23]. Ideally SCM is as fast as SRAM under write/read/erase operation and offer a density as high as magnetic storage platter used in hard-disk drives at similar price ranges (HDD, 826 gigabits per square inch[24], <$0.05 per gigabyte[25]). Current implementations of solid-state disk drives based on FLASH (SSD, 550 Gb per square inch[26], >$0.3 per gigabyte (as of 2014)) are an attempt to reach this goal, but they face serious issues of limited density, limited number of write cycles and other limitations[27]. It has been hinted that a number of prototypical and emerging research devices (ERD) might be suitable for SCM[28].

3.1 Prototypical and Emerging Research Devices

Prototypical devices refers to memory systems that have been, in principle, demonstrated but are not yet fully commercialized. Emerging research devices are at an even earlier stage. They have been successfully demonstrated on a lab scale but are not yet commercialized.

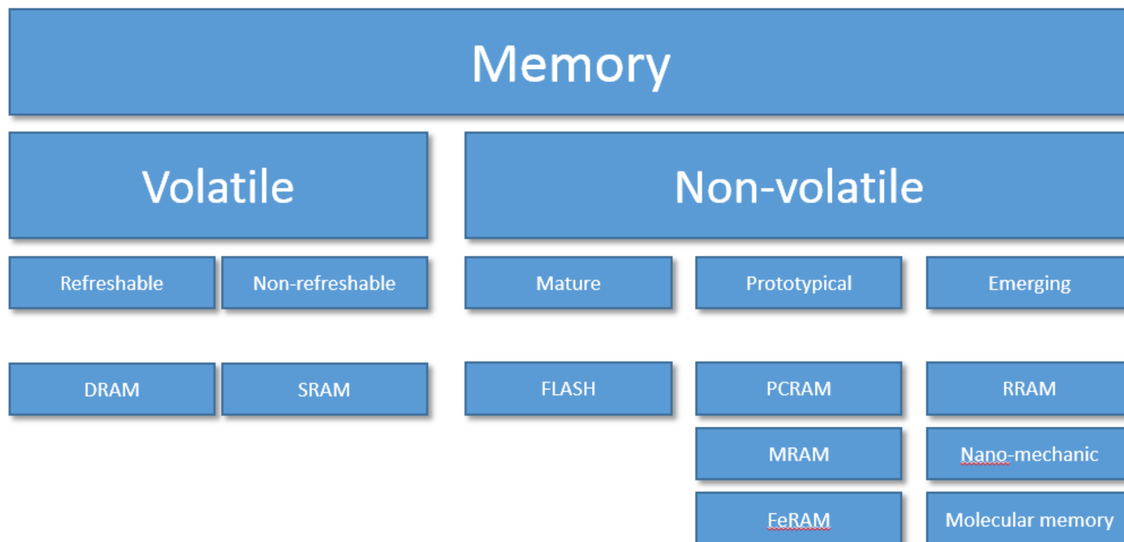


Figure 3.2 Classification of present, current and emerging memory technologies. This tree is an attempt to organize memory technology into already commercialized (mature), commercialized at an early stage (prototypical) and not yet commercialized (emerging) classes. Adapted from[29]

A closer look at figure 3.2 reveals a manifold of memory technologies currently under development. As the memory technology landscape is rapidly shifting some devices might already be implemented in consumer technology at a small scale.

3.2 Phase Change Memory

In a phase change memory (PCM), also referred to as ovonic unified memory, the resistance contrast between a high-resistance amorphous and a low-resistance crystalline phase of a material, e.g. chalcogenide glasses, is used to represent the memory states “1” and “0”. This is, basically, the same working principle and materials used in compact disks (CD), where the different optical properties of the amorphous (low reflectivity) and crystalline (high reflectivity) phases are used. The writing is achieved by suitable current pulses and Joule heating of a small volume of the material. The set operation (high-resistance to low-resistance) is facilitated by

heating the chalcogenide film above its crystallization temperature and then slowly cooled down to enhance crystallization. For reset operation the film is heated above melting temperature and then quenched to remain in an amorphous state. The high currents necessary for reset are a limiting factor for the integration of PCM in larger scales. PCM has already been commercialized to some extent as RAM for mobile devices[30,31], but recently the market situation has shown a trend towards stacked 3D FLASH over PCM[32].

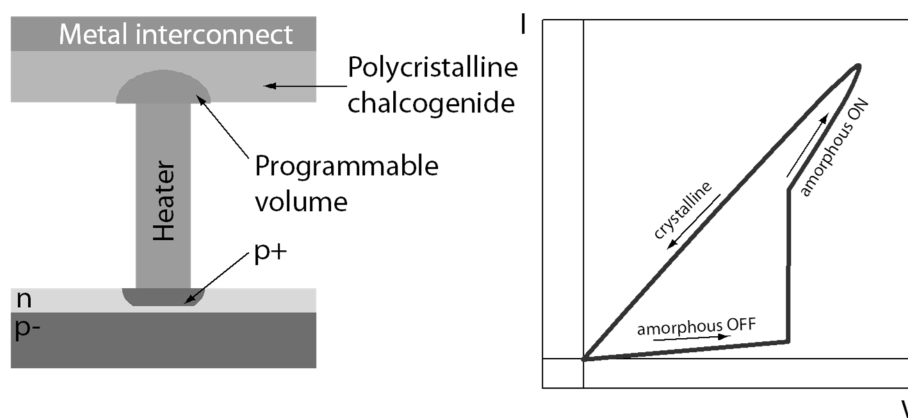


Figure 3.3 left-hand side: schematic layout of a PCM cell. Only a small volume exhibits phase change during memory operation. The series resistance of the cell can be changed by switching between amorphous (high resistance) and crystalline (low resistance) phase of the chalcogenide glass. Right-hand side: I-V characteristics of a PCM. The hysteresis shows two distinct memory states. Adapted from[33,34,35]

3.3 Magnetoresistive Memory

In a magnetoresistive memory the difference in resistance forming the memory states “1” and “0” arises from the tunnelling magnetoresistance effect (TMR). The memory cell is formed by a thin dielectric layer sandwiched between a ferromagnetic layer with permanent (pinned) direction of magnetisation and a ferromagnetic layer whose polarization direction can be switched from parallel to antiparallel with respect to the pinned layer during read and write operation. When the electron tunnels its spin is conserved. As such the tunnelling current is a function of density of states (DOS) and the DOS differ for parallel and antiparallel orientation of the magnetic layers, schematically displayed in figure 3.4.

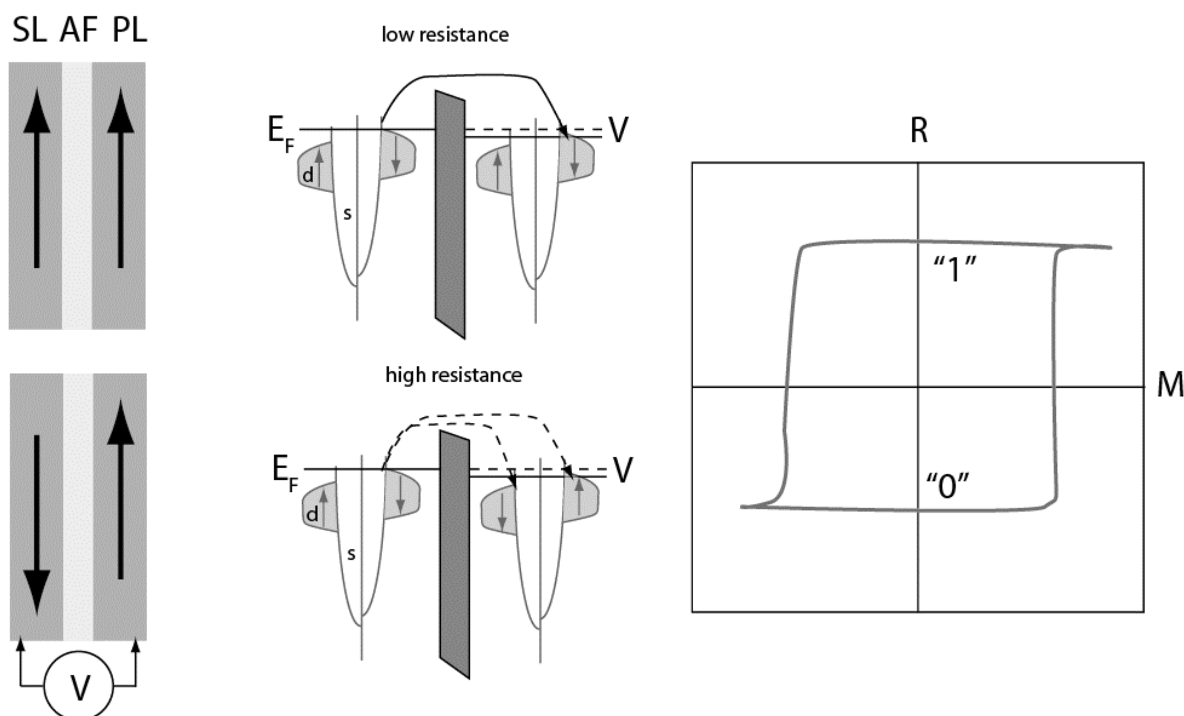


Figure 3.4 Working principle of magnetoresistive RAM on the basis of density of state (DOS)-dependent tunneling current between two ferromagnetic layers (SL, PL) separated by an antiferromagnetic (AF) spacer (left side). In ferromagnetic materials (Ni, Fe, Co) majority band (spin-down) has a higher DOS at the Fermi-surface (center). Right-hand side: in case of parallel magnetized layers the tunnelling current is high resulting in a low resistance ("1"). If during write operation the magnetization is changed to antiparallel the cell will exhibit a high resistance ("0"). Adapted from[36,37]

3.4 Ferroelectric Memory

In ferroelectric memory the memory states are stored in form of remnant polarization of a ferroelectric material (e.g. lead zirconate titanate) as schematically explained in figure 3.5. In practical use FeRAMs have a cell structure similar to DRAM, e.g. one transistor one capacitor (transistor type cell, not shown).

For writing operation a positive or negative voltage is applied across the cell capacitor resulting in an according polarization. Data retention of this type of device is known to be limited due to the limited retention of remnant polarization and ferroelectric RAM (FeRAM) needs to be periodically refreshed, similar to DRAM[38]. To read the stored data of a cell it is switched to the "0" state. If the previous state had been "1" a flow of charges, i.e. a current pulse, is detected. If the previous state had been "0" no charges will flow. A read changes the state of the memory thus requiring a refresh of the cell.

Compared to FLASH they feature a significantly lower power consumption and voltage levels as well as higher read/write speeds[39].

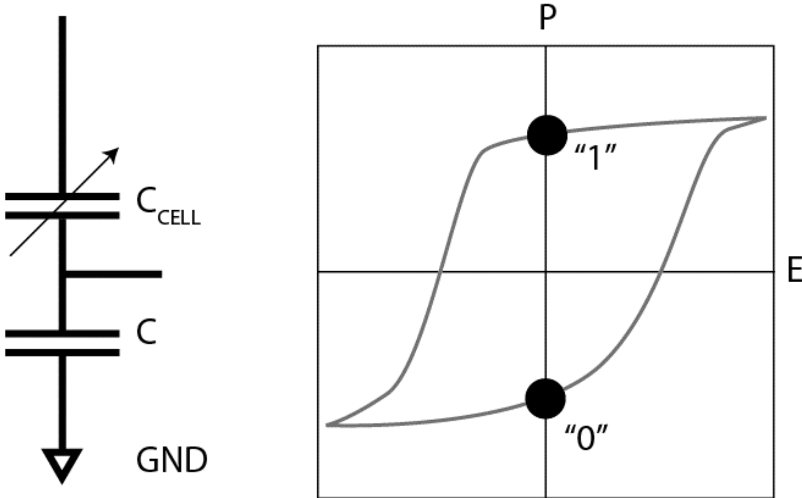


Figure 3.5 Left side: schematic of a ferroelectric memory cell. The memory states are represented by different remnant polarizations, as represented schematically on the right-hand side. Adapted from[40]

Ferroelectric memory is still a niche market but applied in a variety of products, e.g. Texas Instruments incorporates FeRAM in microcontrollers for low-power applications[41].

3.5 Nano-Mechanic Memory

The nano-mechanic memory is a storage concept where the data is stored in forms of nano-sized pits in a polymer layer. It is, in some sense, similar to punch-cards that served as mechanical storage units in the early years of the computing age[42]. Write and readout of the data is facilitated by micro-electromechanical systems (MEMS), similar to the probe of an atomic force microscope. For readout the probe tip is heated and moved into the proximity of the pixel. If the cantilever enters a pit the contact area and the heat flow from the probe is increased compared to the flat surface. This difference in temperature transfers to a difference of electrical resistance and assigned the memory states "0", "1".

For writing the tip is heated above the glass transition temperature of the storage media and the tip causes a dent in the softened polymer upon touching. To erase the bit the hot tip is slowly pulled away, surface tension will follow the tip removing the pit. Refer to figure 3.6 for operation modes.

The whole system is highly sophisticated from a micro-mechanical standpoint of view and the commercialization (IBM: millipede storage[43]) is slow although it offers promising data density.

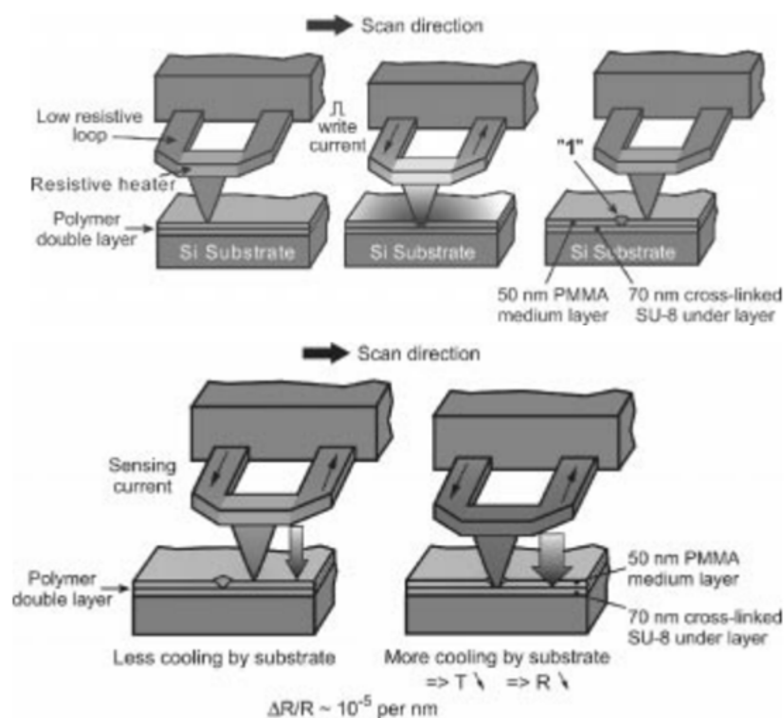


Figure 3.6 Upper half: writing operation of nano-mechanical storage system. The heated cantilever writes a bit by creating a dent in the PMMA layer. Bottom half: read operation based on thermal sensing. Taken from[44]

3.6 Molecular Memory

In molecular memory the data is stored in some inherent characteristic of a molecule. Owing to the ambiguous nature of this concept it is hard to draw a border to other memory systems, as molecular characteristics play a role in almost every memory concept. However some storage mechanism bear strong resemblance to a specific molecular quality and are thus themed molecular memory or molecular switch.

Typically the layout of such a device is metal/molecule/metal whereas the molecule is applied in the form of a self-assembled monolayer (SAM). If the molecule exhibits some form of hysteretic or bistable behaviour, e.g. low- and high-conductance states depending on conformation, this unit forms a memory[45].

This type of memory is in a very early stage of development.

3.7 Resistive Memory

Resistive memory elements store data in form of different resistance states, i.e. a high-resistivity is assigned “0” and a low resistivity “1”. They usually comprise a simple architecture metal/insulator or semiconductor/metal and can be implemented in two-terminal crossbar-architecture which is favourable for high area density. A criterion to further divide the large field of resistive memory is the switching mechanism. It has been shown that in some devices switching will be bipolar[46], i.e. set and reset operation have different polarity of the bias. In this class one finds memory that exhibits a valence change mechanism (VCM) and the electrochemical metallization mechanism (ECM)[47,48].

If set and reset operation fall in the same polarity region the switching is said to be unipolar[49]. This is commonly related to thermochemical effects (TC memory). For a graphical representation see figure 3.7.

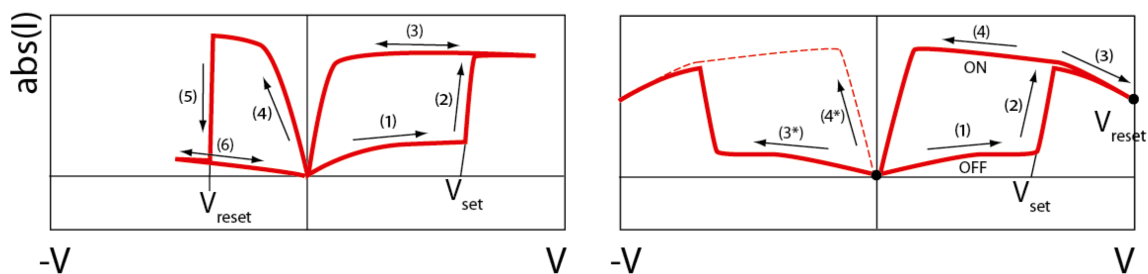


Figure 3.7 Definition of bipolar and unipolar switching behaviour. Left-hand side: bipolar switching characteristics; the SET and RESET voltages have different sign, here the cell can only be set to ON in the positive bias direction and set OFF in the negative. Right-hand side: unipolar switching behaviour under I-V sweep. SET and RESET voltage have the same sign (but might have different magnitude).

3.7.1 Valence Change Memory

In materials where oxygen vacancies are much more mobile than ions (usually transition metal oxides, e.g. TiO_2 or $SrTiO_3$) the valence of the metal can be changed by the local depletion or enrichment of oxygen vacancies. This change in valence is related to a change in electronic conductivity that can be used to represent the memory states “0” and “1”. Voltage pulses of opposite polarity can switch between high and low resistance state by changing the doping profile. During the switching process oxygen vacancies drift, forced by the electric field, towards or away from the anode. The working principle is schematically depicted in figure 3.8.

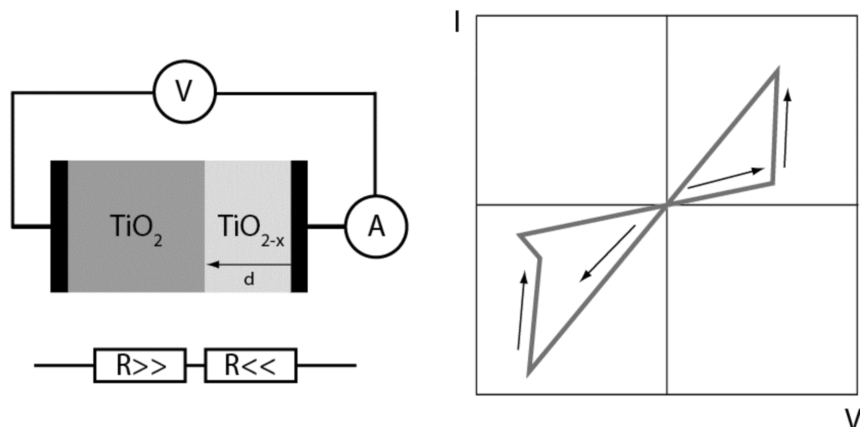


Figure 3.8 Left-hand side: schematic representation of a VCM (this is the famous "HP-memristor"). The resistance switching is explain in terms of oxygen-vacancy doping of TiO_2 to TiO_{2-x}. The bias shifts the doping-depth d and leads to a non-linearity, shown in the I-V characteristics on the right hand side. The switching is bipolar, which can be easily understood by reversing the direction of dopant-drift under a reversed polarity of the external field. Adapted from[10]

Recent work by S.R. Williams et al.[10,50,51] on Pt/TiO_2/TiO_{2-x}/Pt VCM has gained a lot of attention. The significance and originality of this work is sometimes put into question[52,53,54] but from a neutral point of view it can be argued that the connection between non-volatile memory (as the VCM) and the theory of a non-linear circuit element (the memristor[8], or more general memristive devices[9]) is significant as it has pushed open a door when it was realized that not only a single device but in fact all devices that have a pinched I-V characteristic[55] (that is, the (I,V) curve has a hysteresis and includes the (0,0) point in the I-V plane) are not only non-volatile memories but might also be looking forward to application in non-conventional computing as neuristors or artificial nerve-cells[56,57]. Though this is still highly speculative it has implications that go far beyond the scope of this thesis and should be kept in mind when evaluating the significance of any work in this area.

3.7.2 Electrochemical Metallization Cell Memory

In an electrochemical cell (ECM) an ion-conductor is sandwiched between two electrodes. One electrode is chemically active (AE, e.g. Ag, Cu) whilst the other is electrochemically inert with respect to the components of the cell (e.g. Pt, Ir). If a bias of sufficient strength is applied metal is dissolved on the anode and drifts across the intermediate layer region due to the high electric field. At the inert cathode the ion is neutralized and forms a conductive metal bridge. Thus the

name conductive bridge (CB) is also used in literature. For resetting the memory requires a voltage of suitable amplitude and different polarity, thus the bipolar nature of the device.

The work principle is shown in figure 3.9. An extensive review on this topic is given in[58,59].

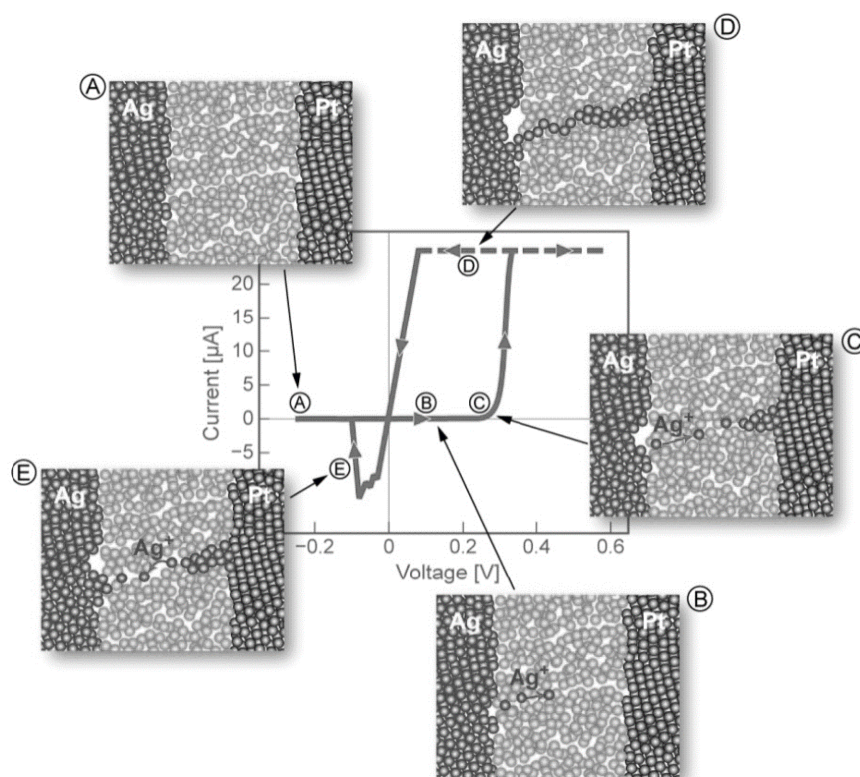


Figure 3.9 Schematic explanation of the set and reset process of an ECM. The AE in this device is silver whereas the inert electrode consists of platinum. The points for set (A-D) and reset (E) operation are marked. Taken from[58]

3.7.3 Thermochemical Memory

Metal/insulator/metal resistive memories that exhibit unipolar switching are considered to belong to the group of thermochemical memory. In this kind of memory the OFF state is usually represented by the high resistance state and by an appropriate voltage pulse the resistance can be switched by many orders of magnitudes (figure 4.3). The switching mechanism suggests that during the ON set operation a metallic highly conductive path ("filament") is formed in the insulating material, similar to the conductive bridge in ECM. Temperature investigations suggest that the switching mechanism is due to thermochemical breakdown of the oxide layer. The heat is generated by Joule heating, i.e. heat is generated by dissipation of electrical power. Historically NiO thin films were the first to be investigated in 1964[60], but a variety of other

oxides and materials were reported ever since, e.g. chalcogenide glasses[61], semiconductors[62], nitrides[63], to name a few. A more extensive list can be found in[64]. Interestingly a wide variety of combination exhibits the same switching behaviour. This already suggests a universal switching mechanism irrespective of the used material.

4 Organic Resistive Switches

As early as 1970 switching in organic materials has been reported[65] and in 1974 the relevance of polymer materials for memory application became obvious[66]. For some years the area of research was a niche topic but it attracted increasing attention around the year 2000[67].

In recent years organic electronics has successfully established its place in the electronics industry, where they sometimes outperform their inorganic counterpart, e.g. organic light emitting devices, or are competitive due to lower prices or and/new form-factors, as in flexible ultra-light organic solar cells[68].

In the course of this work it will be demonstrated that non-volatile memories that embody an organic switching medium ("active layer") exhibit properties that make them very competitive with their inorganic counterpart. From here on such devices will be referred to as *organic resistive switches* (ORS). ORS were reported to exhibit bipolar[69,70] and unipolar resistive switching. The focus here lies on ORS that exhibit unipolar switching. The current-voltage or I-V characteristic is shown in figure 4.3. The basic layout of an ORS and its integration in a crossbar array with minimum footprint $4F^2$ is explained in figure 4.1

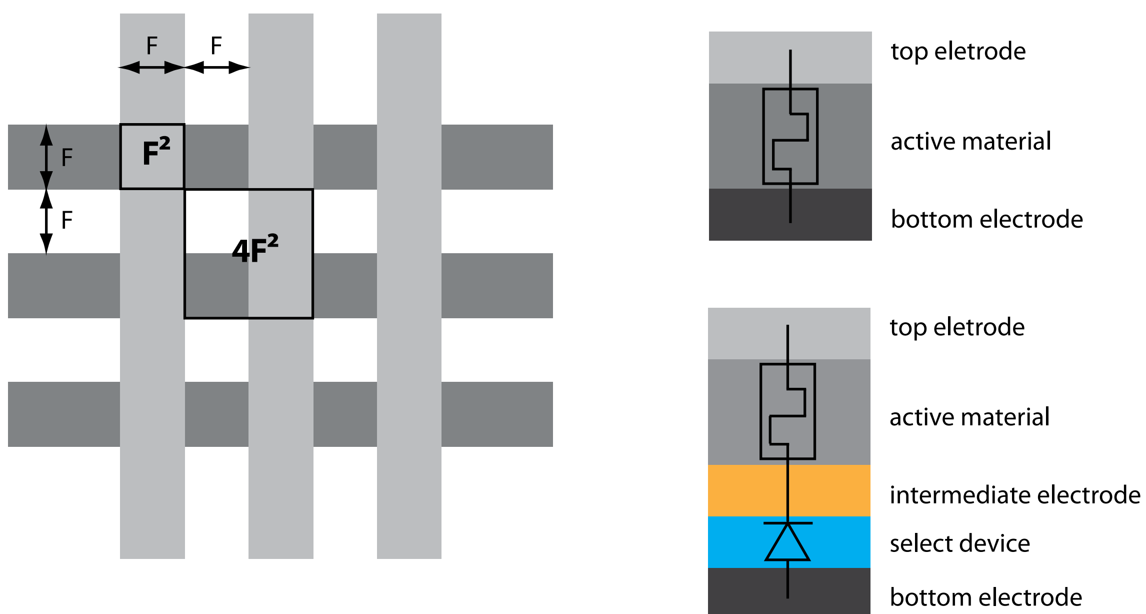


Figure 4.1 Left: schematic explanation of the integration density of $4F^2$ where F is the feature size of the memory element, i.e. the electrode and spacing width. On the right-hand side the stack of an ORS is given. This simple structure shown on top is, however, not yet suitable for array integration due to the sneak-path problem[71] (a high-resistive cell (OFF cell) surrounded by low-resistive cells (ON cells) will not be read-out correctly because of the current bypassing the OFF cell via the ON cells). For that reason a select device is necessary, e.g. a transistor or diode. A diode is a two-terminal device like the ORS itself and thus does not increase the footprint of the memory cell.

4.1 Materials for ORS

The choice of a set of materials is an ambiguous one as it was already shown that ORS can be built from an almost infinite set of combinations of conducting (metal) electrodes and insulating or semiconducting layer[72,73] without a significant change in functionality.

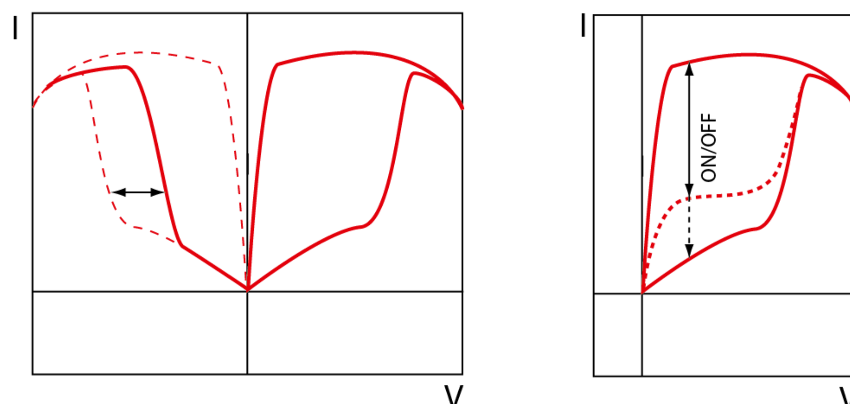


Figure 4.2 left: schematic I-V characteristic of an ORS that exhibits total symmetry when the same material is used for top- and bottom electrode (dashed line in the left half-plane) and deviation from that symmetry that occurs when one electrode is changed. Left: schematic I-V characteristic of an ORS employing an insulator (solid line) or an organic semiconductor (dashed line). The ON state is usually not effected as expected from filamentary switching mechanism, but the OFF state in an organic semiconductor exhibits higher intrinsic conductivity. Adapted from[72]

4.1.1 Electrode Materials

Usually metal or conducting oxide electrodes are used to enclose the organic layer. The switching characteristics are surprisingly independent of the choice of materials as will become more clearly later. Typical choices of materials are indium tin oxide (ITO), aluminium, silver, gold. The symmetry of the I-V characteristic in the left and right half-plane is to some extend dependent on the materials used for top- and bottom electrode. If the same material is used a totally symmetric I-V characteristic is usually observed for positive and negative bias (figure 4.2).

4.1.2 Insulating and Semiconducting Materials

The choice of insulating or semiconducting material for the active layer is rather arbitrary for the device function. A semiconducting material will usually exhibit a higher OFF current as it

has a higher intrinsic conductivity (figure 4.2). Since the ON state is not influenced significantly this will decrease the ON/OFF ratio.

Resistive switching has been reported in many organic semiconducting and insulating materials but the most prominent are: Alq_3[74], NPB[75], P3HT[76], PEDOT:PSS[77], PI[78], PMMA[79], PS[80], PVA[81], PVK[82], PVP[83].

For further work PMMA was chosen as it is a non-hazardous air-stable solution-process able and cheap dielectric.

4.2 The Switching Mechanism – A Source of Confusion

Carrying over to the research done in the past years of our time, a multitude of switching mechanisms was proposed. The initial report (1967) by Simmons and Verderber (SV-mechanism)[84] held metal particles in the insulating layer of an Al/SiO_x/Au device responsible for resistive switching. Charges trapped on this particles would build-up a space-charge field. Upon exceeding a certain voltage the trap-energy would shift with respect to the Fermi level, thus switching the device in the ON state. Upon removal of the excess charges the device would revert to its OFF state. In 1970 Dearnaley and Stoneham reported switching in metal/insulator/metal devices to be the consequence of the formation and rupture of filaments. The forming mechanism was described to involve dielectric relaxation and ion migration[85]. In the same year Pender and Fleming reported switching in organic devices. Switching in Al/Ps/Al was attributed to the formation and rupture of carbon-rich filaments[86]. In 1974 Henisch et al. attributed switching in SnO_2/PMMA/Mo to field controlled chain ordering[66]. In the following decades a variety of switching mechanisms were postulated for organic resistive switches. Switching in terms of Coulomb blockade[87], or charge-transfer processes[88], as well as conformational change in certain molecules[89]. Furthermore it was postulated that a certain amount (a thin layer of about 4 nm) of metal in the middle of the organic layer was critical to obtain switching[67].

With above wide spectrum of proposed switching mechanism in mind it is evident that a thorough investigation of the physics behind the switching mechanism is necessary in order to pave the way for future progress in the field of memory application of ORS. In 2014 Nau et al.[72] were able to proof by means of photovoltaic effect and impedance spectroscopy to break down the zoo of switching mechanism and establish filament formation and rupture as the

physical processes dominating switching from OFF to ON and vice versa, respectively. The switching mechanism is graphically presented in figure 5.3.

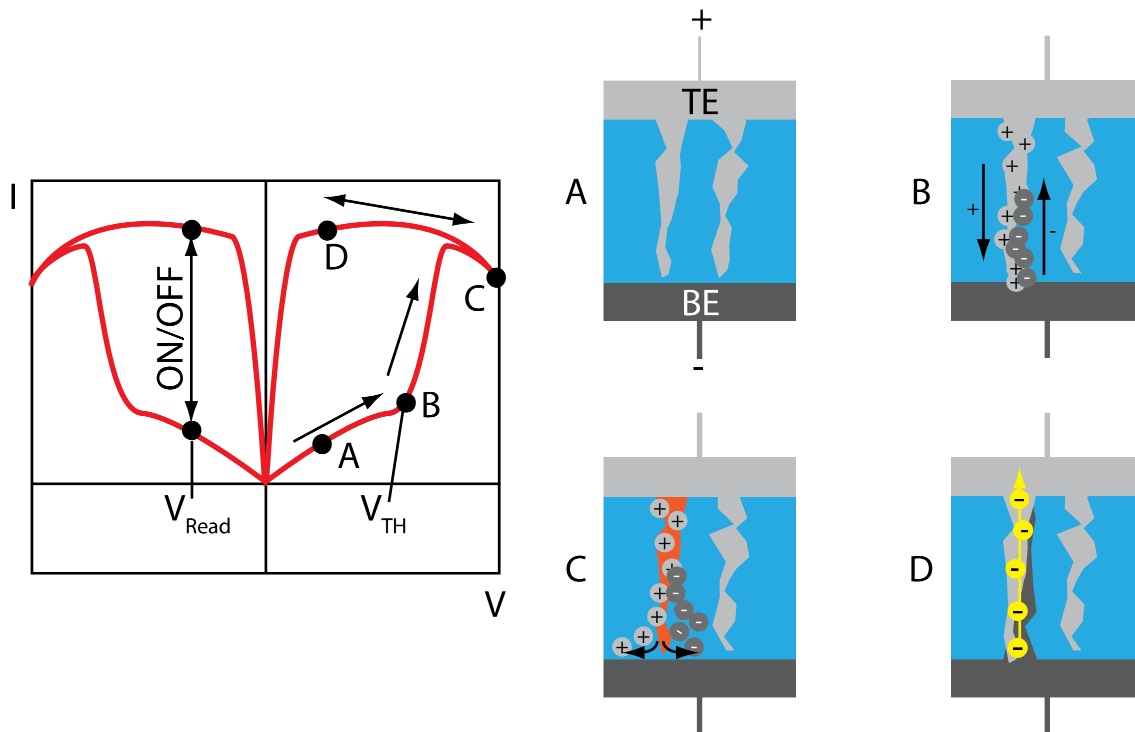


Figure 4.3 I-V characteristics and filamentary model for resistive switching in metal/insulator/metal resistive switches with thermochemical switching mechanism. The device is initially in its high-resistance (OFF) state (A) The top (TE) and bottom electrode (BE) are separated by a (thin) layer of insulating material (gap). The device exhibits space-charged limited current. Upon application of a suitable bias (the TE is positively biased relative to the TE) the insulating layer exhibits resistive switching by a heat assisted and field driven accumulation of metal atoms across the gap (B). The device is in its ON (highly conductive) state, where a metal bridge, in this context called filament, connects top- and bottom-electrode (D). The device now exhibits ohmic conduction. Upon increasing bias and current heat locally dissipates the electrode, reverting the device to its OFF state (C). Adapted from[90]

The physics behind that filamentary process, however, is still widely unknown. The motivation to get a clear understanding of the switching process are twofold. From a fundamental point of view the fact that such a simple device has evaded a rigid framework and description of the underlying working principles for so long is motivation in itself. From a more practical standpoint the missing understanding of the switching mechanism limits engineering efforts to tailor ORS to specific needs, i.e. voltage level adjustments and switching time, to name just two.

As such the aim is to build on the fundamental working principle of filament formation as a switching process and present experimental evidence that, in conjunction with a model description, will allow a better understanding of the phaenomena of resistive switching.

5 The Reference PMMA Device

The following section will discuss basic features of an ORS. The device has the structure depicted in figure 5.1 and will be called reference PMMA device throughout this work.

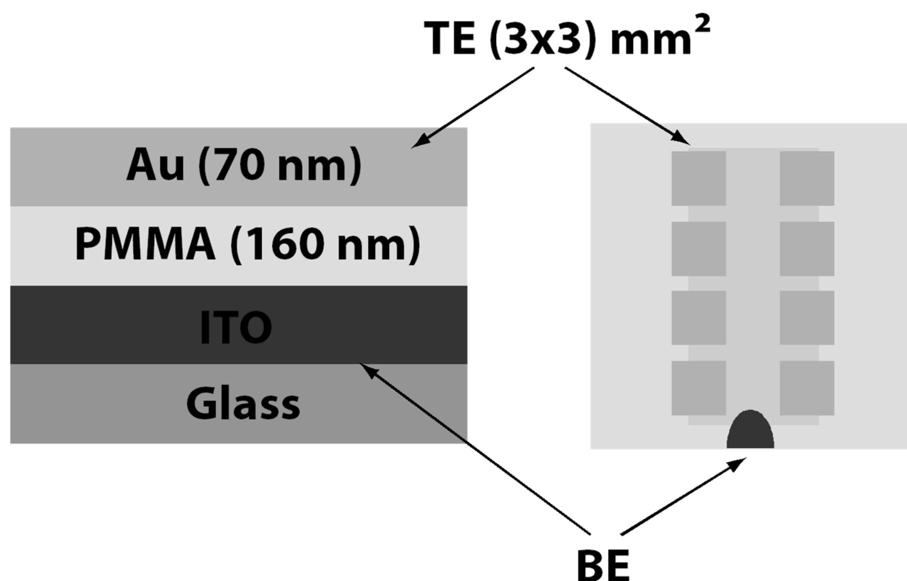


Figure 5.1 Layout of the ORS reference device. Each substrate carries 8 ORS in a single-cell layout with a common-BE. The BE is ITO on a glass substrate, the insulating layer is PMMA spin-cast from solution. The top-layer is evaporated under vacuum and patterned using a shadow mask.

5.1 Fabrication of Reference PMMA Device

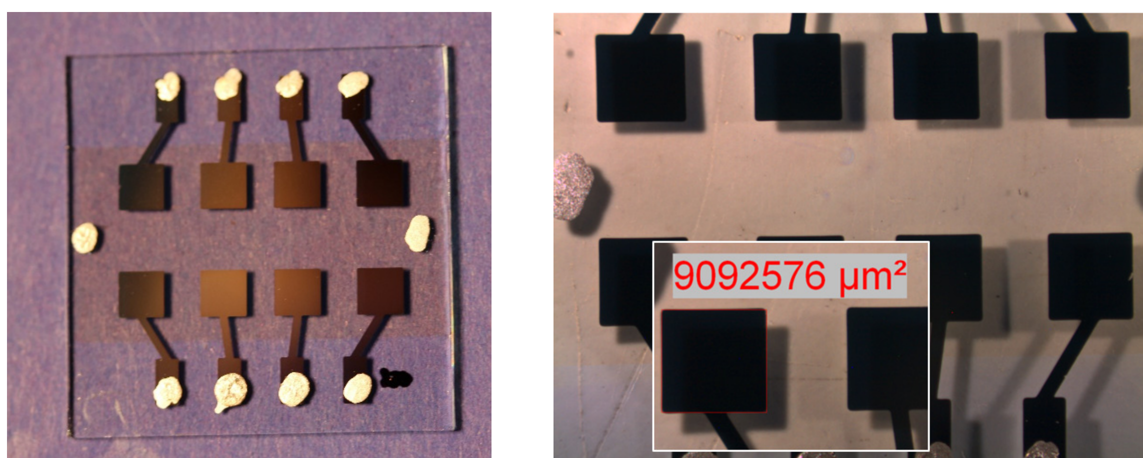


Figure 5.2 Reference PMMA device with the structure ITO/PMMA/Ag. The left hand side shows a photograph, the left hand side is recorded using a microscope under small magnification. The inset shows the electrode area is (3x3) mm²

An ITO coated glass is pre-patterned by scotch tape. The part of the ITO that is not covered by tape is etched away by hydrochloric acid. The substrate is then cleaned by rinsing in acetone and 2-propanol and 15 min sonication in 2-propanol. A 30 g/l PMMA (Sigma-Aldrich M_W~120,000) in toluene solution is spin cast using 1500 rpm for 40 seconds and a ramp of 4 under clean room atmosphere in a laminar flow box. The substrate is subsequently annealed at 170°C for 10 min to remove residual solvent. The resulting film is clear of any stains or impurities under the light microscope. Film thickness was measured to be 160 nm using atomic force microscopy (AFM). The substrate is transferred to the vacuum deposition device (VDD) and the chamber is evacuated to a pressure less or equal 10^{-6} mbar. The silver (Ag) or gold (Au) top electrode is evaporated from a tungsten boat at a constant rate of 1 nm s^{-1} to a final thickness of 70 nm. After fabrication the device is transferred to a glove box with argon atmosphere (H_2O <1 ppm, O_2 <1 ppm) for characterization. Figure 5.2 shows the final stage of the device. The yield of working devices was close to 100% with this configuration.

5.2 Basic operation principle and electrical characterization

In any application scenario the ORS is a device that is characterized from the outside by its resistance which in turn is represented by current and voltage.

5.2.1 Conditioning

A pristine device requires a conditioning procedure or forming step before it can operate as a memory. This procedure refers to a single or a series of bias sweeps that will enable resistive switching in the device. Conditioning differs from device to device but has shown to be very simple in the here presented reference device. Usually switching was obtained after a single voltage sweep 0V - 15 V – 0 V (figure 5.3).

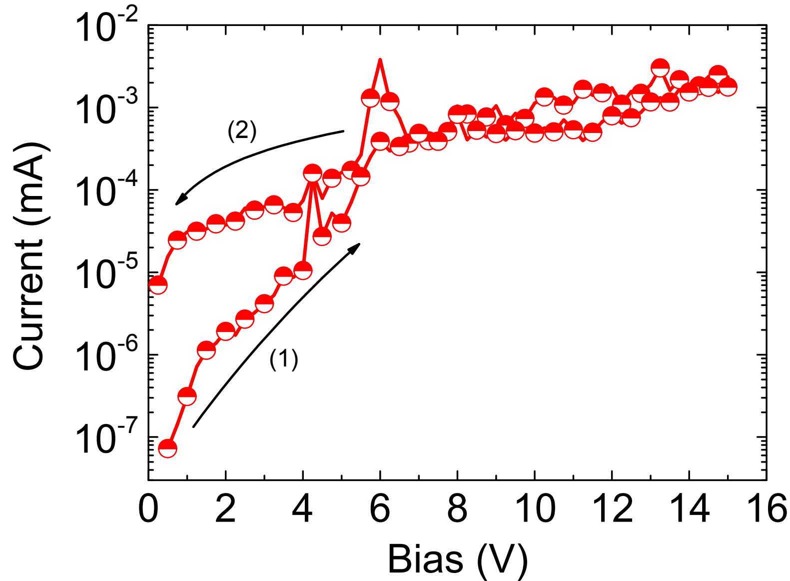


Figure 5.3 Conditioning of reference PMMA memory device. A double sweep between 0 and 15 V enables switching in this type of device. (1) and (2) refer to the sweep direction in sequence.

The commonly accepted reason for conditioning is the need to apply a field high enough to create an initial pre-filament in the organic layer[91].

5.2.2 I-V Sweep Characterization

All devices are characterized using an Agilent B1500A parameter analyser on a probe station in a glove box atmosphere (H_2O, O_2 <1 ppm) and tungsten needle contacts or a specifically made probe chamber.

The device is contacted via tungsten tips on a grounded low noise stage (Karl Süss PM5). The Agilent B1500A parameter analyser is connected via triaxial cables. The device is characterized using the standard I-V sweep mode. In all characterizations unless noted otherwise the positive bias is applied on the top electrode and the bottom electrode is grounded.

The I-V characteristic obtained from a reference PMMA device under positive bias sweep (0->5 -> 0 V) is depicted in figure 5.4. The sweep sequence is indicated by numbered arrows. Initially the device is in its OFF state and the conduction is low. At roughly 3 V switching occurs as indicated by the sudden surge in current. Upon increasing the bias further the NDR region is reached where a gradually increased bias leads to a decrease in current (3.5 – 4.5 V). At the end of the NDR the device can be reset to the OFF state (5 V). If the bias is decreased from 3 V down to 0 V the device is in its ON state as indicated by the much higher current

level. If read out at 1 V the device has an ON/OFF ratio of more than 4 orders of magnitude. The grey shaded areas indicate proper voltage levels for pulsed operation mode: read – 1 V, set – 3 V, reset – 5 V.

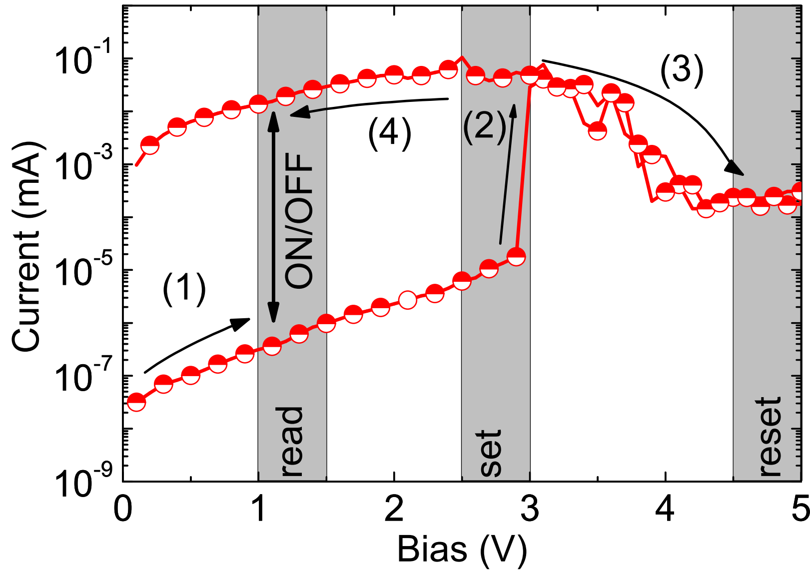


Figure 5.4 I-V characteristics of a conditioned reference PMMA device under positive bias sweep. (1)-(4) and the arrows refer to the sequence of sweeps and direction. Switching occurs at 3 V, the NDR lies between 3.5 and 4.5 V and the memory can be reset at 5 V. The bistable behaviour can clearly be seen, the ON and OFF state are separated by a factor of 10^4 at 1 V. The grey bars indicate voltage levels for pulsed memory operations.

5.2.3 Conduction Mechanism in I-V Sweep Mode

A common method to evaluate the conduction is a double-logarithmic plot. This way a wide spectrum of conduction mechanisms has been observed and fitted[92]. In a metal current is known to follow Ohm's law (eq. 1):

$$J_{drift} = \mu enE = \mu en\frac{V}{d} \propto V^1 \quad \text{Eq. 1}$$

Here one assumes that free mobile electrons (valence electrons) in a high uniform density (n) and constant mobility (μ) are drifting under the influence of an electric Field (E) that is directly proportional to the applied bias voltage (V). The situation in semiconductors and insulators is however different as free charge carriers have a much smaller or vanishing density. In such a material charges can accumulate and limit the charge-transfer. This is known as space-charged

limited current (SCLC), commonly known as Child's law[93]. For ohmic injection, unipolar conduction and in absence of traps it can be written (eq. 2)[93].

$$J = \frac{Q}{t} \approx \frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{L^3} \quad \propto V^2 \qquad \text{Eq. 2}$$

This can be extended to include shallow traps. The mobility μ is replaced by an effective mobility $\mu_{eff} = \mu\Theta$ where the trap depth E_{td} and the density of traps states N_t is included in the factor Θ accordingly to (eq. 3)

$$\Theta \approx \frac{N_c}{N_t}\exp\left(-\frac{E_{td}}{kT}\right) \qquad \text{Eq. 3}$$

This can be interpreted to be the result of only a fraction of the charges injected are free, therefore the mobility is reduced by a factor Θ. In this case the current will still be proportional to V^2 since Θ is independent of V. In case of SCLC the lower bias regime still shows ohmic conduction if the thermally generated free carriers n_0 inside the material dominate. The onset of SCLC then takes place at $V = \frac{8}{9}\frac{qn_0d^2}{\varepsilon}$ [94].

A deviation from the above presented power law occurs when traps limit the conduction. This is known as Helfrich-Mark model[95] and the current-voltage relation has the form (for traps distributed exponentially in energy space) (eq. 4)

$$J = q^{1-l}\mu N_v\left(\frac{l}{l+1}\frac{\varepsilon\varepsilon_r}{H_b}\right)^l\left(\frac{2l+1}{l+1}\right)^{l+1}\frac{V^{l+1}}{d^{2l+1}} \propto V^{l+1} \qquad \text{Eq. 4}$$

Here the trap distribution is represented by a characteristic temperature T_c and occurs as fitting parameter in above formula $l = \frac{T_c}{T}$. The total trap-density is H_b. By taking a double-logarithmic plot the transport mechanisms can be analysed as depicted schematically in figure 5.5.

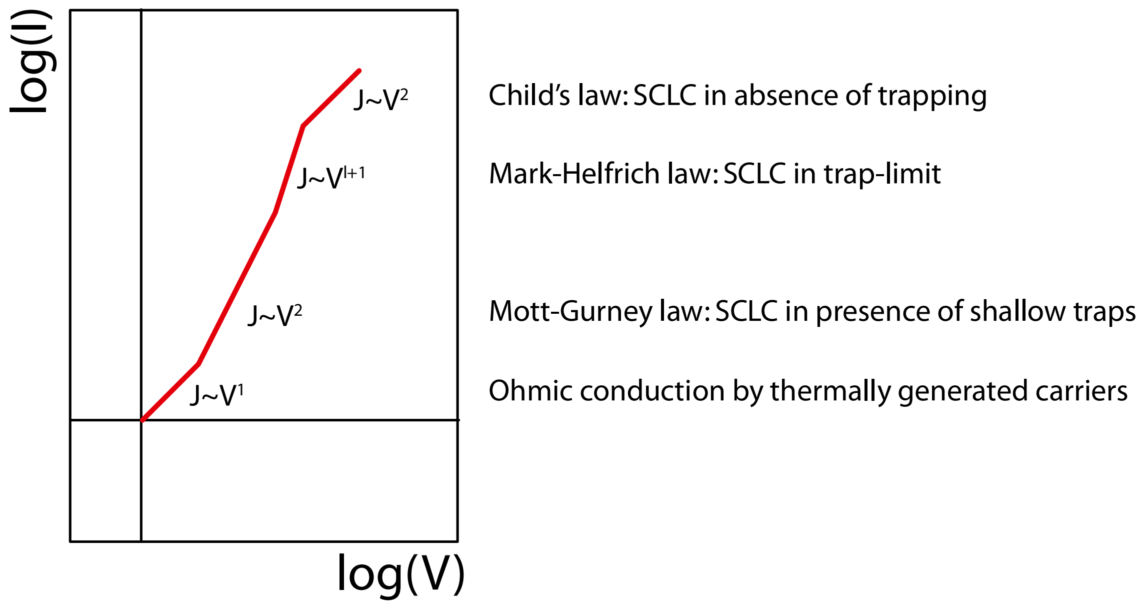


Figure 5.5 Different regions for SCLC and the corresponding exponents (slopes) of the I-V characteristics for a single charge carrier in an insulating or semiconducting organic film with ohmic contact. Adapted from[96]

Using these equations good agreement between obtained data and the model is found as depicted in figure 5.6. First, for the OFF state, a slope very closed to 1 is observed in accordance with the ohmic conduction by thermally generated carriers. A transition to SCLC in presence of shallow traps is observed. For the ON state a slope of 1.5 is fitted, which does not fit perfectly for ohmic conduction but a small deviation is expected as the filament cannot be thought of as a solid wire.

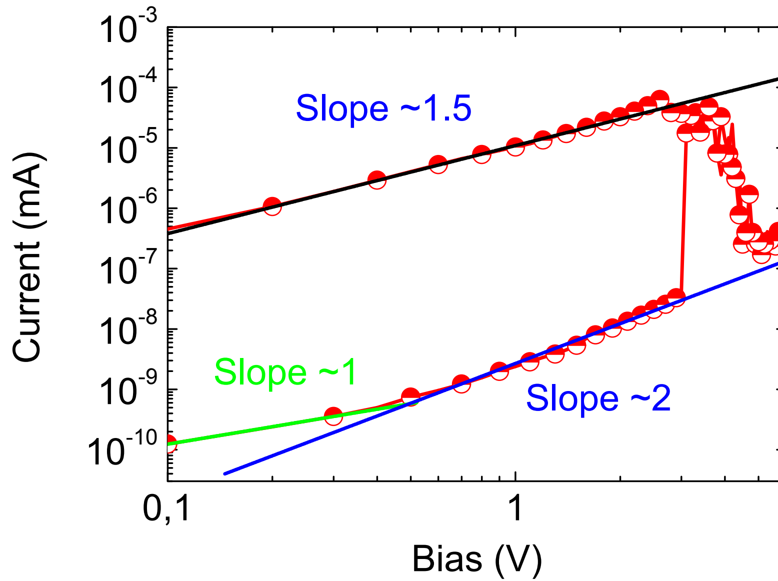


Figure 5.6 double-logarithmic plot of the I-V characteristics of an ITO/PMMA/Au device under positive bias. The fitted lines indicated the slope. The OFF state can be fitted with two slopes, (0.96±0.007) and (2.19±0.05), respectively, in good accordance to SCLC with thermally generated carriers and in absence of traps, respectively. The ON state slope is (1.46±0.02), close to ohmic.

5.2.4 Memory Stability Measurement

A desired property of any memory is a stable ON and OFF state, i.e. the states do not exhibit a drift over time. To test the stability of the reference PMMA device the memory device was set into its ON state and then measured for at least 200 seconds under a constant bias of 1 V in 200 ms time-steps amounting to approximately 10000 measurements. The resulting figure 5.7 clearly shows that at a read-out bias of 1 V the memory state is stable for at least 200 seconds. The drift of the ON state resistance is minimal and standard deviation lies within approximately 8% ($(48000 \pm 4000)\Omega$).

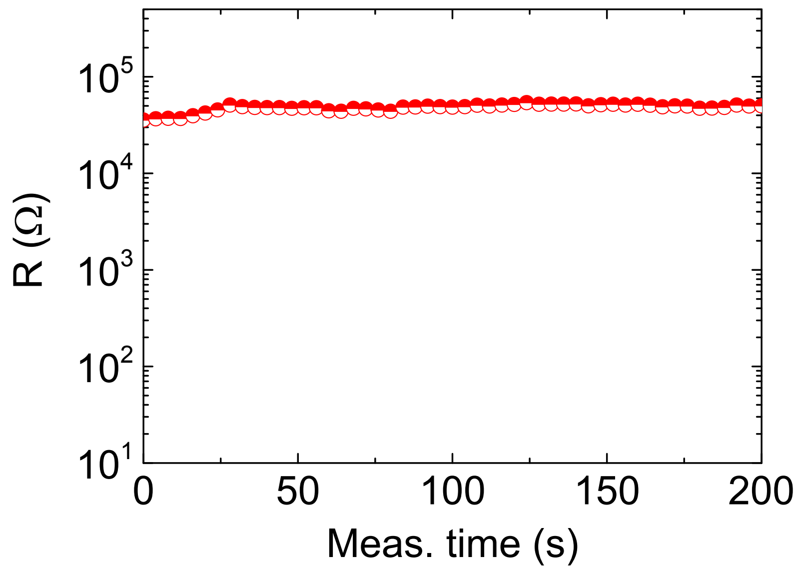


Figure 5.7 Stability of the memory state "ON" over 200 seconds under constant read-out bias of 1 V. A measurement at 1 V was taken every 200 ms amounting to 1000 data points. Only 5% of points shown here to increase visibility.

5.2.5 Memory Cycle Test

For this test voltage pulses of 3 V (write) and 6 V (erase) were applied for 50 ms each. In between the resistance was read-out at 1 V with the same pulse length. The resulting figure 5.8 clearly shows that the switching is quite reliable. If a tolerance-range (grey boxes) of height 10^2 is drawn for OFF and ON state approximately 50 out of 500 states fall out of both ranges. Interestingly the switching appears to be more reliable towards the end of the measurement. This could indicate that the device has not been perfectly conditioned initially. Even though this is not a perfect behaviour it shows that switching in the reference PMMA device is reliable.

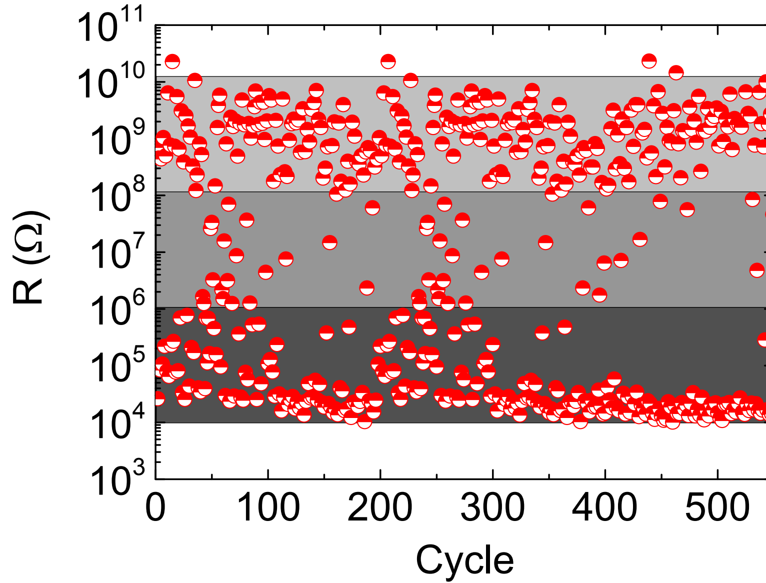


Figure 5.8 Switching pattern of reference PMMA ORS. 3 V and 6 V were applied to write and delete the memory. In between the memory state is read out at 1 V. All pulses were applied for 1 ms. The grey boxes indicate ranges of height 10^2. Approximately 50 out of 500 states fall in the centre box, i.e. indicating that switching failed and a clear discrimination of the ON and OFF states is no longer possible.

5.2.6 Impedance Characterization

Another powerful tool is LCR spectroscopy or impedance spectroscopy where the devices' impedance and phase angle response for an AC signal ("level") is recorded. Using an equivalent circuit diagram (ECD) as suggested in[72], the device can then be modelled using two basic components capacitance (C) and ohmic resistance (R)[97]. With respect to a physically correct model it can be clearly shown that a capacitive behaviour is measured in an OFF device. This changes to ohmic when a device ON state is measured. The amplitude of the level needs to be low enough to ensure the device is not switched during measurements.

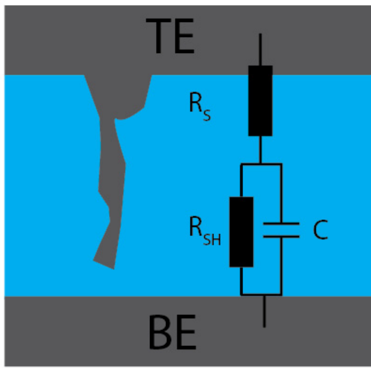
By means of an equivalent circuit (EC) analyser the phase and impedance spectrum can be fitted to obtain the numerical values of the electrical devices in the circuit. The software used is the freeware *EIS analyser*[98].

For an ORS the simplest ECD is presented in figure 5.9. This EC and typical values for R_{SH}, R_S and C are used to simulate the phase behaviour, as is shown on the right hand side of the figure. The analytical expression for this EC is given in[72] and shown in (eq. 5) for the phase angle and in (eq. 6) for the impedance.

$$\tan(\varphi) = \frac{\frac{2\pi \cdot f \cdot C \cdot R_{SH}^2}{1 + 4\pi^2 \cdot f^2 \cdot C^2 \cdot R_{SH}^2}}{R_s + \frac{R_{SH}}{1 + 4\pi^2 \cdot f^2 \cdot C^2 \cdot R_{SH}^2}} \quad \text{Eq. 5}$$

$$Z = R_s + \frac{R_{SH}}{1 + 4\pi^2 \cdot f^2 \cdot C^2 \cdot R_{SH}^2} + i \cdot \frac{2\pi \cdot f \cdot C \cdot R_{SH}^2}{1 + 4\pi^2 \cdot f^2 \cdot C^2 \cdot R_{SH}^2} \quad \text{Eq. 6}$$

$$|Z| = \sqrt{Re\{Z\}^2 + Im\{Z\}^2}$$



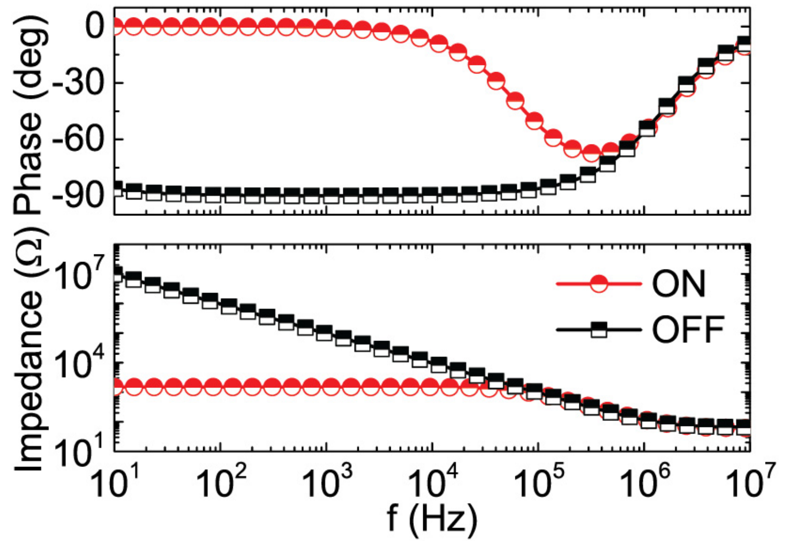


Figure 5.9 left: schematic cross-section of an ORS in ON and OFF states, respectively and the corresponding ECD. RS is the series resistance, RSH the shunt-resistance and C the capacitance of the circuit. In case of an ON device RSH will be small and therefore dominate the impedance characteristics at low frequencies. At high frequencies the impedance contribution from the capacitance will be small and dominate the parallel circuit. By previous considerations the switching should therefore be observable by a change of impedance and phase angle. On the right-hand side a simulation of the phase behaviour for ON and OFF state is given, showing previously described phase behaviour, the values used for the simulation are R_S=60 Ω, R_{SH}=10^3 Ω, C=1 nF (ON) and R_S=60 Ω, R_{SH}=10^6 Ω, C=1 nF (OFF), respectively . Adapted from[72]

The LCR spectrum of the reference PMMA device was recorded in a range of 20 Hz to 2 MHz and a level of 500 mV (rms) (figure 5.10). In the phase picture we can clearly see a transition from ohmic behaviour (phase angle close to 0°) to capacitive behaviour (phase angle -90°) when the device is switched from the ON to the OFF state. At high frequencies both lines coincide

indicating an almost identical series resistance which dominates the EC at high frequencies. The numerical values for ON and OFF state are summarized in table 2.

Table 2 Results for impedance spectroscopy of ON and OFF state of reference PMMA device. The uncertainty shown is solely of the fit. The fitting routine used was Levenberg–Marquardt. As expected the RS changes only insignificantly and the capacitance for ON and OFF state is almost identical. The main contribution to ON/OFF switching is the shunt resistance, a strong indicator for filamentary switching.

	R_{SH} (Ω)	R_S (Ω)	C (nF)
ON	$(1.007\pm0.0007)*10^5$	(40 ± 9)	(1.280 ± 0.006)
OFF	$(5.92\pm0.06)*10^8$	(48 ± 2)	(1.28 ± 0.04)

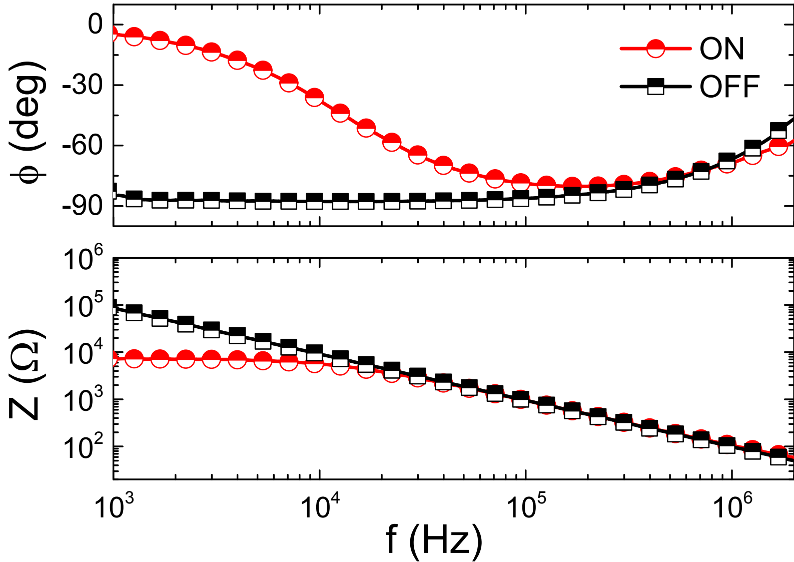


Figure 5.10 Phase angle and impedance spectra over frequency. The change in phase angle from ON state (circles, dominated by a low phase angle, ohmic resistance) to the OFF state (squares, phase angle close to -90°, dominated by capacitance) is clearly observable and in excellent agreement with simulated results previously shown.

5.3 Influence of H_2O and O_2 on the Switching Mechanism of Standard PMMA ORS[2]

To further investigate the switching mechanism a set of experiments was designed to investigate the influence of reactive species, namely water in form of relative humidity (RH-%) and oxygen (O_2 vol.-%). For this experiment the ORS was fabricated according to previously reported methods using the glass/ITO/PMMA (160 nm)/Au (70 nm) stack in a flow cell and a gas-flow controller. In a mix setup the cell is first flushed with inert nitrogen (N_2). After the conditioning sweep the device is then operated whilst the atmosphere is controlled by selectively adding O_2 or H_2O to the N_2 atmosphere.

5.3.1 Stability of the ON State under Readout and Reactive Atmosphere

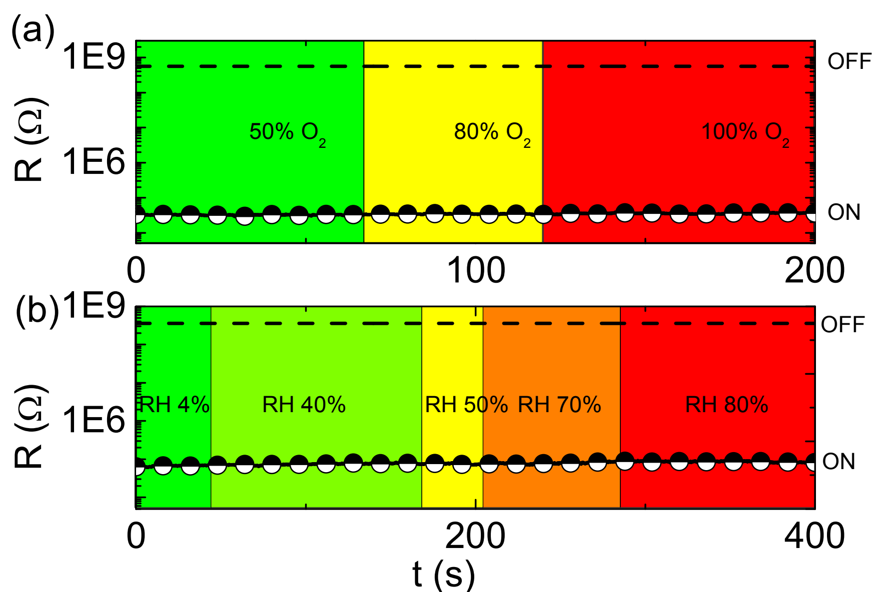


Figure 5.11 Stability of the memory ON states read out at a continuous bias of 1 V over time as a function of relative oxygen (a) and relative humidity (b) in nitrogen gas, respectively. The concentration is indicated by the colour and is raised during the measurement. The memory state is clearly preserved over time and the variation of the ON state resistance is minimal when compared to the ON/OFF difference (the OFF state is indicated by the dashed lines). Note that in graph (b) the total measurement time is longer in order to stabilize the humidity in the measurement chamber

[2] Parts of this section were published separately in Applied Physical Letters

The device was switched on under inert N_2 atmosphere. Then the reactive gases O_2 and H_2O are added, respectively. The relative concentration is controlled by a gas-mix setup. By subsequently increasing the concentration of the respective gas, as indicated by the shaded areas in figure 5.11. During the entire measurement the memory state is monitored by reading out the memory at 1 V. Clearly, the stability of the ON state is not significantly influenced as long as the voltage level is low, i.e. read-out around 1 V. Under a constant readout bias of 1 V the memory state did not degrade for a testing time of 200 s for O_2 and 400 s for H_2O. For H_2O the measurement time was longer in order to stabilize the RH-% in the cell.

5.3.2 Switching Under Atmosphere

After the state-stability was confirmed the actual switching process under reactive atmosphere was investigated. An I-V sweep for the ON device showed that at a certain power occurring around 1.5 V and 10^{-2} mA the memory state starts to degrade and the device switches to its OFF state. More detailed investigations revealed that as little as 5 vol.-% O_2 or 10 RH-% were sufficient to lead to a degradation of the memory state and suppress switching under sweep or pulse operation. For the results refer to figure 5.12 and figure 5.13 for RH-% and vol.-% O_2, respectively. The failure mechanism in both experiments are basically identical: approaching a certain threshold corresponding to a distinctive dissipated power (marked by a certain bias level and current) the filament rapidly degrades. During the following sweep switching is always suppressed. When the chamber is flushed with N_2 for a short time (range of seconds) full switching is re-established without another conditioning sweep.

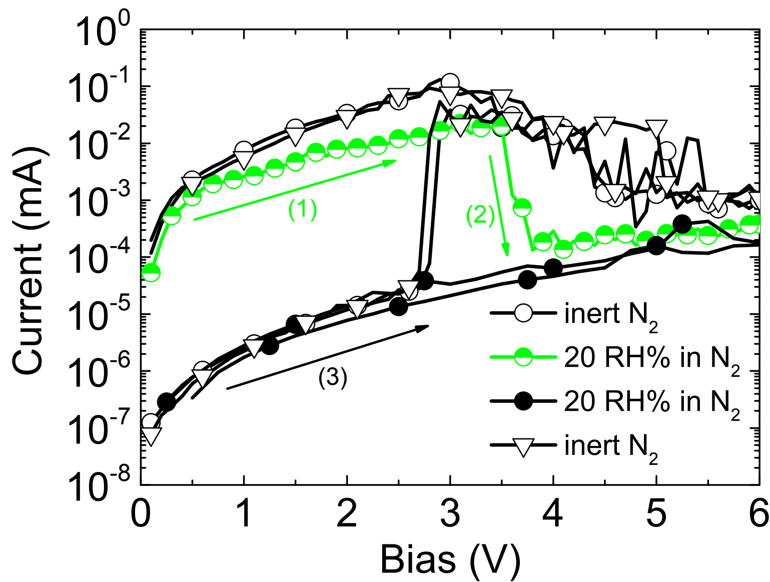


Figure 5.12 Change of switching behaviour under **relative humidity** in nitrogen atmosphere. After an initial sweep under nitrogen atmosphere (open circle) the device was switched on. Then water vapour (20RH% is shown here) is introduced into the chamber. Under a subsequent I-V sweep the device fails (half-filled circles) at around 4 V indicated by arrows), and switching could not be facilitated (closed circles) in the following sweep. After flushing the chamber with nitrogen for approximately 5 seconds full switching was re-established (open triangles).

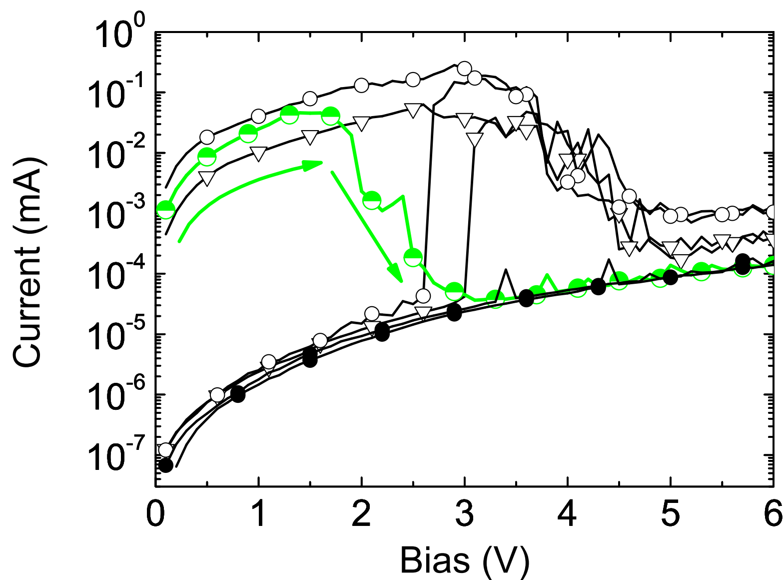


Figure 5.13 Change of switching behaviour under **oxygen** atmosphere. The device is initially in its ON state. Oxygen is introduced into the chamber (100% is shown here). Under a subsequent I-V sweep the ON state degrades at around 2 V (indicated by the arrows). Switching from OFF to ON could not be facilitated in the following sweep (closed circles), the reactive atmosphere blocks the switching mechanism. After flushing the chamber with nitrogen for approximately 5 seconds switching was possible again when the memory was tested under I-V sweep (triangles).

5.3.3 Switching With Current Compliance

To demonstrate that the suppression of switching is power-related switching in reactive atmosphere under limited current (current compliance (CC)) was tested. For low level of CC switching was possible but under increasing of CC the memory state, again, fails. As such the process of switching ON and OFF is clearly facilitated and limited by dissipated power, respectively. The result is depicted in figure 5.11. An I-V sweep of an OFF device is taken to trigger a switching event. Under as little as 5 vol.-% O_2 in N_2 no switching is observed without CC. When a low CC is set, e.g. 10^{-3} mA switching was possible. When the CC was increased, however, the device would again degrade into the OFF state and it is not possible to switch it to the ON state. This is a very strong indication that the switching is related to a certain dissipated power and the presence of a reactive gas lowers the power to degrade the filament significantly.

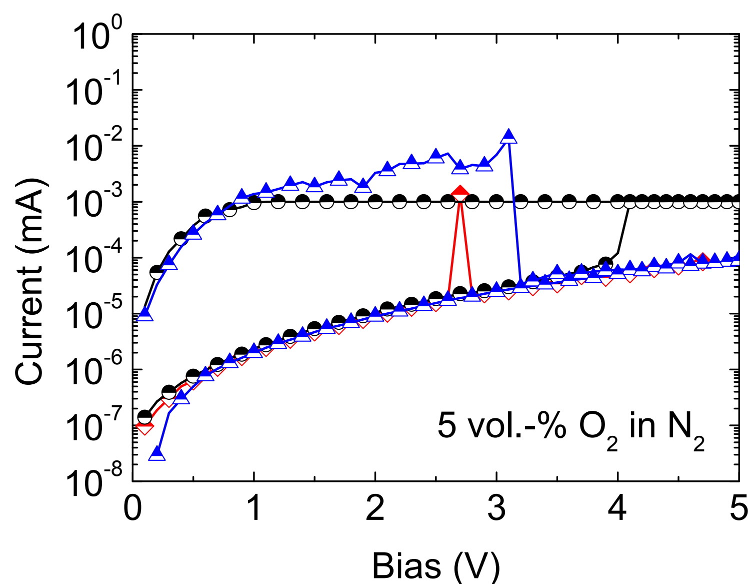


Figure 5.14 Investigation of switching under reactive atmosphere, here 5 vol.-% O2 in N2. An I-V sweep of the OFF state devices shows that without CC switching from OFF to ON is suppressed (diamonds) and no switching occurs. When the current compliance is set to 10^{-3} mA (half-filled circles) switching ON is again possible. However increasing the CC in the following sweep to 10^{-1} mA resets the memory to the OFF state (triangles). With the same CC no switching occurs in the following I-V sweep.

5.4 Time-of-Flight Secondary Ion Mass Spectroscopy

Since all above mentioned investigation methods are indirect methods, i.e. a model of some sort is needed to connect the physical process of resistive switching to the data an additional, direct method for ORS analysis will aid in gaining insight to the switching mechanism.

Devices were fabricated and set to specific conditions (pristine, pre-switching, memory cycle ON, memory cycle OFF) and then analysed by time-of-flight secondary ion mass spectroscopy[3] (TOF SIMS). The nature of TOF SIMS is entirely invasive as a cutting ion beam scans the surface removing atoms. The removed atoms or ions to be precise are then analysed using mass spectroscopy. Thus for each pixel of the device the concentration of a certain ionic species can be determined and a 3-D reconstruction of the device is possible.

Dual beam ToF-SIMS imaging (TOF-SIMS IV spectrometer, by IONTOF) was performed, in non-interlaced mode, using low energy Cs+ ions (500 eV) for sputtering, and a Bi3+ beam for the analysis phase. Each volume element of (1x1) μm^2 (in-plane) x 1 nm (in-depth) contains information of the full mass spectrum, with a mass resolution $M/\Delta M \sim 5000$. 3D reconstructions are generated by selecting a mass peak in the mass spectrum and visualizing its intensity in the analysed volume. The filament position could be easily identified in operated devices due to the different local chemical composition (mainly due to a higher surface contamination) which modifies the contrast of the secondary ions image of the top electrode surface.

For the evaporated TE the interface was investigated as well as the evolution of filaments in the device at different stages: pristine, cycled, OFF and ON state and completely erased (see figure 5.15). The ON and OFF state can be clearly distinguished by stronger penetration depth of the metal in ON devices compared to OFF. Pristine and ON devices share some similarities as can be expected as pristine devices have shown to be actually in an ON-like state after fabrication.

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[3] The TOF-SIMS analysis was performed by Yan Busby at Université de Namur ASBL.

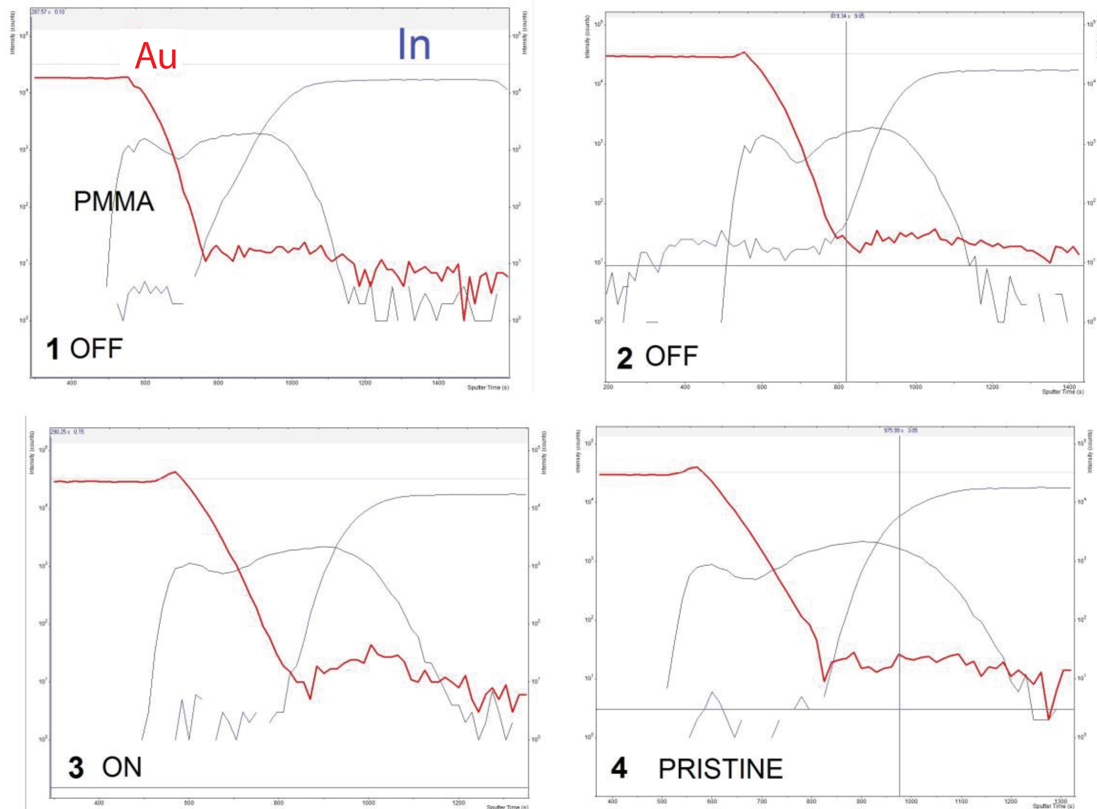

Figure 5.15 TOF-SIMS reconstruction of the different stages of ORS. OFF, ON and pristine device stages are shown. The lines refer to the concentration of the investigated elements (Au, PMMA, In are shown). ON and pristine device show relative similar characteristics. The Au and In concentration in the PMMA layer is increased compared to the devices in OFF state.

To get a clear spectroscopic picture of the filament in ON and OFF state the surface was scanned for high concentrations of metal ions in the organic layer using <yx> scan mode. At a point of increased metal concentration the device was then cut in the <yz> or <xz> direction to reveal the nature of the filament. The results are depicted in figure 5.16. As can clearly be seen in a pristine device there is only very weak diffusion of gold from the TE in the organic layer. Upon conditioning this concentration is clearly increased leading to a strong filament-type gold path in active and inactive devices whereas the latter only differs in the absolute concentration but not in the nature of the filament. In switched ON devices (active filament) there is a considerable counter-drift of indium from the BE that is not present in the OFF device (inactivated filament). We can thus conclude that the switching is facilitated in terms of change of indium concentration. If the device is forcefully deleted (burned out) there is a hole from the TE to BE and in the organic layer. An investigation of other elements ("contaminants") show (figure 5.17) that there seems to be a hole in the PMMA where the contamination is dominant when compared to the surrounding area.

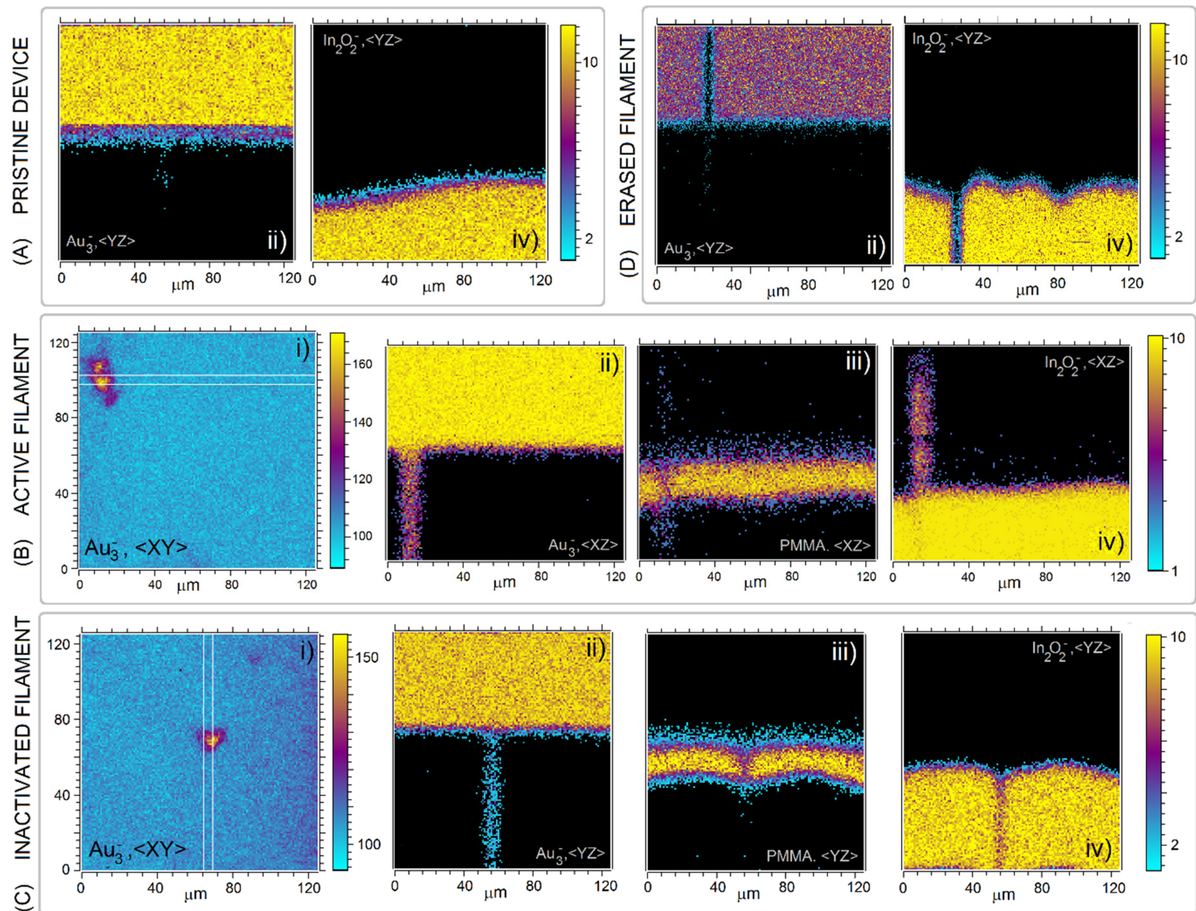

Figure 5.16 TOF-SIMS analysis of Au, PMMA and In of different states of differently conditioned ORS. (A) Pristine device, (B) active filament, (C) inactivated filament (D) erased filament. Compared to the pristine device the concentrations of Au and In in the PMMA layer for active devices is clearly increased. In an inactivated ORS the In concentration is reduced. In an erased filament Au and IN is completely removed from the PMMA layer.

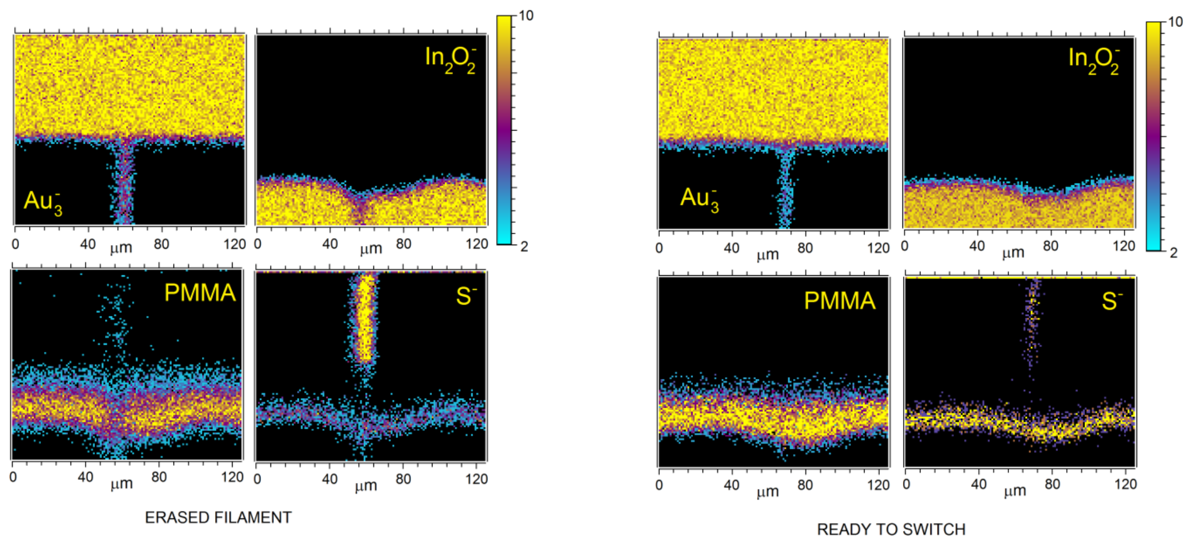

Figure 5.17 ToF-SIMS cross-sections reconstructed from 3D profiles showing the preferential diffusion of contaminants (here for S but similar results for Cl, O, K) in an erased filament (left panels) and a ready-to-switch filament (right panels).

6 ORS with Transfer Printed Gold Top Electrode

There is a widespread uncertainty about the role of metal atoms or ions implanted in the organic layer during fabrication on the switching behaviour. Early reports on ORS go as far as to claim that metal present within the organic layer is critical for the switching ability[67] and related mentioning of metal implanted in the organic layer during evaporation of the top electrode to be substantial for switching[99,100].

6.1 Fabrication of Transfer Printed ORS

Since the switching mechanism in MIM device seems to be universal the influence of implantation can be questioned. To investigate this thoroughly ORS were fabricated without evaporation of the top electrode (TE). Instead the TE was transferred by means of van-der-Waals forces under intimate contact of a soft polydimethylsiloxane (PDMS) stamp covered with gold under low temperature, a so called metal transfer print (MTP), also frequently referred to direct metal transfer (DMT) in literature[101]. The successful fabrication of ORS using MTP shows that roll-to-roll fabrication is a suitable fabrication method for ORS.

6.1.1 Stamp Fabrication for MTP

First a negative of the electrode structure (essentially two parallel metal lines with a width of approximately 3 mm) were patterned on a Si-wafer using a photolithographic process and SU-8 photo resin. Then the wafer was mounted in a casting mould (3D printed). The PDMS (Sylgard 184, Dow Corning) was mixed (1:10 of curing agent:silicone base) and degassed in an exicator to remove the bubbles. After carefully casting the PDMS into the mould it was cured for about 4 hours under elevated temperature of 60°C. This results in a bubble-free flexible substrate carrying the elevated features of the electrodes (figure 6.1).

Before the PDMS stamp is covered with metal it was treated with hexamethyldisilazane (HMDS) at high temperature to ease the transfer from the stamp to the ORS device.

Finally the stamps are mounted in the vacuum chamber and gold is evaporated at a base pressure of $1*10^{-6}$ mbar at a steady rate of 1 nm s^{-1} to a thickness of about 70 to 100 nm (confirmed by AFM).

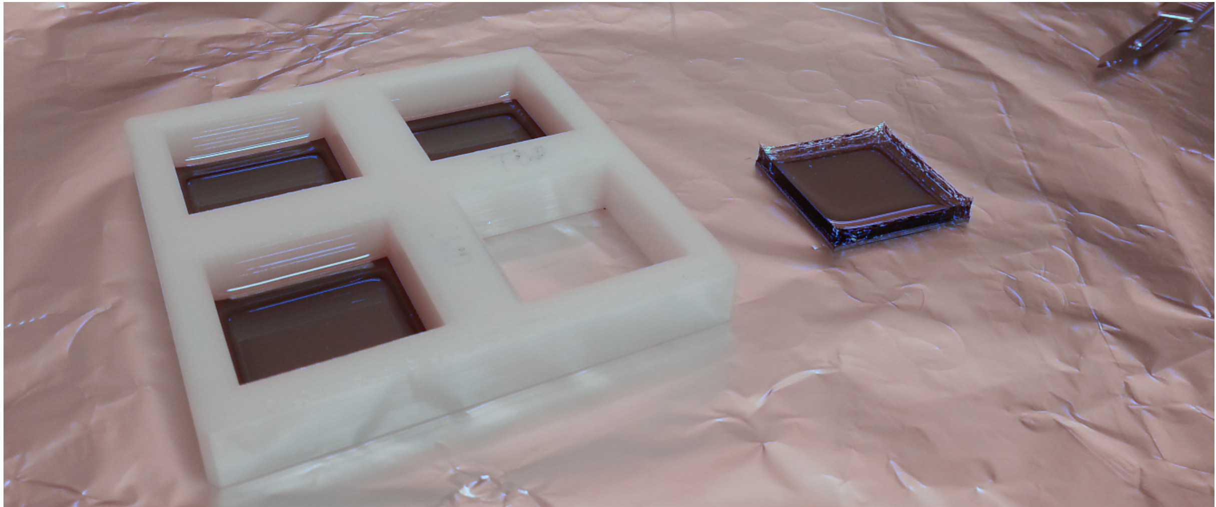

Figure 6.1 Stamp mould and PDMS stamp as prepared for HMDS treatment

6.1.2 Fabrication of ORS Using MTP

The remaining layer of the ORS was again spin cast (PMMA 30 g/L toluene, 160 nm) and annealed at 170°C on top of patterned ITO on glass substrate. After heat treatment the gold covered PDMS stamp and the substrate was brought to transfer temperature (range 105°C-160°C) and the stamp is aligned and placed on the PMMA using only a small additional weight of about 30 g. After waiting 10-30 seconds the stack is removed from the heat plate and cooled down to room temperature (about 10 min). With a swift motion the stamp is removed and the gold is transferred neatly to the PMMA. Scanning electron microscopy investigations revealed that the so transferred layer consists of many islands and micro-cracks (figure 6.2) but conductivity was close to literature values for a neat evaporated Au film (confirmed by four-probe measurement).

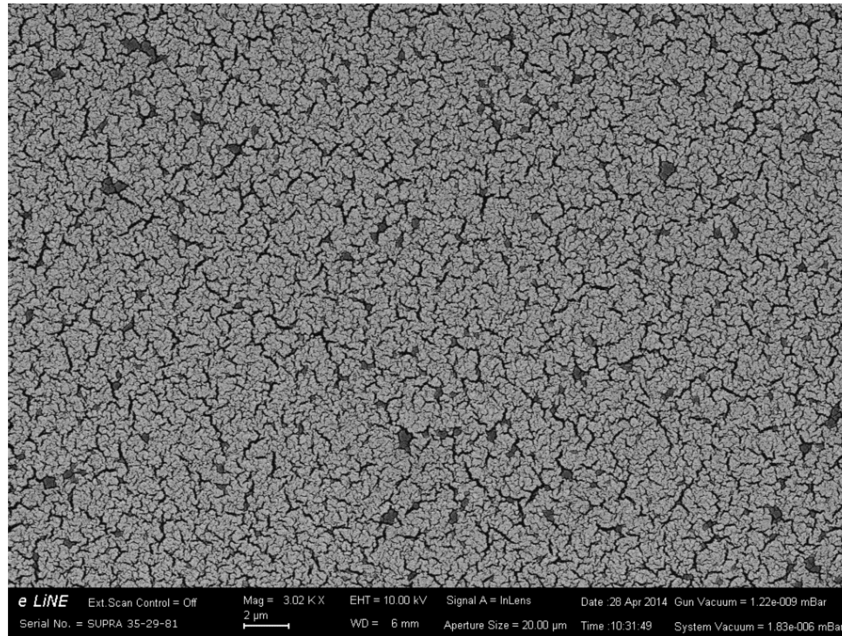

Figure 6.2 Gold layer after transfer under the scanning electron microscope clearly showing a huge amount of cracks and islands.

Electrical characterization was performed using an Agilent B1500A parameter analyser. The device was kept under inert Ar atmosphere in a glove box (O_2, H_2O < 1 ppm). Contact was obtained via tungsten needles on a probe stage (Züss PM5)

6.1.3 Conditioning Procedure

Switching ability was easily obtained by applying a single 0-15 V sweep. In that aspect there is virtually no difference to the evaporate TE devices. As shown in figure 6.3 the device seemed to be initially in an ON-like state. This might be due to a very inhomogeneous TE and a likewise fabrication-related increased defect density in the PMMA layer leading to a pre-conditioning filament. The high current degrades around 3 V under the initial sweep and upon reverse sweep direction switching can be observed.

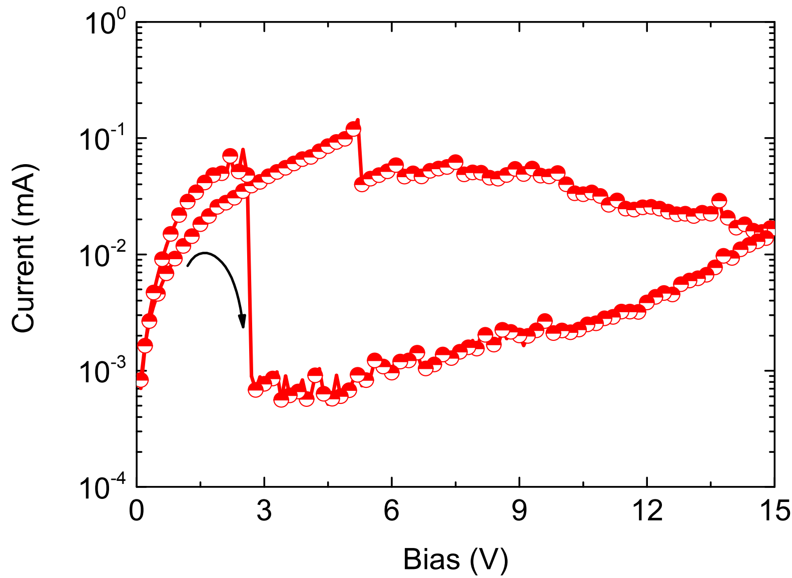

Figure 6.3 Conditioning of MTP ORS. The device was ready to switch after a single 0-15 V sweep. The device appeared to be initially in an ON state (high current level) and was reset by the initial sweep (indicated by the arrow).

6.1.4 Memory Sweep Characteristics

A double sweep of the conditioned MTP TE ORS is shown in figure 6.4. Similar to the standard ORS device the threshold voltage is around 2.5 V and the NDR spans from 3.5 to 5 V. The ON/OFF ratio is slightly lower at 10^3 measured at 1 V.

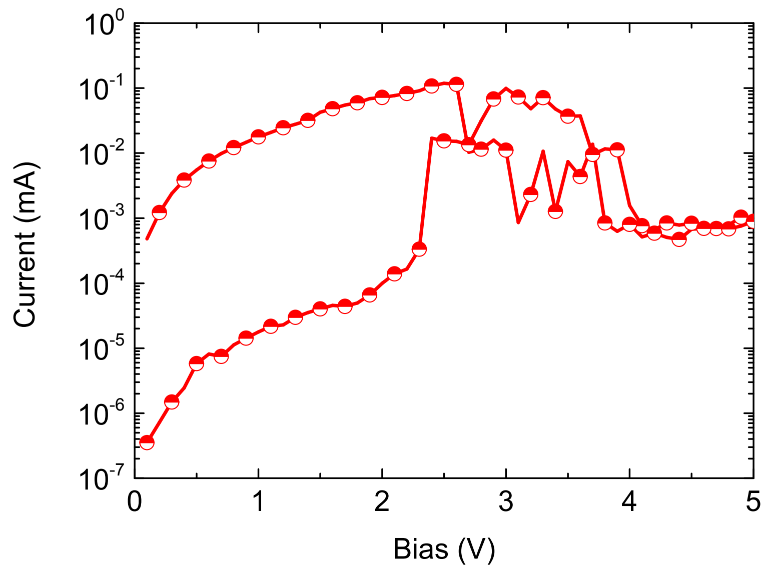

Figure 6.4 I-V sweep characteristics of the MTP TE ORS. Threshold voltage is about 2.5 V with an NDR spanning from 3.5 to 5 V. ON/OFF ratio is about 10^3 at 1 V.

6.1.5 Memory Retention Measurement

The ON state of a switched ON device stored in a glove box was not altered over a duration of 4 weeks.

6.1.6 LCR Spectroscopy

For ON and OFF state the full LCR spectrum was recorded. It clearly shows the transition of an ohmic to capacitive behaviour following the switching OFF. For the results see figure 6.5.

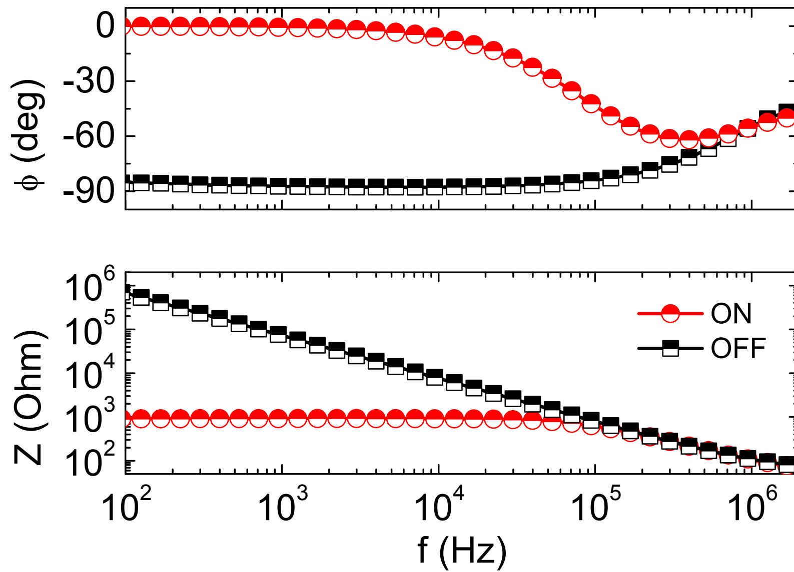

Figure 6.5 Phase and impedance spectrum for OFF (half-filled circles) and ON state (half-filled squares) of the MTP TE ORS.

Impedance analysis was performed with previously described parameters and ECD. The results are given in table 3. As expected the ON/OFF switching can be attributed to a change in the shunt resistance R_{SH} whilst series resistance R_s and capacitance C remain almost constant. In absolute numbers R_{SH} shows an all-over reduction by three orders of magnitude when compared to the reference PMMA device but other than that the values show a comparable trend.

Table 3 Results for impedance spectroscopy of ON and OFF state ITO/PMMA/Au MTP ORS. The uncertainty shown is solely of the fit. The fitting routine used was Levenberg–Marquardt. As expected the R_S changes only insignificantly and the capacitance for ON and OFF state is almost identical. The main contribution to ON/OFF switching is the shunt resistance, a strong indicator for filamentary switching. The uncertainty of the fit for the OFF state is higher due to higher noise in the spectrum

	R_{SH} (Ω)	R_S (Ω)	C (nF)
ON	(849±0.3)	(49±0.3)	(2.00 ±0.01)
OFF	$(8.1\pm0.5)*10^5$	(50±5)	(2.1±0.05)

6.1.7 TOF-SIMS Spectrometry

The SIMS analysis of the MTP TE device turned out to be a difficult task as the holes in the top electrode lead to a strong superposition of the PMMA signal and ITO signal from the bottom of the device and the signal from the top (gold ions), see figure 6.6. This clearly shows that the film is not uniform (as previously shown using SEM, figure 6.2). As the functionality of the device was demonstrated nevertheless this is not directly a drawback.

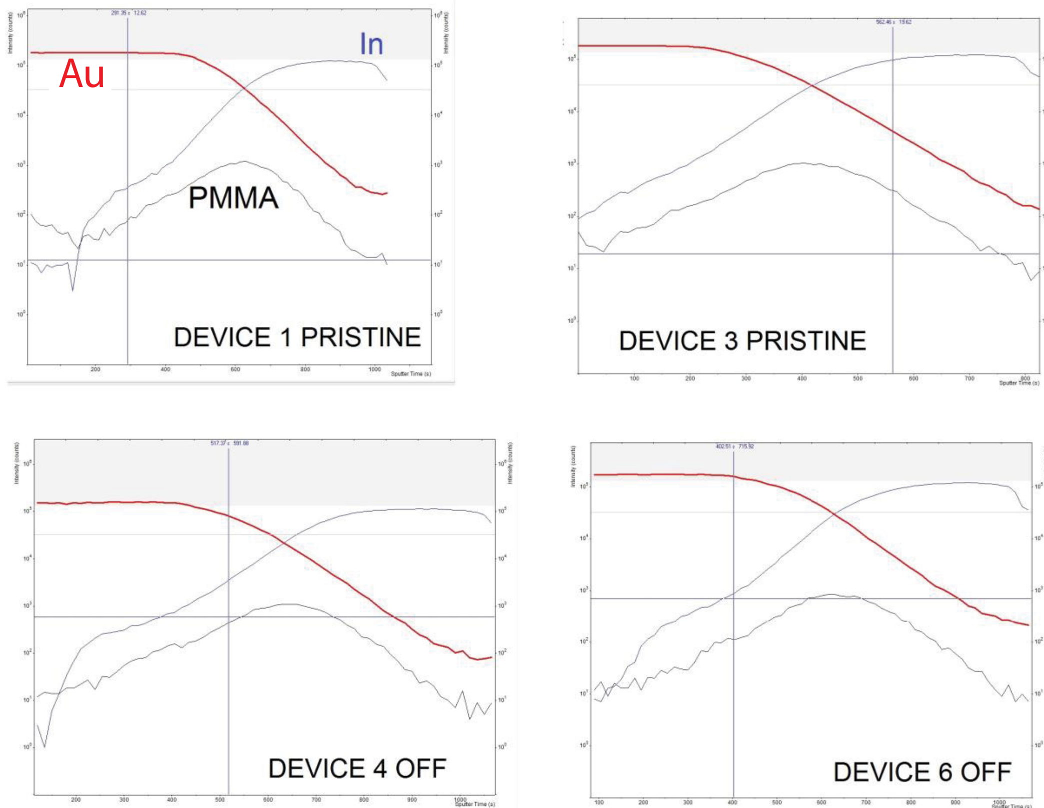

Figure 6.6 TOF-SIMS reconstruction of the interface for MTP TE ORS. There is a dominant signal from the bottom of the device over the active layer (PMMA) and some signal intermixing from BE (ITO) and TE (gold). A clear reconstruction of the interfaces was therefore not possible.

7 Laminated ORS

7.1 Fabrication of Au/PMMA/Au ORS via Lamination

A different approach to fabricate ORS is lamination. In this method top and bottom half of the device are fabricated separately and then laminated together using heat and pressure. Like MTP this fabrication method is related to roll-to-roll (R2R) fabrication that recently has gained a lot of attention in different areas of semiconductor industry[102].

7.1.1 Fabrication of Half ORS Cells

The top and bottom half are fabricated symmetrically with respect to the active layer. A flexible substrate, Kapton HN500 (DuPont) was chosen as it shows high stability with respect to solvents and high temperatures. The foil was cut into wafer-sized pieces, cleaned according to standard procedure. The cleaned substrate were mounted on PDMS covered glass that acts as support for spin coating. In the following step silver was deposited in the VDD at a base pressure of 1*10-6 mbar at a rate of 1 nm s-1 resulting in a 70 nm thick layer. The so prepared patterned substrates were O_2-plasma etched for 30 seconds at 50% in order to increase wettability and PMMA was spin-coated on each half of the device resulting in a layer thickness between 160 nm and 220 nm (confirmed by AFM) for concentrations of 30 g/L to 50 g/L PMMA in toluene.

7.1.2 Fabrication of PDMS Support Substrates

Processing flexible substrates with standard methods usually exhibits difficulties due to the flexibility. It is therefore advised to mount the foil on a supporting substrate. PDMS allows for an intimate contact between substrate and foil and allows for complete and clean removal after processing. First PDMS is mixed 1:10 (curing agent to silicon base) and degassed in an exicator for about 30 min to remove air bubbles. The resulting PDMS is then diluted using n-hexane 50:50 (by volume). This results in a thin viscose liquid that can be easily spin-coated on glass substrates using high speeds (around 5000 rpm gave the best results). Subsequently the PDMS covered glass substrate is annealed at 170°C to remove residual solvents for 10 min.

7.1.3 Lamination of ORS

The completed half devices are laminated using heat and pressure. First a working window was obtained, where functioning devices could be fabricated. If for example heat and pressure are too high the devices are short circuited, if either is too low the devices are not mechanically stable and delaminate.

Careful evaluation of temperature (T, °C) and pressure (p, bar) was necessary in order to produce devices that have a firm contact between bottom and top half but avoiding short-circuiting the device due to too high temperature and/or pressure. By variation of both process parameters a working window was established: 90°C $< T <$ 95 °C (literature values for T_g=105°C) and 20 bar $< p <$ 30 bar (see figure 7.1).

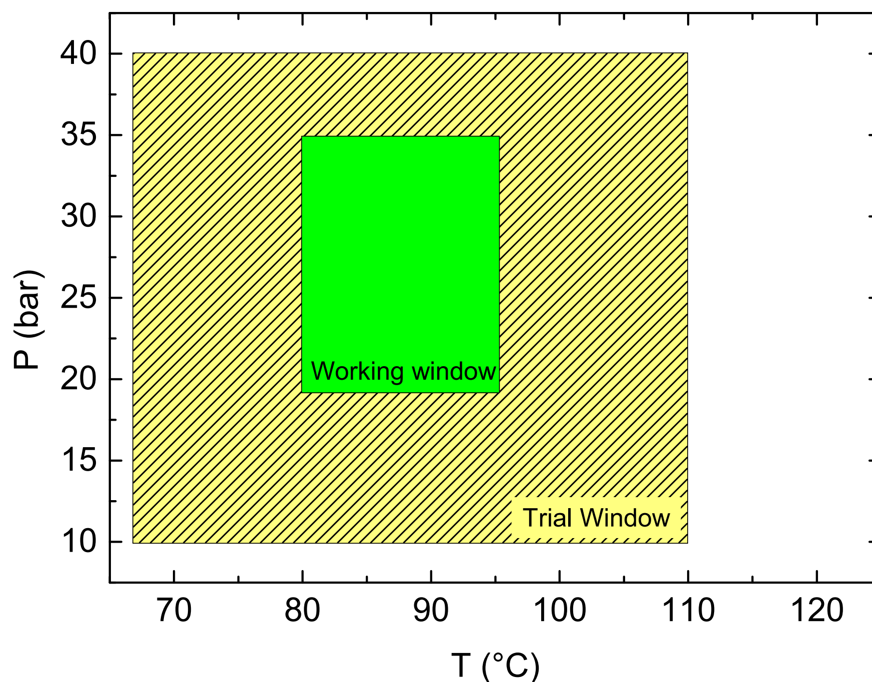

Figure 7.1 working window for lamination with respect to temperature and pressure. Inside the working window the lamination procedure yielded working laminated devices. If the pressure or temperature is chosen too low the devices delaminate, if they are too high the devices are short-circuited.

For the lamination procedure two metal blocks were pressed together using disk-springs. The force can be adjusted by the compression of the springs, pressure is calculated by dividing the force by the full device area. The whole device is held under constant temperature on a hot plate, figure 7.2. After approximately 10 minutes the lamination block is cooled down to room

temperature and the device can be removed. The resulting devices are mechanically stable and not short circuited. An example is shown in figure 7.3

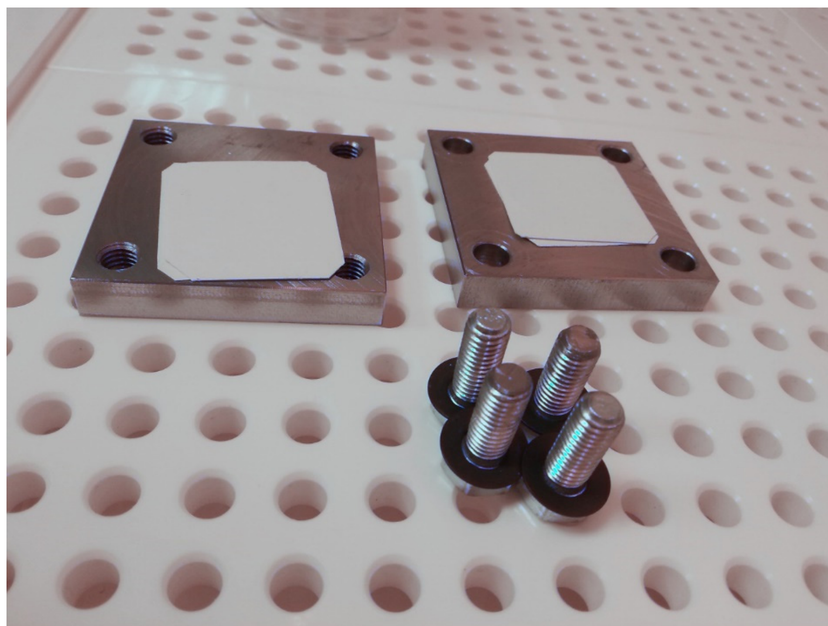

Figure 7.2 lamination device. The metal blocks are held together by four screws. Spring disks can be seen on the screws.

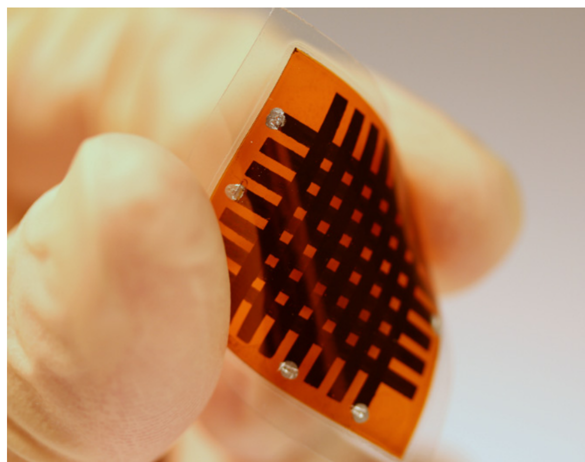

Figure 7.3 Laminated ORS in crossbar structure.The device structure is Kapton/Ag (70 nm)/PMMA (220 nm)| PMMA (220 nm)/Ag (70 nm)/Kapton.

7.2 Electrical Characterization

The Kapton was carefully removed using a scalpel to expose the electrodes. Adhesive silver was applied in order to guarantee a good electrical contact. All characterization was carried out under glove box Ar atmosphere (O_2, H_2O < 1 ppm) using an Agilent B1500A parameter analyzer contacted by tungsten needles on a probe station.

7.2.1 Conditioning Procedure

Conditioning consisted of a single 0-13 V sweep. The device was initially in OFF state but switched on at increased bias (figure 7.4). A CC was set as previously fabricated devices had shown to be sensitive to high current levels at high conditioning bias resulting in recurring breakdown.

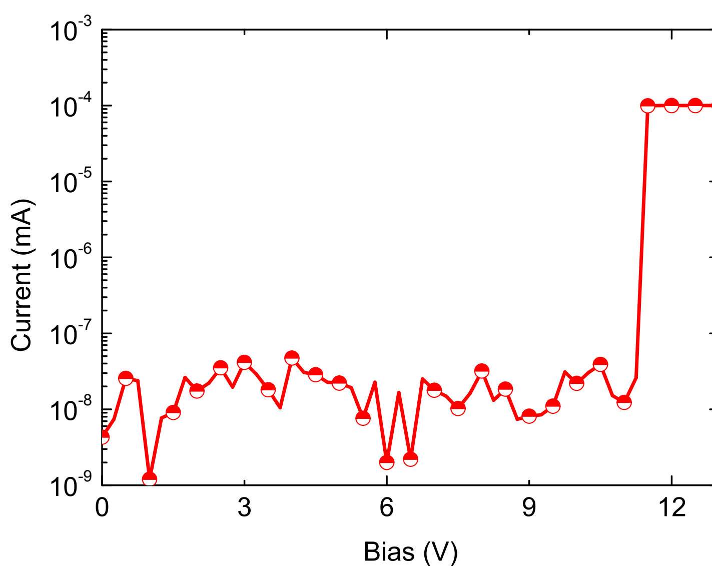

Figure 7.4 conditioning sweep of laminated ORS. A single sweep from 0-13 V established switching

7.2.2 Memory Sweep Characteristics

The I-V characteristic is shown in figure 7.5. The threshold voltage lies around 3 V and is as such comparable to the standard device. ON/OFF ratio however is poor in this devices and did not exceed 10^2 at 1 V. The NDR was not well pronounced and switching repeatedly failed and the device needed conditioning sweeps repeatedly. It was concluded that the high pressure and elevated temperatures necessary for reliable mechanic stability are not suited to fabricate electrically stable and reliable ORS.

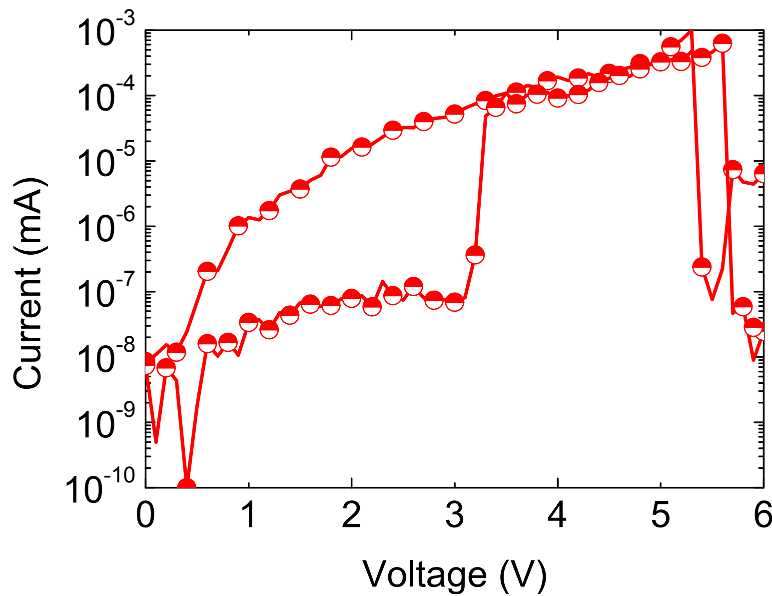

Figure 7.5 I-V characteristics under sweep. The switching however was not reliable, the NDR is not well pronounced and the ON/OFF ratio is about 100 at 1 V.

8 ORS on Super-Thin Substrate Mylar1.4

Recently new form factors, e.g. devices that bend or stretch or can conform to surfaces, especially skin, have gained a lot of attention[68,103]. Processing on ultrathin substrates like Mylar1.4 (DuPont Teijin Films) poses additional challenges for processing, e.g. poor mechanical or chemical stability.

The flexible substrate Mylar1.4® CW02 is a PET film initially designed for wound capacitors. It has a film thickness of 1.4 µm, an RMS surface roughness of 26 nm and a maximum roughness of 700 nm[104]. The substrate was obtained from Pütz Folien GmbH[105].

8.1 Fabrication of Metal/Organic/Metal ORS on Super-Thin Substrates

Since spin-casting did not seem applicable for this type of device the organic semiconductor tris(8-hydroxyquinolinato)aluminium (Alq_3) was chosen as organic layer as it can be deposited using a VDD.

For this device Mylar1.4 was mounted on PDMS coated glass slides and cut to the right dimensions. The foil was carefully cleaned by rinsing with propanol and blow-dried under N_2. As BE silver was deposited under a base pressure of $1*10^{-6}$ mbar at a steady rate of 1 nm s^{-1} resulting in a 70 nm thick layer. As active layer Alq_3 was deposited at a rate of 0.1 nm s^{-1} at a base pressure of $7*10^{-7}$ mbar resulting in 270 nm. Eventually the TE was deposited, silver again under above noted conditions to result in a 100 nm layer. Between the deposition steps vacuum was not broken. The devices are measured in glove box under Ar inert atmosphere.

During measurement the devices were attached to the supporting substrate. When they are removed from it one obtains a very thin, light and highly flexible device that easily adheres and conforms to thin structures, see, for example, figure 8.1.

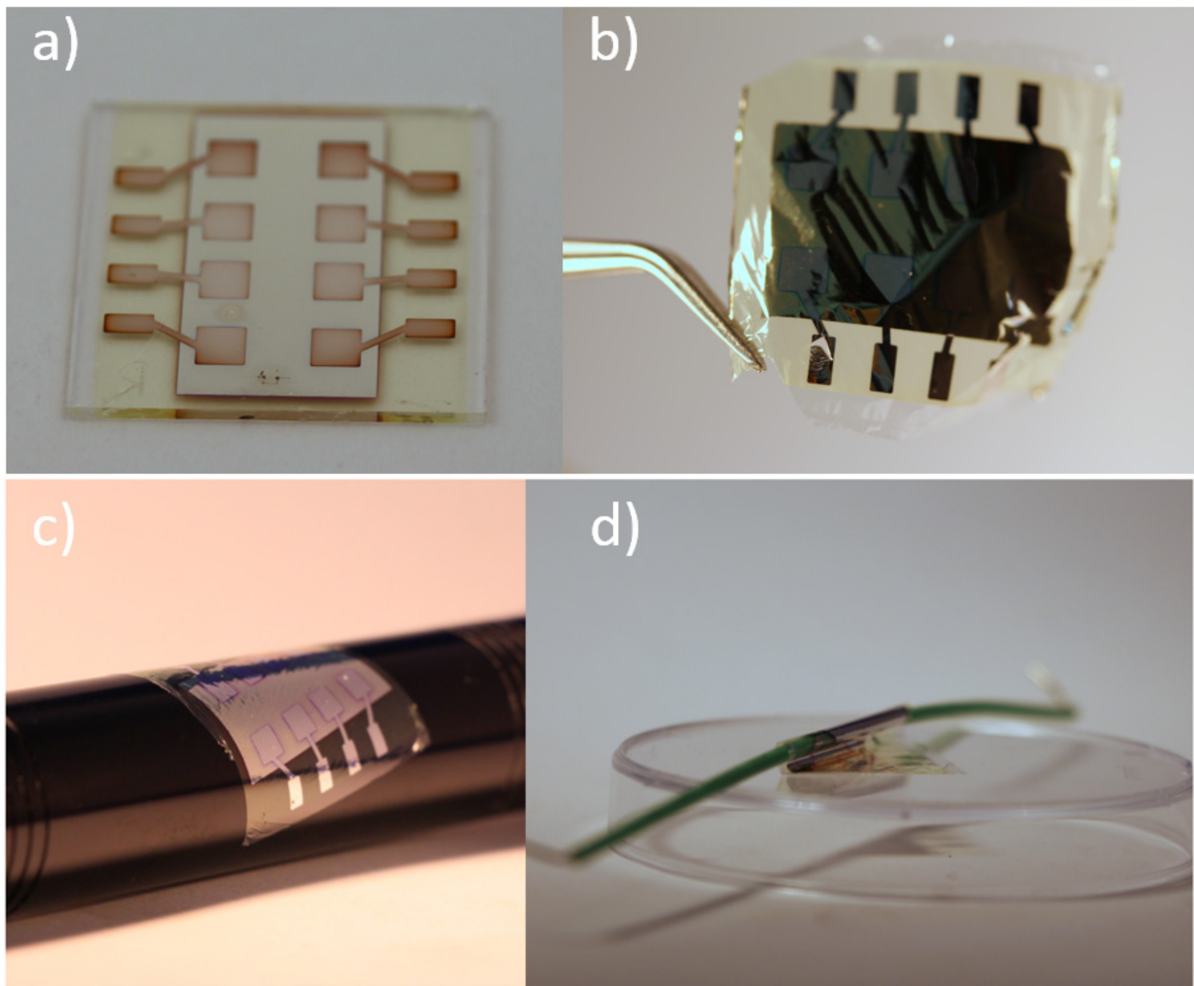

Figure 8.1 An ORS on super thin Mylar1.4 substrate. a) the ORS is mounted on the supporting substrate. b) after removal from the support substrate as a free thin film. The device is so thin and flexible it easily conforms to thin structures, shown in c) and d).

8.2 Electrical Characterization

8.2.1 Conditioning Procedure

The device is initially in its OFF state and conditioning was a straight-forward procedure. The results are depicted in figure 8.2.

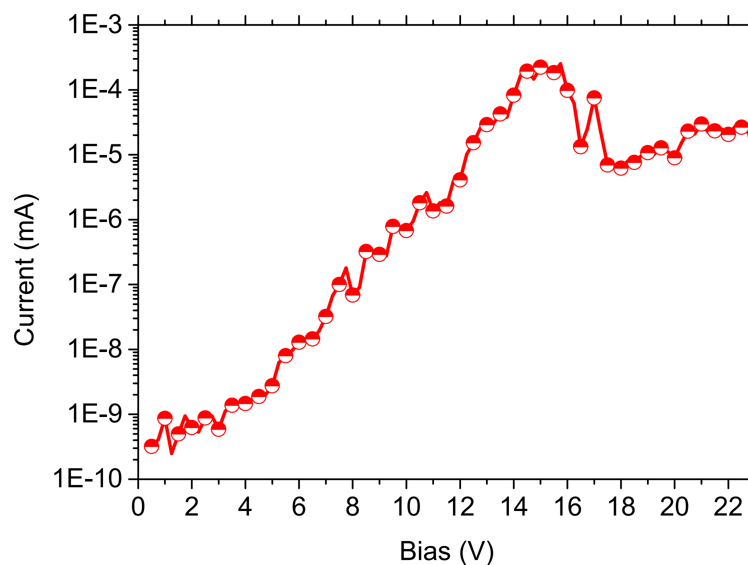

Figure 8.2 Conditioning sweep of Ag/Alq_3/Ag device. The device was initially in its OFF state but was switching ready after a sweep up to 23 V.

8.2.2 Memory Sweep Characteristics

I-V sweep characteristics were obtained (figure 8.3). The threshold voltage is about 3 V with an NDR region spanning from 3.5 V to 4.5 V. ON/OFF ratio is about 10^5 at 1 V. The absolute current levels (at equal electrode area of 3x3 mm^2) are higher as in the PMMA reference device since Alq_3 is a semiconductor and exhibits higher intrinsic conductivity. All measurements were taken whilst the device was still mounted on the supporting substrate.

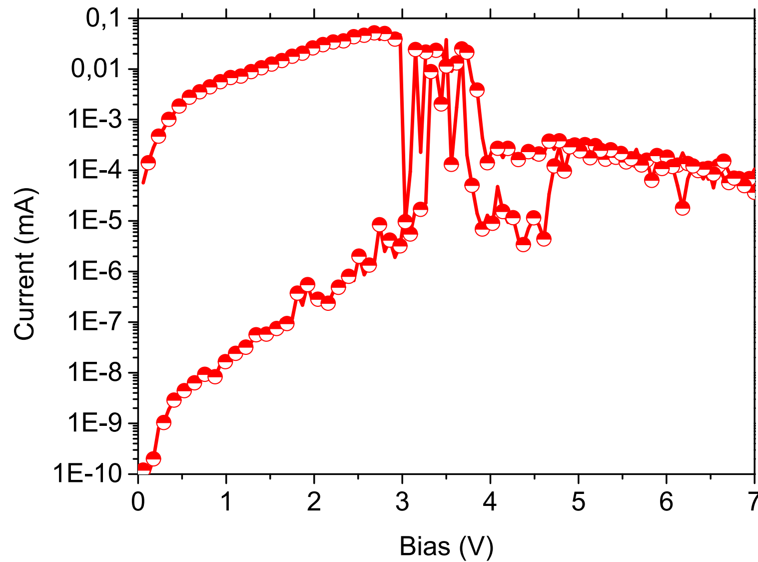

Figure 8.3 I-V sweep characteristic for metal/Alq_3/metal ORS on ultrathin substrate Mylar 1.4. The device exhibits a threshold-voltage of 3 V and an NDR between 4 and 5 V. The ON/OFF ratio is about 10^5 at 1 V. The current levels of this device are high compared to the PMMA reference device which is attributed to the higher intrinsic conductivity of the semiconductor Alq_3.

8.2.3 LCR Spectroscopy

Impedance analysis was performed with previously described parameters and ECD. The results are given in table 4. As expected the ON/OFF switching can be attributed to a change in the shunt resistance R_{SH} whilst series resistance R_s and capacitance C remain almost constant.

Table 4 Results for impedance spectroscopy of ON and OFF state Ag/Alq_3/Ag ORS on super thin-substrate. The uncertainty shown is solely of the fit. The fitting routine used was Levenberg–Marquardt. As expected the R_S changes only insignificantly and the capacitance for ON and OFF state is almost identical. The main contribution to ON/OFF switching is the shunt resistance, a strong indicator for filamentary switching. The uncertainty of the fit for the OFF state is higher due to higher noise in the spectrum

	R_{SH} (Ohm)	R_S (Ohm)	C (nF)
ON	$(1.1\pm0.1)*10^4$	(42 ± 0.2)	(1.12 ± 0.04)
OFF	$(9.2\pm0.1)*10^6$	(48 ± 3)	(1.13 ± 0.05)

9 Nanoscale Organic Resistive Switch

As mentioned in the introduction downsizing is a major driving force of the semiconductor industry. It is as such of great academic and engineering interest to explore the lower size limit of a technology. For inorganic resistive switches downscaling to 20 nm was successfully demonstrated[106].

9.1 Fabrication of Nanoscale ORS

The small sizes prohibit fabrication via the previously reported methods, i.e. shadow-mask evaporation or MTP. To fabricate devices with features in the nm regime e-beam lithography and a lift-off process was utilized[4].

Devices fabricated had Cr/Au/SU-8/Au or Cr/Au/SU-8/Cr structure. SU-8 is an epoxy-based negative photoresist by MicroChem[107] that exhibits similar electrical properties to PMMA. The device layout is depicted schematically in figure 9.1. On the left hand side the stack-structure for a Cr/Au/Su-8/Au device is given. The Cr layer acts as adhesion promoter for the gold layer and is omitted in the schematic. The pixels are formed by the intersection of TE and BE.

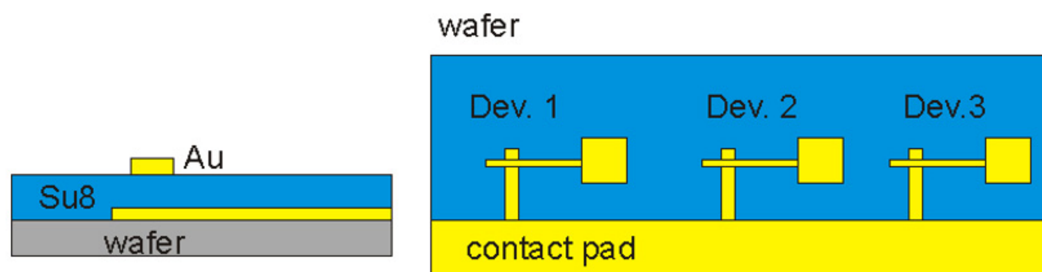

Figure 9.1 Schematic of the Nano-ORS with gold/SU8/gold stack structure. On the right-hand side the principle layout is depicted. The intersection of the electrode lines form devices of different electrode area. Larger contact pads are processed as well to allow contacting the devices using the standard tungsten needles.

[4] Device fabrication and SEM characterization was performed by Johannes Kofler at NTC Weiz.

Different electrode widths, electrode materials and active layer thicknesses were explored. Details are given in table 5. The devices are given different designations *Nano1* to *Nano4* to address them in the text.

Table 5 Device structure and electrode dimensions for Nano-ORS. Given are the line widths of the electrodes (multiple possible on one substrate) and the layer thickness (approximately) of the SU8 layer

Device	Structure	Line widths (nm)	SU8 thickness (nm)
Nano1	Cr (4 nm)/Au (30 nm)/SU8/Au (30 nm)	20	180
Nano2	Cr (4 nm)/Au (30 nm)/SU8/Au (30 nm)	20	180
Nano3	Cr (4 nm)/Au (30 nm)/SU8/Cr (30 nm)	20	180
Nano4	Cr (4 nm)/Au (30 nm)/SU8/Au (30 nm)	1000, 500, 200, 100	30

The reduced device dimension pose some challenges for the characterization. Contact was obtained as previously reported using tungsten needles on a probe station.

9.2 Nanoscale ORS 1

The structure of the ORS Nano1 was Cr (4 nm)/Au (30 nm)/SU-8 (180 nm)/Au (30 nm). The line width of TE and BE are 20 nm each resulting in an active area of (20x20) nm^2. A pixel is shown in figure 9.2.

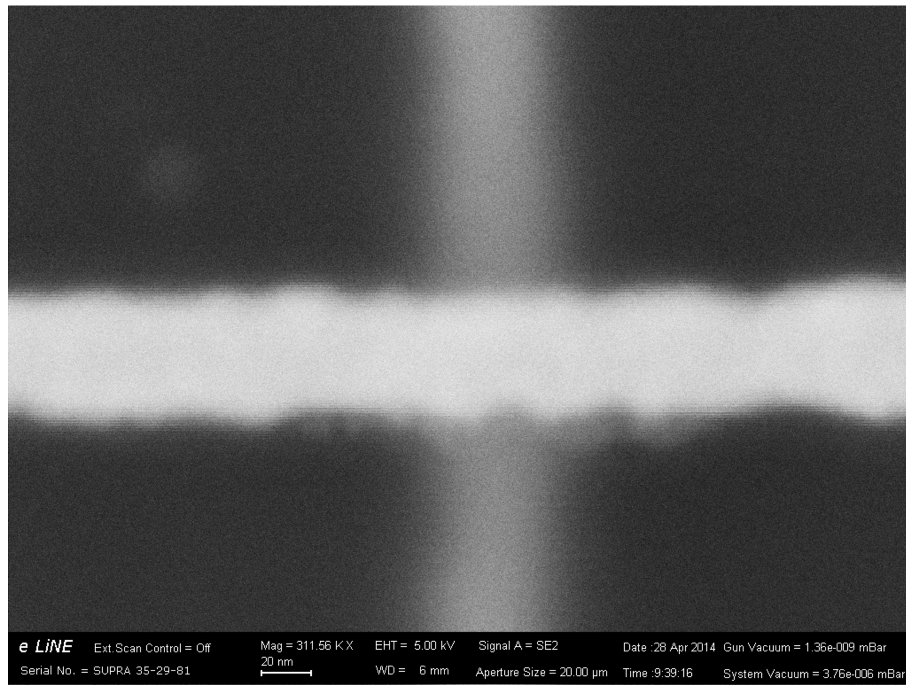

Figure 9.2 Memory pixel of Nano1. The intersection of TE and BE each of width 20 nm is shown in a SEM image.

9.2.1 Conditioning Procedure

Interestingly the conditioning of the device proved rather cumbersome. Since the device structure is similar to previously conditioned Au/PMMA/Au devices a conditioning voltage of about 15 V was expected but it turned out that voltages as high as 100 V were necessary. The drastically decreased active area of the device makes it less likely to contain defects. These defects presumably lead to a locally enhanced electric field which act as strong driving force for the metal drift. Since the high bias would cause thermal destruction upon switching it was necessary to gradually increase the CC in steps of only a few ten nA. The conditioning procedure is depicted in figure 9.3 for Nano1 with an electrode width of 20 nm. The CC is gradually increased after every sweep and a bias as high as 60 V was necessary. A discharge peak can be seen that gradually vanishes. When the discharge peak vanishes from the I-V characteristics a filament is apparently formed and the device is ready to switch.

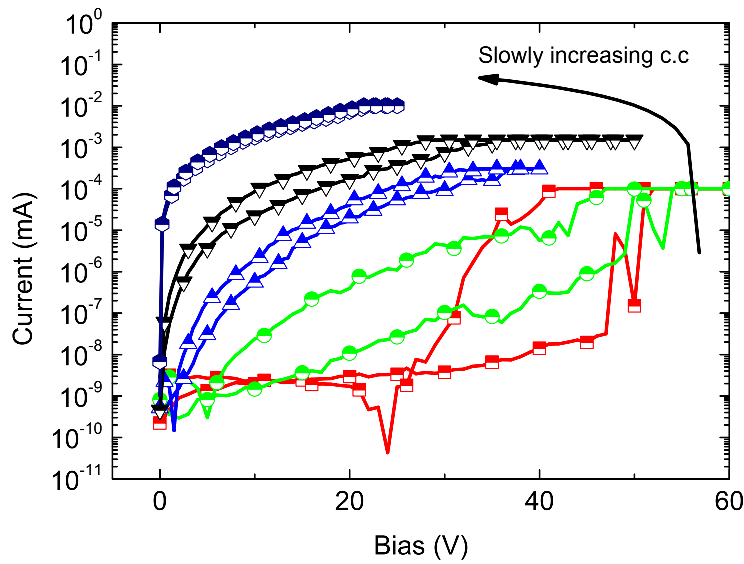

Figure 9.3 Conditioning procedure of ORS Nano1 and a device of 20 nm electrode width. The CC is increased gradually after each sweep (only a few sweeps are shown for clarity). The initially appearing peak at reverse sweep direction decreases after each subsequent sweep. When the peak does no longer occur a filament is apparently formed and the device is ready to switch.

9.2.2 Memory Sweep Characteristics

After conditioning the device was attempted to switch in I-V sweep mode. The initial results were very promising as the ON/OFF ratio exceeded expectations by reaching 10^6 at 1 V, mostly due to the very low OFF current limited by the small active area of (20x20) nm^2. The result is shown in figure 9.4. As can be clearly seen the threshold voltage was shifted to higher values (a shift of about 4 V leading to a threshold of 7 V) relative to the reference PMMA ORS.

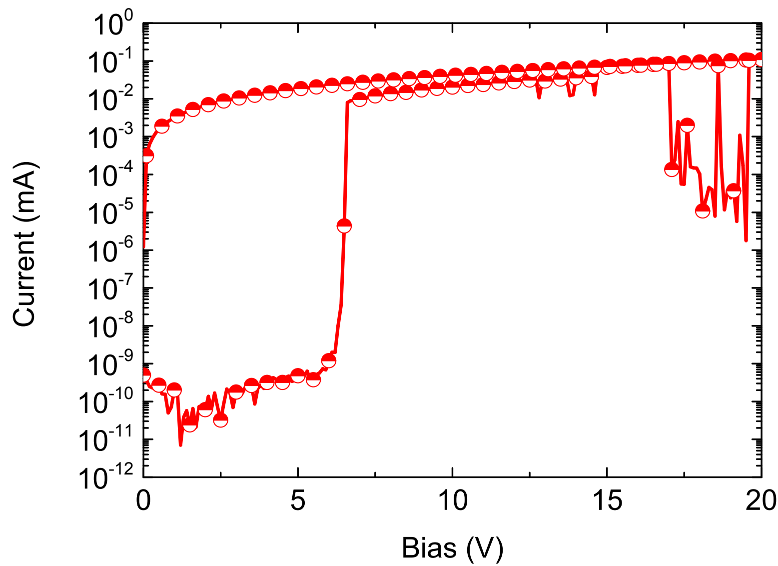

Figure 9.4 I-V sweep of ORS Nano1 and an electrode width of 20 nm. The threshold voltage is shifted to higher values at around 7 V. The ON/OFF ratio is >10^6 at 1 V

In order to investigate the shift of threshold voltage the device was investigated under the SEM. Small gaps in the support line leading to the intersection were discovered, most likely due to a process instability during the e-beam lithography. The higher resistance could be explained by such gaps in the supply line being not completely closed as were observed in SEM image figure 9.5. Apparently the gaps in the supply line are closed during conditioning but do not form a perfectly conducting structure thus adding to the resistance.

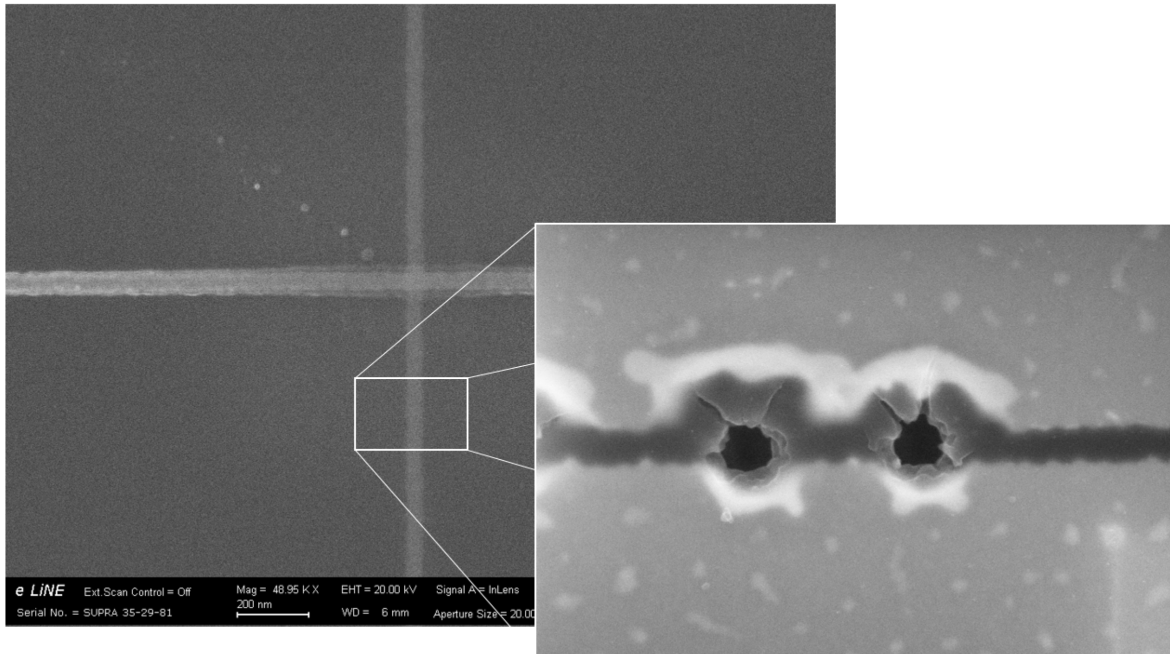

Figure 9.5 Schematic explanation of high threshold voltage due to additional resistors formed by gaps in the supply line. In the SEM image gaps in the line structure were observed, most likely due to a drift in the e-beam during lithography. During conditioning the gaps are apparently closed but do not form a well conducting structure

The devices on the ORS Nano1 showed stability issues where the ORS would be irreversibly damaged during sweep operation. The SEM analysis showed that the whole electrode intersection was ablated due to thermal stress leaving no conducting structure behind (figure 9.6). The small structure apparently poses as a strict constrain on the switching power.

It was possible to analyse a switched ON device, depicted in figure 9.6. The structure in the centre of the active area is most likely a formed filament.

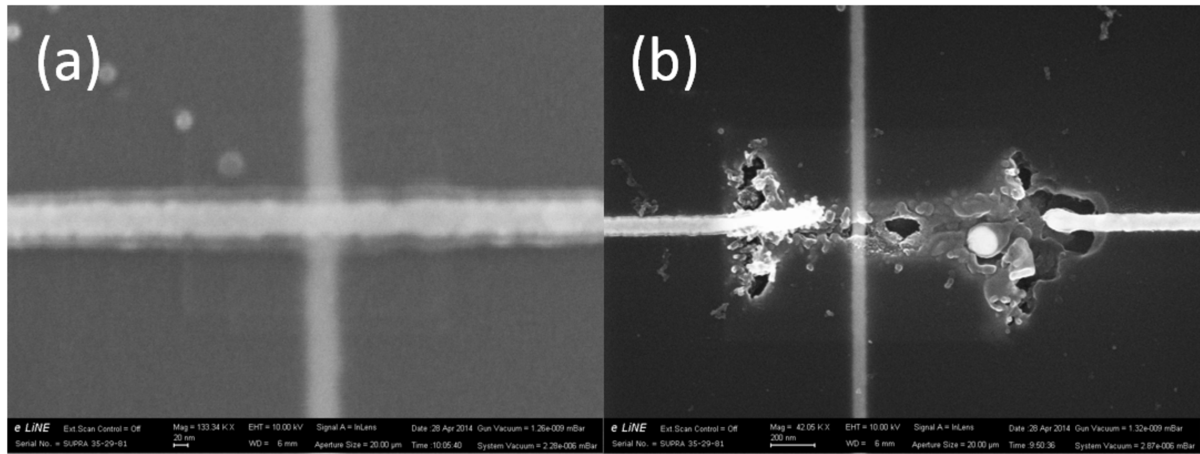

Figure 9.6 SEM images of Nano1 ORS in two different conditions. Healthy pre-switching ORS (a) compared to a thermally destroyed ORS (b) that failed during sweep operation. The electrical failure seems to ablate the whole TE in the vicinity of the crosspoint. Local temperatures seem to be high enough to destroy the active layer (SU-8) as well.

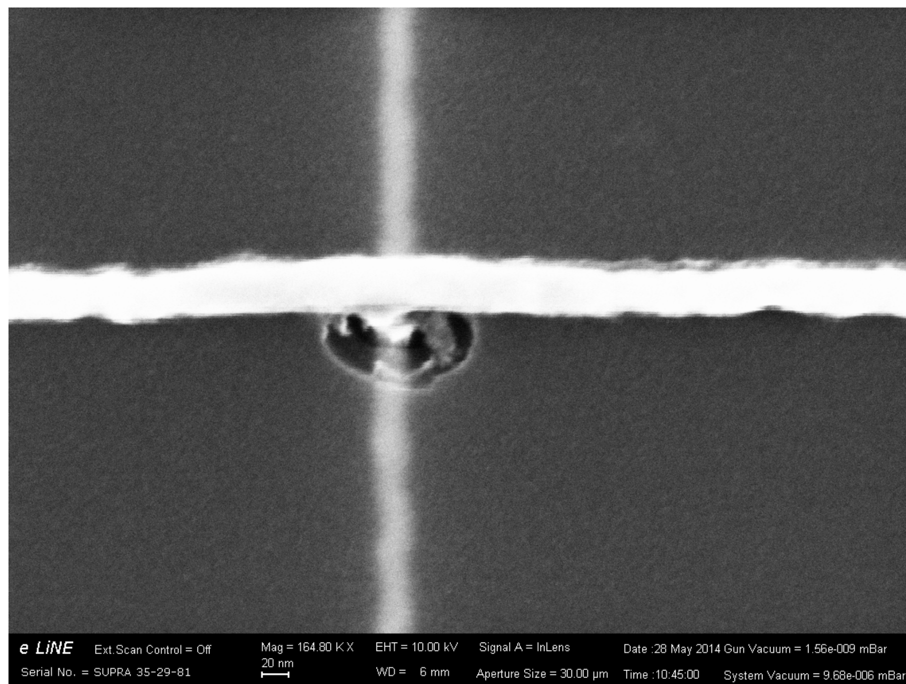

Figure 9.7 SEM image of Nano1 ORS. The electrode width is approximately 20 nm resulting in an active area of (20x20) nm². The image shows the active area of a switched ON working device. In the centre of the pixel a structure is visible that presumably is a filament of the ON state device.

9.3 Nanoscale ORS 2

In order to determine if the increased threshold voltage was a side-effect of build-errors in the support line another set of devices was fabricated with the same process parameters and structure. The width of the electrodes was slightly increased to 50 nm resulting in a (50x50) nm² active area.

9.3.1 Conditioning Procedure

Conditioning of the second series nanoscale ORS (Nano2) was similar to previously shown conditioning procedure and is shown in figure 9.8. By gradually increasing the CC after each sweep and bias levels up to 100 V the discharge peak vanished and the device seemed ready to switch.

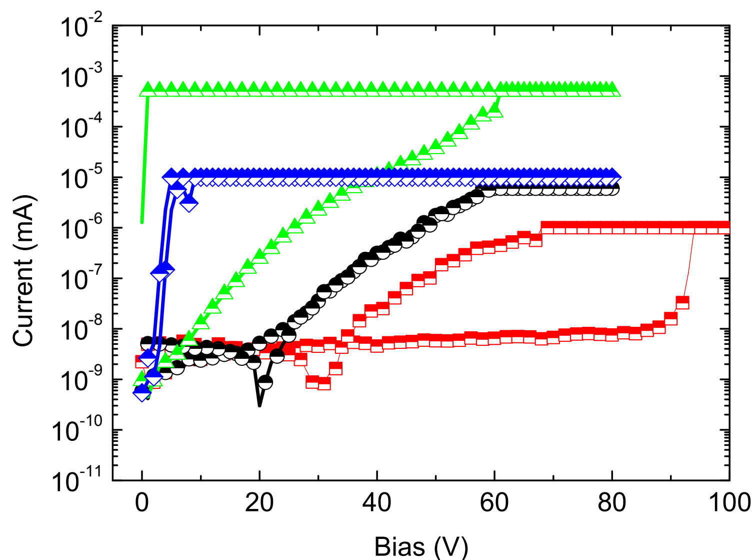

Figure 9.8 Conditioning of ORS Nano2 with a structure of Cr/Au/SU8/Au. The device had an active area of (20x20) nm². Under gradually increasing CC the discharge peak vanishes and the device is ready to switch.

9.3.2 Memory Sweep Character

The memory could not be switched to ON as all devices were destroyed during sweep operation. This could indicate that in previously switched devices the horizontal gaps in the supply line acted as intrinsic current compliance protecting the device during filament formation. As no

such gaps were discovered in Nano2 a high current would be able to thermally overload the device.

When investigated under SEM all electrodes were ablated in devices where switching was attempted as shown in figure 9.9.

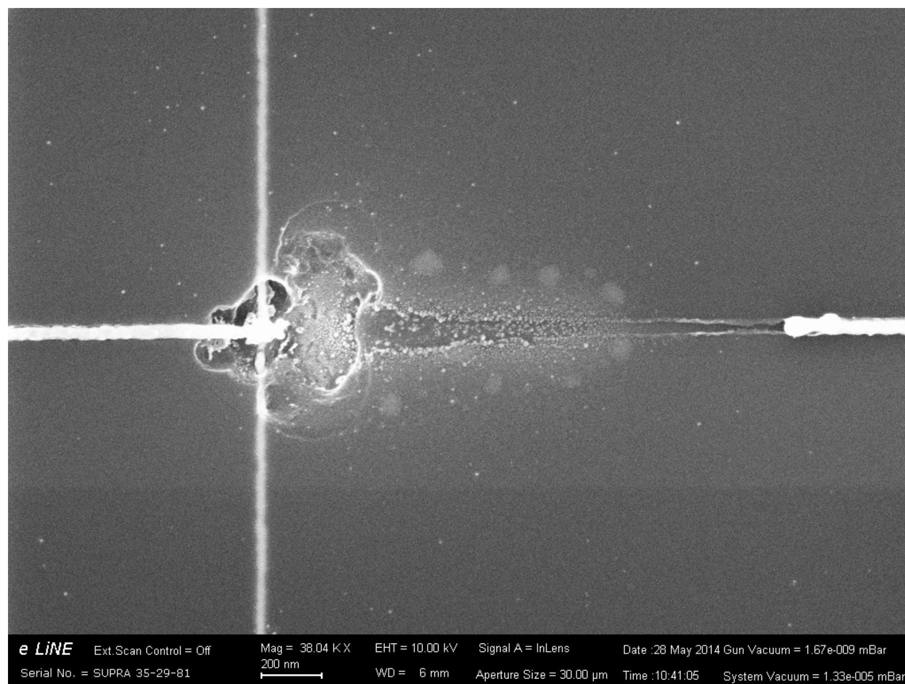

Figure 9.9 SEM image of the thermally destroyed active area of ORS Nano2. Apparently the device exhibited massive current overload on switching attempt and the electrode is ablated.

9.4 Nanoscale ORS 3

From series 1 and 2 of the nanoscale ORS it is apparent that thermal overload of the device destroys the TE. In an attempt to overcome this issue a device with chromium TE was fabricated. This should result in a device that is less susceptible to melting of the TE as chromium has a higher melting temperature.

9.4.1 Conditioning Procedure

Conditioning was successful with the same procedure as noted above (see figure 9.10).

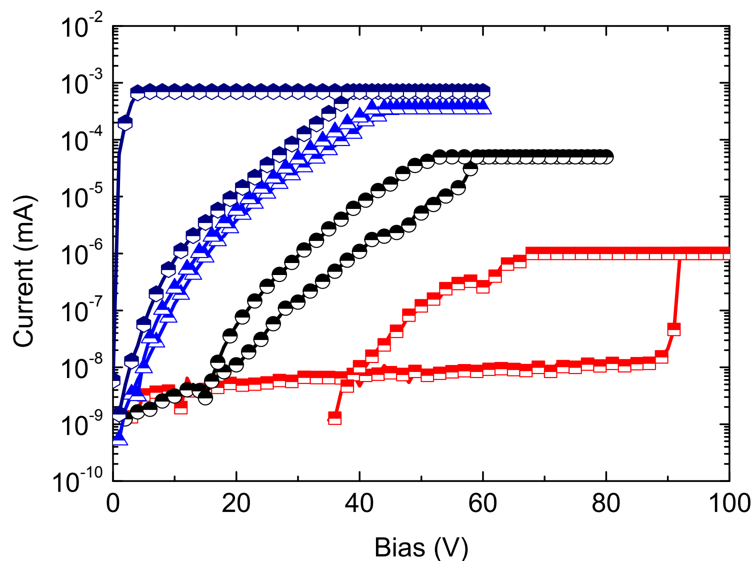

Figure 9.10 Conditioning procedure of ORS Nano3. After a few conditioning sweeps with increasing CC switching could be obtained

9.4.2 Memory Sweep Characteristics

For this device reliable switching was finally possible in I-V sweep mode. The result of a full I-V sweep is shown in figure 9.11. The ORS has a threshold voltage of about 3 V (comparable to the reference PMMA device), the NDR extends from 3.5 to 5 V and the ON/OFF ratio is about 10^8 at 1 V readout bias, which is higher than in the reference PMMA device. This behaviour can be explained by the area-limited current in the OFF state.

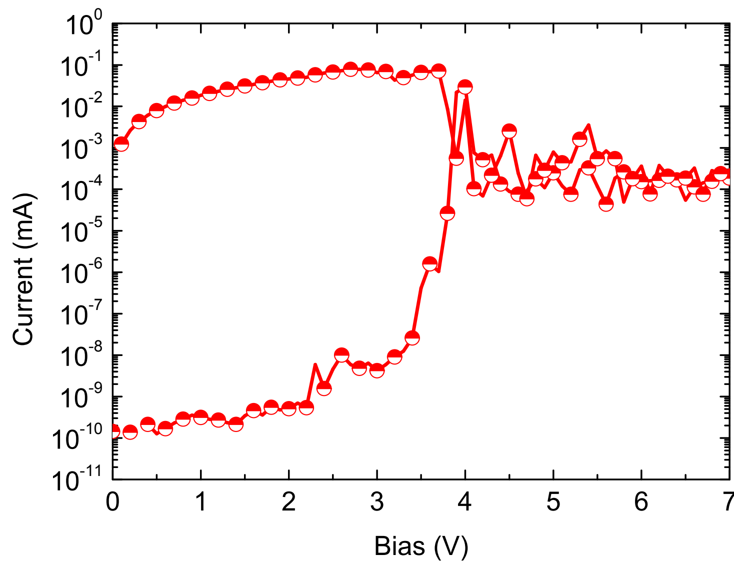

Figure 9.11 I-V sweep characteristics of nanoscale ORS 3 with the structure Cr/Au/SU8/Cr. Threshold voltage was about 3 V and the ON/OFF ratio is about 10^8 at 1 V.

9.4.3 LCR Spectroscopy

For the ORS Nano3 ON and OFF state impedance spectra were taken. The phase angle clearly shows a transition from ohmic to capacitive transition when the device is switched from ON to OFF (figure 9.12).

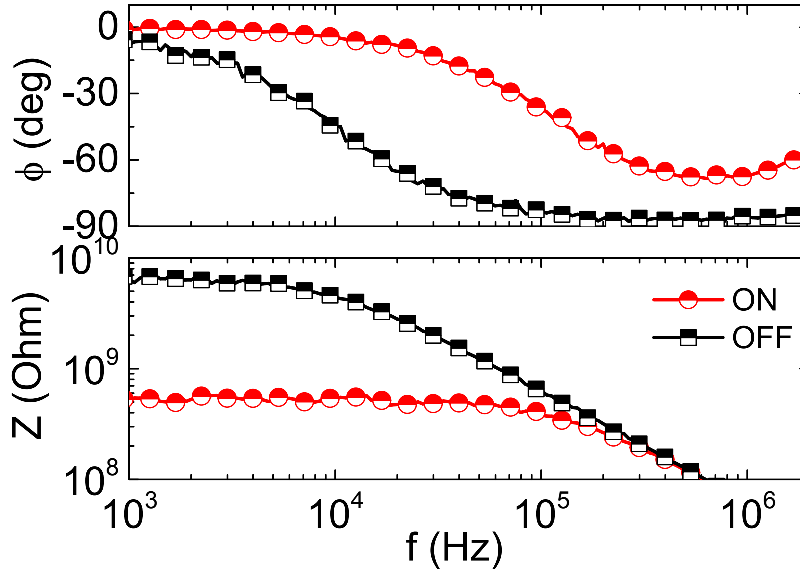

Figure 9.12 Phase angle and impedance over frequency for ON (squares) and OFF (circles) state of nanoscale ORS 3. The transition from ohmic to capacitive behaviour under switching OFF can be observed.

The impedance analysis yielded the values presented in table 6 for R_S, R_{SH} and C of the ECD. The analysis showed that again the switching is primarily facilitated through a change of shunt-resistance R_{SH} whilst C and R_S exhibiting almost constant values for ON and OFF state. The high resistance of the OFF state increased the noise level and thus the uncertainty of the measurement when compared to the reference PMMA device.

Table 6 Results for impedance spectroscopy of ON and OFF state Cr/Au/SU8/Cr nanoscale ORS. The uncertainty shown is solely of the fit. The fitting routine used was Levenberg–Marquardt. As expected the R_S changes only insignificantly and the capacitance for ON and OFF state is almost identical. The main contribution to ON/OFF switching is the shunt resistance, a strong indicator for filamentary switching. The uncertainty of the fit for the OFF state is higher due to higher noise in the spectrum

	R_{SH} (Ohm)	R_S (Ohm)	C (pF)
ON	$(2.2\pm0.07)*10^5$	(3200±300)	(2.5 ±0.2)
OFF	$(6.8\pm0.1)*10^8$	(3100±700)	(2.5±0.7)

9.5 Nanoscale ORS 4

Previously fabricated nano-ORS seem to fail at a certain point due to thermal stress that occurred during conditioning rather than switching. Since a critical field has to be applied in order to form a pre-filament[91] reducing the interlayer thickness seemed a reasonable next step. In ORS Nano4 the layer thickness was reduced to about 30 nm (an approximately 6-fold reduction from previous ORS) and different electrode widths of 1000 nm, 500 nm, 200 nm and 100 nm were used to form the pixels.

9.5.1 Conditioning Procedure

Initially the conditioning procedure looks very promising. The voltage associated with the critical field for pre-filament formation is clearly reduced (from about 100 V to 60 V) when compared to ORS with higher SU8 thickness. Unfortunately the conditioning regularly failed at current levels too low to indicate switching ability of the ORS. This is displayed in figure 9.13. Initially the CC can be increased from 10^{-6} mA to 10^{-4} mA. If the CC is increased further the device suddenly fails (triangles in the plot), indicating overload of the device.

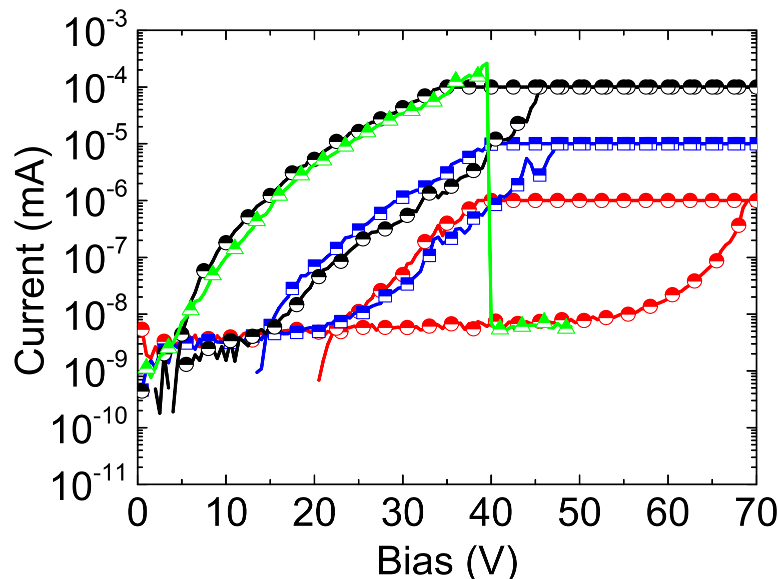

Figure 9.13 Conditioning of nanoscale ORS Nano4. Each sweep the CC was increased from 10^{-6} mA to 10^{-4} mA. The ORS were unable to sustain a current high enough to allow resistive switching (~10^{-3} mA) as it fails during the sweep (triangles). The lower critical voltage compared to thicker ORS devices e.g. Nano2 is visible from the early onset (about 60 V compared to 100 V).

9.5.2 Memory Sweep Characteristics

Next a critical lower limit for electrode line width for reliable memory operation was investigated. From the standard device it is known that dimensions of (3x3) mm^2 pose no problems. For the miniaturization line widths of 1000 nm, 500 nm, 200 nm and 100 nm were tested. Surprisingly only ORS with an electrode width of 1 µm could be switched reliably (figure 9.14), all smaller ORS failed under above displayed failure mode.

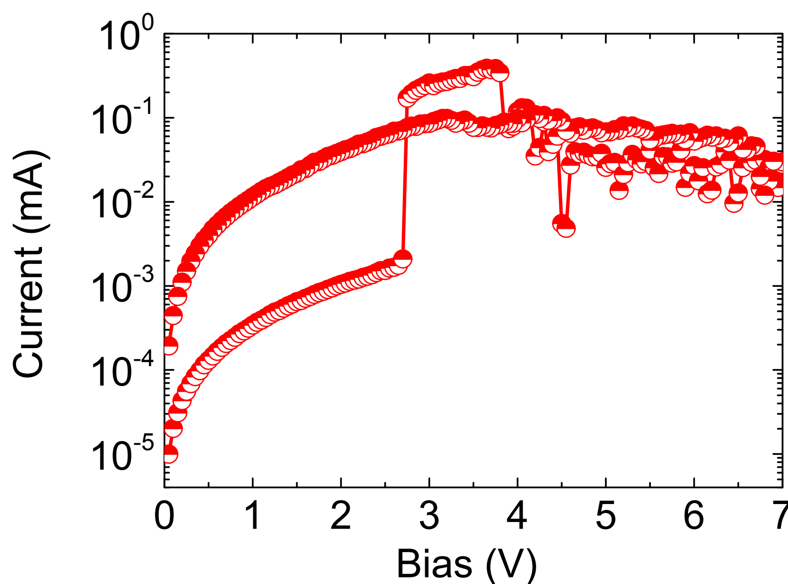

Figure 9.14 Bistability in ORS Nano4 with 1000 nm electrode width. The device exhibits a threshold voltage of about 3 V comparable to the reference PMMA ORS. The NDR is not well pronounced but extends approximately from 3.5 to 7 V. The ON/OFF ratio of this device was reduced and only reached about 10^2 at 1 V due to a very high OFF-current.

SEM images of the cycled devices were obtained to analyse the cause of electrical failure. From the obtained images it was again apparent that the devices thermally overload and the TE cracks or evaporates during the conditioning or switching attempt. First the successfully switched devices was analysed (figure 9.15). The image shows that the TE is intact. However a small "dent" exists in the top-right corner of the pixel that might explain the high OFF-current. Either during fabrication or conditioning the TE and/or the underlying SU8 seems to have been damaged. A comparison with a device that exhibited breakdown (figure 9.16) shows that in this case, as previously observed, the TE is destroyed most likely due to thermal overload. A large crack now separates the supply line (extends to the right side, shown in the inset) from the pixel.

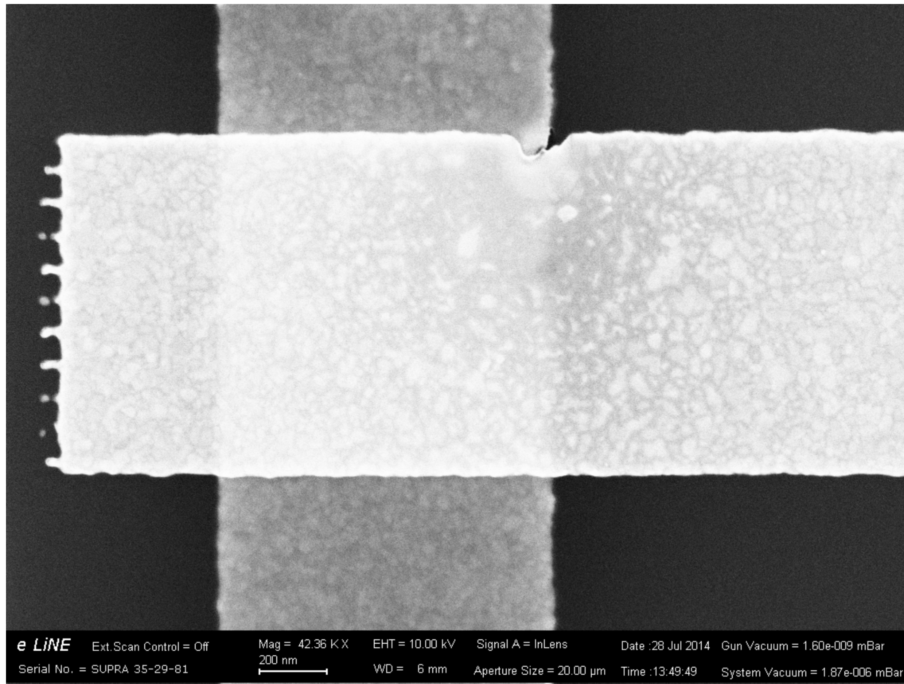

Figure 9.15 Nanoscale ORS Nano4 in a SEM image. The electrode width of the device is (1x1) µm. This device successfully switched in I-V sweep mode but the OFF-current was high. This might be attributed to a short-circuit path in the top-right corner of the pixel.

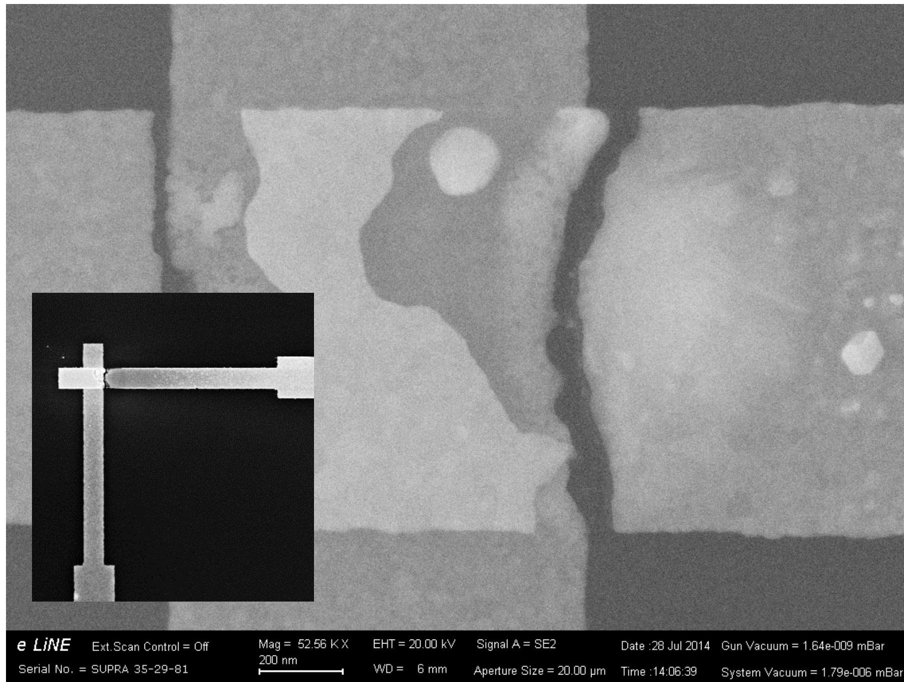

Figure 9.16 Nanoscale ORS Nano4 in a SEM image. The device had an electrode width of 1 µm. This device failed during conditioning. The destroyed TE is clearly visible. A crack separates the supply line (extends to the right as shown in the inset) from the intersection that forms the memory pixel.

All devices with an electrode width smaller than 1 µm showed similar images of destroyed electrodes in the SEM.

10 Summary and Conclusion

The switching in metal/PMMA/metal ORS has been demonstrated to be clearly of filamentary nature. This is supported by the I-V characteristics as well as impedance spectroscopy that show a transition of the phase angle from close to 0° in the ON state to close to -90° for the OFF state associated with a change in conduction mode from ohmic to space-charge-limited current.

The formation of so-called pre-filaments has been demonstrated by TOF-SIMS analysis. Those filaments are ready to switch upon the following sweep and their formation is closely related to the field strength applied over the organic layer. In most devices the field associated with the conditioning voltage is in the range of $E=U/d=15/(200*10^{-9})=65$ MV/m. Local fields might be much stronger as previously diffused metal atoms can form tips that greatly enhance the local field. Under this voltage a strong drift of metal ion from the TE occurs simultaneously to a counter-drift from the BE, as was shown by TOF-SIMS spectrometry of conditioned devices. The switching ON and OFF is mediated by a rather small local change of metal concentration close to the BE.

In the presence of reactive species, namely water vapour and oxygen the power necessary to degrade the filament is significantly altered. This points towards an electrochemical reaction that might be enabled by local high temperature due to Joule heating. After degradation of an active filament under reactive atmosphere and reintroduction of the OFF device into inert atmosphere the device is ready-to-switch without another conditioning procedure. This shows that not only a single but probably multiple filaments coexist in the active layer, as is likely due to the stochastic nature of filament formation. The fact that multiple filaments are active during switching is also strongly suggested by previous reports in literature were multiple hot-spots were recorded using an infrared camera[108] and conductive AFM studies[109].

The final experiment concerning the downsizing of the ORS puts forward a certain constrain concerning the shrinking of ORS. As demonstrated switching in devices of (20x20) nm^2 to (50x50) nm^2 is not easily possible as the heat cannot be transported away from the switching region fast enough and thermally overloads the active zone leading to a rapid and irreversible degradation of the filament close to the switching region. The form of the rupture and the form of the remaining electrodes hint that the material (here gold and chrome) liquefies or evaporates at a high rate. Of course heat dissipation[21] is not a problem that is unique for ORS but at the current stage of development and owing to the necessity of filament formation it poses a serious issue. Furthermore it can be expected that at a certain area the material available to form a

second filament when the previous filament (filaments) is completely erased as was shown in the TOF-SIMS data is not readily available in such small dimensions.

ORS based on metal/PMMA/metal sandwich structure clearly show advantageous features such as ease of processing under ambient temperature using a variety of fabrication methods, viz. vapour deposition, direct metal transfer, closely related to roll-to-roll fabrication technique, lamination or lithographic methods. The devices can be fabricated on a variety of rigid and flexible substrates as well as super thin polymer foil.

The single pixel exhibits excellent conditioning behaviour, stable switching patterns and long-term retention even when temporarily exposed to reactive atmospheres, i.e. water and oxygen. The ON/OFF ratio is better than most competing device structures in this class making metal/organic/metal resistive switches a very promising realization of resistive memory.

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