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Investigation of Organic Thin Film Transistors Using a Soluble Pentacene Derivative

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Supervisor:

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Abstract

Organic based electronics offers opportunities for the production of economical as well as efficient electrical components for a wide variety of applications reaching form large area flexible displays and chemical senors to solar cells.

This thesis focuses on production techniques and electronic properties of solution processed organic thin film transistors (OTFTs) based on 6,13-Bis(triisopropylsilylethynyl) (TIPS) pentacene as semiconductor material.

Although relatively new to the materials science community, TIPS pentacene has been shown to impose great mobilities and high on/off ratios. Moreover, TIPS pentacene is soluble in several solvents - a feature not available for "standard" pentacene application. Further, TIPS pentacene shows great air stability, which is a major advantage compared to the well known polymer Poly-(3-hexylthiophene-2,5-diyl) (P3HT).

In this thesis a discussion of different production techniques as well as solvent specific influences is provided. The role of interfacial layers for pretreatment and parameter controlling is presented. The influences of air exposure and light illumination on device parameters are discussed with respect to consequences for stability and performance of the OTFTs. Moreover, solution based TIPS pentacene devices are compared to thermally evaporated TIPS pentacene OTFTs as well as "standard" pentacene devices to gain information about the quality of this certain OTFTs.

Kurzfassung

Organische Materialien bieten die Möglichkeit, sowohl ökonomisch als auch effizient, elektrische Bauelemente herzustellen. Deren Anwendung sind weitreichend, beginnend von großflächigen flexiblen Bildschirmen über chemische Sensoren bis hin zu Solarzellen.

Die Diplomarbeit beinhaltet mehrere Methoden, die das Aufbringen vom organischen Halbleitermaterial 6,13-Bis(triisopropylsilylethynyl) (TIPS) Pentacen aus einer Lösung ermöglichen. Weiters werden elektronische Charakterisierungen, die das Verhalten und spezielle Eigenschaften von Transistoren zeigen, durchgeführt.

Das Interesse an TIPS Pentacen ist aufgrund der hohen erreichten Mobilitäten und des guten Verhältnisses zwischen Einschalt- und Auschaltstrom des Transistor immens gestiegen. Weiters ist TIPS Pentacen, im Gegensatz zu Pentacen, in unterschiedlichen Kohlenwasserstoffen löslich. Ein weiterer großer Vorteil von TIPS Pentacen gegenüber anderen organischen Halbleitern ist die ausgezeichnete Stabilität an Luft, welche speziell gegenüber dem ausführlich untersuchten Polymer Poly-(3-hexylthiophene-2,5-diyl) (P3HT) einen großen Vorteil darstellt.

Die vorliegenden Arbeit zeigt die Unterschiede der Transistoreigenschaften hinsichtlich der verwendeten Aufbringungsmethoden und Lösungsmittel. Es wurden Grenzflächenmodifikationen vorgenommen und deren Einfluss auf die spezifischen Kenngrößen eines Transistors, insbesondere die Schwellspannung, untersucht. Des weiteren wird speziell auf den Einfluss von Licht und Luft auf das Transistorverhalten eingegangen. Vergleichend dazu werden Transistoren mit thermisch aufgedampften TIPS Pentacen und herkömmlichen Pentacen Schichten herangezogen, wodurch eine qualitative Beurteilung der Ergebnisse der aus Lösungsmittel aufgebrachten organischen Halbleiterschichten möglich ist.

Acknowledgments

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- Birgit Kunert and Harald Kerschbaumer for general lab support
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Contents

1. Introduction

Kahng and Atalla demonstrated the first metal-oxide-silicon field effect transistor in 1960. It took then more than two decades until 1987 the first organic field effect transistor (OFET) was presented by Koezuka.[1],[2] Electrical advantages and versatile applications make organic materials very attractive for many components of electrical devices.[3] Electronic applications are reaching from flexible integrated circuits [4],[5],[6] to large area displays or solar cells.[7],[8],[9] Other applications based on organic materials are, for example, radio frequency identification cards (RFIDs) [10] or chemical sensors (e.g detection of vapor or humidity).[11],[12],[13]
One reason for the tremendous increase of interest in developing organic thin film transistors (OTFTs) is the increasing performance compared to amorphous silicon (a-Si) thin film transistors.[14] On/off ratios as well as mobilities have increased significantly. Mobilities nowadays reach values up to 10 $cm^2V^{-1}s^{-1}$ in case of single crystals and polycrystalline films consisting of small molecules [15] and 0.6 $cm^2V^{-1}s^{-1}$ for solution processed polymers.[14]
Beyond the mentioned technological interest, one has also take the importance of OTFTs for fundamental research into account. OTFTs provide potential to gain insight into the charge transport mechanism in organic semiconductors.[16] Therefore, it is essential to understand all the various factors which influence the performance of OTFTs, beginning with intrinsic properties as well as the process and manufacturing techniques.

However, in spite of all advantages organic devices provide, their inorganic counterparts typically still offer better over all performance. Disadvantages like lower mobilities which correlate with low switching speeds as well as reduced lifetime still limit the technical success and breakthrough of organic materials in the field of electronics.[17]
In mainstream semiconductor technology, the metal-insulator-semiconductor field effect transistors (MISFETs) based on inorganic semiconductors are the leaders regarding important electronic devices.[18]

1.1. Scope and Structure of this Thesis

This thesis concentrates on the production techniques as well as on properties, performance, and quality of solution processed OTFTs. Beside the well known polymer Poly-(3-hexylthiophene) (P3HT), in this thesis 6,13-bis(triisopropysilylethynyl) pentacene (TIPS pentacene) is used as semiconductor material.
TIPS pentacene is a relatively new semiconductor material and is known for its high mobilities as well as high on/off ratios.[19],[20],[21] In comparison to the usual pentacene, TIPS pentacene is amongst others well soluble in toluene as well as acetone and anisole.[22] Further, TIPS pentacene shows a great stability towards air and light.[23]

Different solution processed production techniques (dip coating, drop casting, and spin coating) are discussed and the advantages and disadvantages of the various techniques are summarized in this work. Main factors like reproducibility and performance of the devices by using different kinds of production techniques are compared. Two different solvents and the impact on the device performance are discussed. All these results can be find in chapter 4.
To gain information about the quality and efficiency of the solution based OTFTs, those results are compared with evaporated pentacene and TIPS pentacene devices. Grazing incidence x-ray diffraction (GIXRD) measurements has been performed to understand the behavior of the molecules in the semiconductor layer.
To control the device parameters (especially the threshold voltage) and to improve the overall performance, interface modifications with self assembled monolayers (SAMs) and different polymers were performed (chapter 5).
Stability measurements (time evolution) as well as the influences of exposure to air and light are discussed and correlated with the results of x-ray diffraction (XRD) measurements. Last but not least the effect of mobility degradation is shown and explained (chapter 6).

Part I.

General Overview

2. Operation Modes of Organic Thin Film Transistors

This section gives a comprehensive overview concerning the general production techniques and the physical basics behind OTFTs. In detail, the chapter discusses the design, the working principle, and the way of extraction important device specific parameters out of measured characteristics. Finally also the used semiconductors are described briefly.

2.1. Organic Thin Film Transistor (OTFT)

In general, every thin film transistor needs three main parts:

- Electrodes (Gate, Source, Drain)
- Semiconductor
- Dielectric

In some sense the device acts like a plate capacitor with the gate electrode acting as one plate and the semiconductor as the second one. By applying a voltage between source and drain charges are injected or retrieved to and from the semiconductor. As a result, a conducting channel appears and allows to drive a current from source to drain.[15] There are two types of semiconductor materials, namely n-type (or n-channel) and p-type (or p-channel) semiconductors. The major difference between those two is that in n-type semiconductors electrons are responsible for the charge transport, whereas in the case of p-type materials holes form the conducting channel.[24]
Figure 2.1 shows two common geometries as well as the design of organic transistors. The

difference between top and bottom contact geometry is the position of the semiconductor layer relative to the electrodes. On the left side of figure 2.1 the gold electrodes are evaporated first and the semiconductor is deposited on top. This type is called **bottom contact**. In **top contact** geometry, the semiconductor is deposited on the pretreated substrate and the gold electrodes are evaporated afterwards. Both types were used during this work.
The main reason for using different geometries is the different interaction of the organic material with the insulator and/or the electrodes (e.g. influence of the contact resistance). Especially when using solution processed films, the geometry has a tremendous impact on the performance of the transistor.

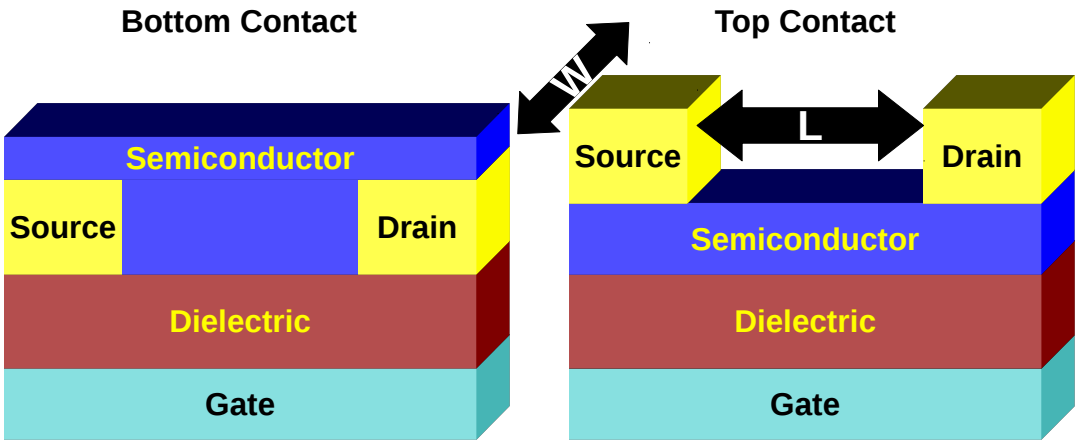


Figure 2.1.: Two common geometries of organic thin film transistors. Left: Bottom contact; Right: Top contact.

The substrates used through out this thesis consisted of highly p-doped silicon acting as gate electrode at the same time. On top of the gate electrode an approximately 150 nm thermally grown layer out of silicon dioxide SiO_2 is used as dielectric. Both, highly doped silicon and silicon dioxide are delivered laser cut.[1] During this work each wafer came from the same charge (delivered October 2010).
On those wafers the semiconductor layer can be deposited via different techniques (e.g.

[1]Company: Siegert Consulting e.K.; Franzstrasse 107 D-52064 Aachen Germany

thermal evaporation, spin coating, drop casting, or dip coating). Further information about the deposition of the semiconductor can be found in chapter 4.
The 50 nm thick gold electrodes are deposited via thermal evaporation through a shadow mask.
In figure 2.1 two important parameters of an OTFT are indicated; the **channel length L** and the **channel width W**. Both, the channel length (which is the distance between the source and drain electrodes) as well as the channel width are important for data extraction (see section 2.5).[15] In our case the channel width is constantly 7 mm, the channel length varies between 25 µm and 50 µm. The size of each wafer is 2 cm x 2 cm. A picture of a device is shown in figure 2.2. It is a bottom contact device, where the TIPS pentacene was spin coated onto the substrate from a toluene solution. On each substrate four transistors are located. The two slightly smaller pads in the middle can be used as gate electrodes if the dielectric and the deposited semiconductor gets shortened before the gold electrodes gets evaporated. Therefore, between the highly doped silicon and the gold, a conduction channel is formed.
To reduce the charging current and thus also the gate current, the organic semiconductor around each transistor was scratched away with a knife. This is essential for reducing the off current and improve the on/off ration of the device by a factor of 100.

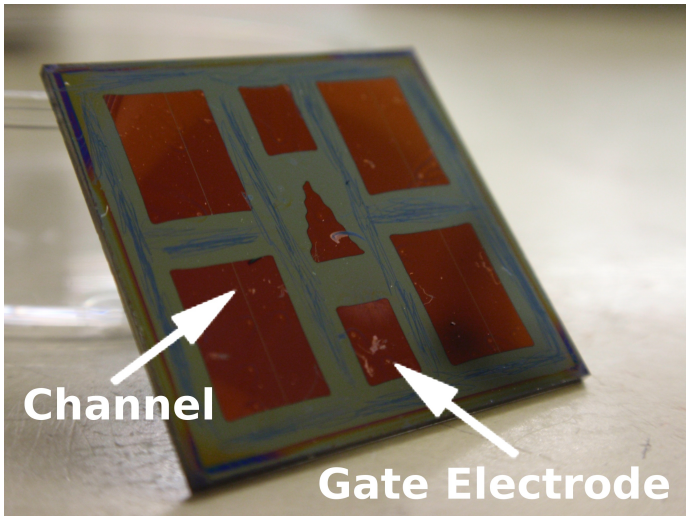


Figure 2.2.: Picture of a standard device including four transistors. The left white arrow indicates the channel on the transistor, the right white arrow indicates one of the two gate contact pads. TIPS pentacene was spin coated onto the substrate from a toluene solution (bottom contact geometry).

2.2. Working Principle

This section briefly describes the working principle of a **p-type** OTFT (principle based on [17]). Figures 2.3, 2.4 and 2.5 show cross sections through transistors where different source-drain voltages and gate voltages are applied. The "+" indicates positive charges (holes), "-" the negative charges (electrons), respectively. The threshold voltage (the voltage where the holes start to get accumulated and where the channel gets conductive) is set to zero in this example.
The following cases can be distinguished:

(a) $V_{\mathbf{TH}} = \mathbf{0}$, $V_{\mathbf{S}} = V_{\mathbf{D}} = \mathbf{0}$, $V_{\mathbf{G}} < \mathbf{0}$ (figure 2.3)

By applying a negative gate voltage, electrons in the gate are responsible for the accumulation of the holes at the dielectric-semiconductor interface. The holes are distributed uniformly. Obviously no current is flowing from source to drain because there is no potential difference between those two (both are grounded).

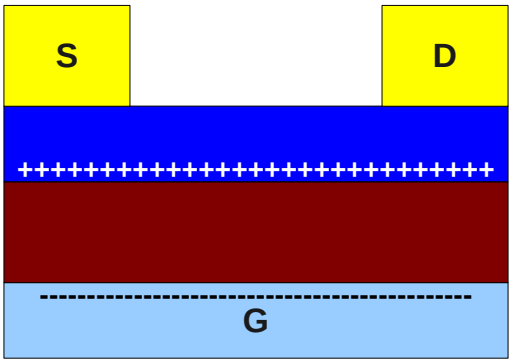


Figure 2.3.: Schematic working principle of a p-type OTFT shown in the accumulation regime.

(b) $V_{TH} = 0$, $V_S = 0$, $V_G < V_D < 0$ (figure 2.4)

The situation changes by applying a negative drain voltage. Now charges can flow from source to drain. If the drain voltage is less negative than the gate voltage the transistor operates in the **linear regime**. Therefore, the device behaves ohmic which means that by increasing the source-drain voltage the drain current increases linearly. The holes are almost uniformly distributed in the channel.

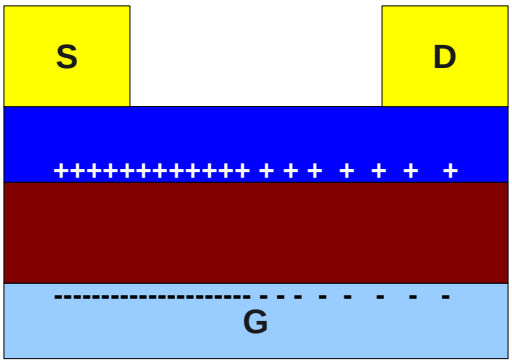


Figure 2.4.: Schematic working principle of a p-type OTFT shown in the linear regime.

(c) $V_{TH} = 0$, $V_S = 0$, $V_D < V_G < 0$ (figure 2.5)

Applying a drain voltage which is more negative than the gate voltage leads to saturation of the drain current. Now the transistor operates in the **saturation regime**. Further increase of the drain voltage does not lead to higher (absolute value) drain currents. A **depletion zone** forms and grows by applying higher source-drain voltages. The specific point where the saturation regime begins is called **pinch-off-point**.

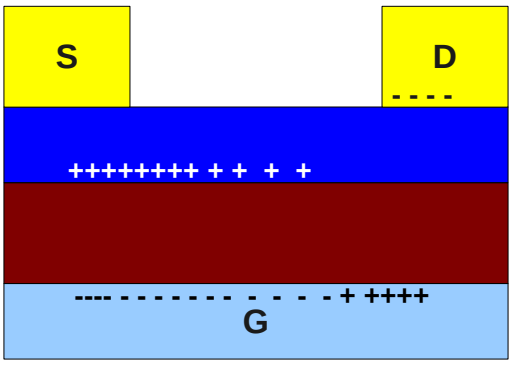


Figure 2.5.: Schematic working principle of a p-type OTFT shown in the saturation regime where the depletion zone is formed.

The following equations (2.1 and 2.2) summarize this behavior for p-channel devices:[18],[25]

Linear Regime:

$$|V_{\mathrm{D}}| \leq |V_{\mathrm{G}} - V_{\mathrm{TH}}| \tag{2.1}$$

Saturation Regime:

$$|V_{\mathrm{D}}| > |V_{\mathrm{G}} - V_{\mathrm{TH}}| \tag{2.2}$$

V_{D} ...Source-drain voltage
V_{G} ...Gate voltage
V_{TH} ...Threshold voltage

2.3. Measuring Device Characteristics

Figure 2.6 shows the measurement system used for the characterization of our OTFTs. Via probing tips the source and drain pads get contacted. To contact the gate there are two possibilities:
The first one is directly from the top (via one of the two middle gold pads in figure 2.2). In this case the dielectric layer has to get slightly cut through at the gate pad position before the gold is evaporated onto the device. Then, the contact between the highly doped silicon gate gets shortened with the two small gold pads.
The second method, which is shown in figure 2.6, is from the bottom via a copper plate. A conductive carbon tape holds the device to prevent the substrate to slip.
A **Keithley Dual Source Meter** allows to measure the drain current and the gate current simultaneously by sweeping gate or drain voltage.

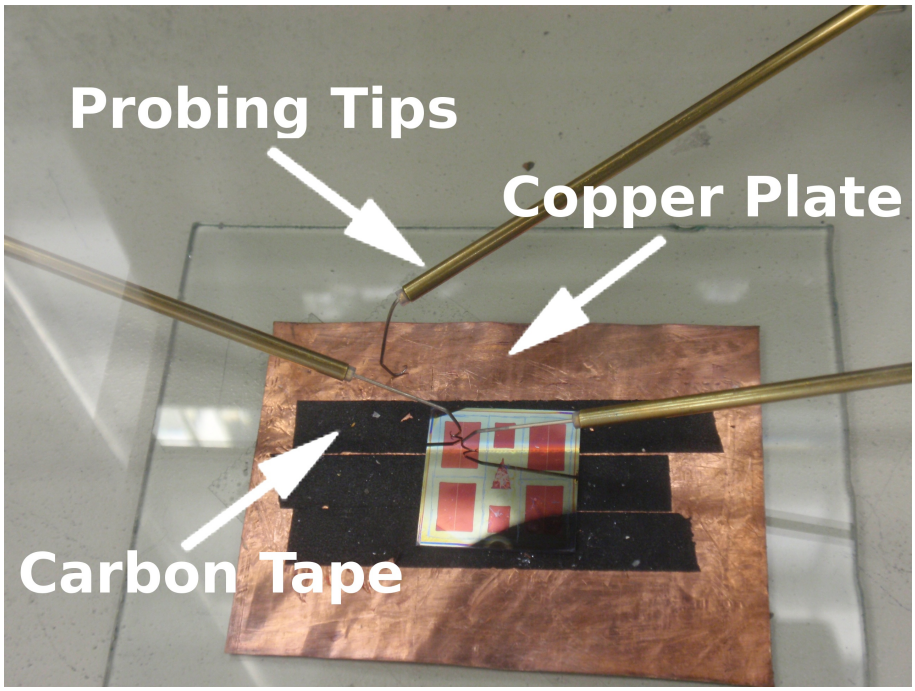


Figure 2.6.: Standard measurement setup. Via probing tips the gold pads get contacted. The carbon tape holds the device on the copper plate.

The following figures (figure 2.7, 2.8, 2.9 and 2.10) are examples for the standard analysis of devices.

2.3.1. Transfer Characteristics

Figure 2.7 shows the transfer characteristics of a spin-coated TIPS pentacene device deposited from 1 wt.% solution in toluene. In this depiction the gate voltage is swept and the drain current is measured for different drain voltages.
Out of these characteristics the mobility, the threshold voltage and the turn-on voltage (see below) can be obtained. Also the size of the hysteresis and the maximum value of the drain current can be determined.
Both, the linear and the saturation regime can be used for determining these parameters.

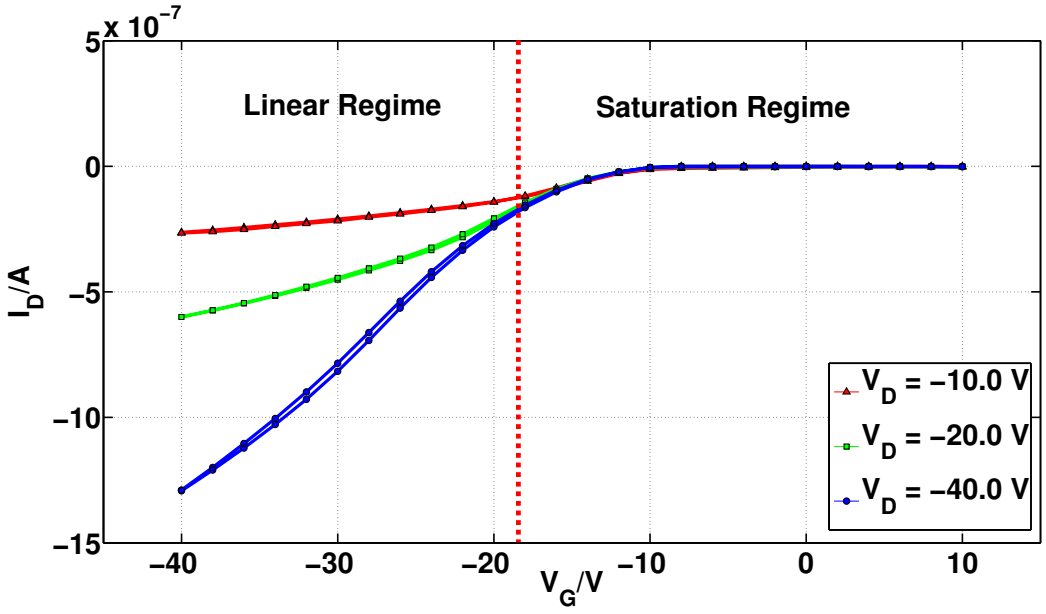


Figure 2.7.: Transfer characteristics of a spin coated TIPS pentacene device. The dotted line separates the linear and the saturation regime for the drain voltage V_{D} = -10 V. The threshold voltage lies around V_{TH} = -8 V.

Logarithmic Plot

Figure 2.8 shows logarithmic plots of the transfer characteristics for the same device. The turn on voltage (the voltage where the device starts to operate) as well the on/off ratio (difference between maximum current and off current) are indicated.

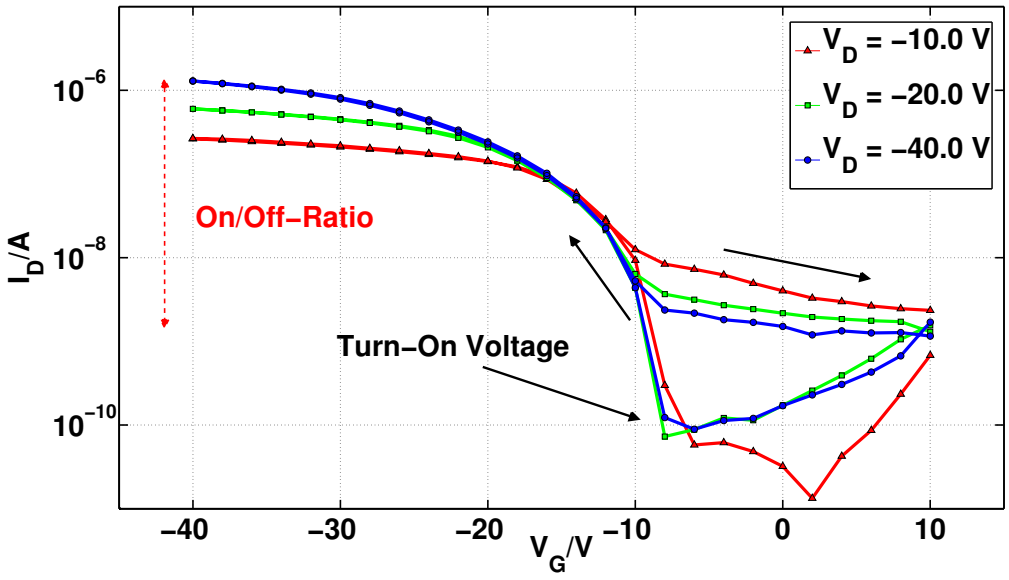


Figure 2.8.: Logarithmic plots of the transfer characteristics of a spin coated TIPS pentacene device for different drain voltages. The turn on voltage lies around V_{on} = -8 V, the on/off ratio is about 10^3.

Square Root Plot

Plotting the square root of the drain current over the gate voltage leads to the so called "square root plot" where important device parameter can be extracted (figure 2.9). One important parameter is the threshold voltage which is the extrapolated linear fit to zero drain current. Further the mobility can be obtained by the slope of a linear fit in the saturation regime (details see below).[26]

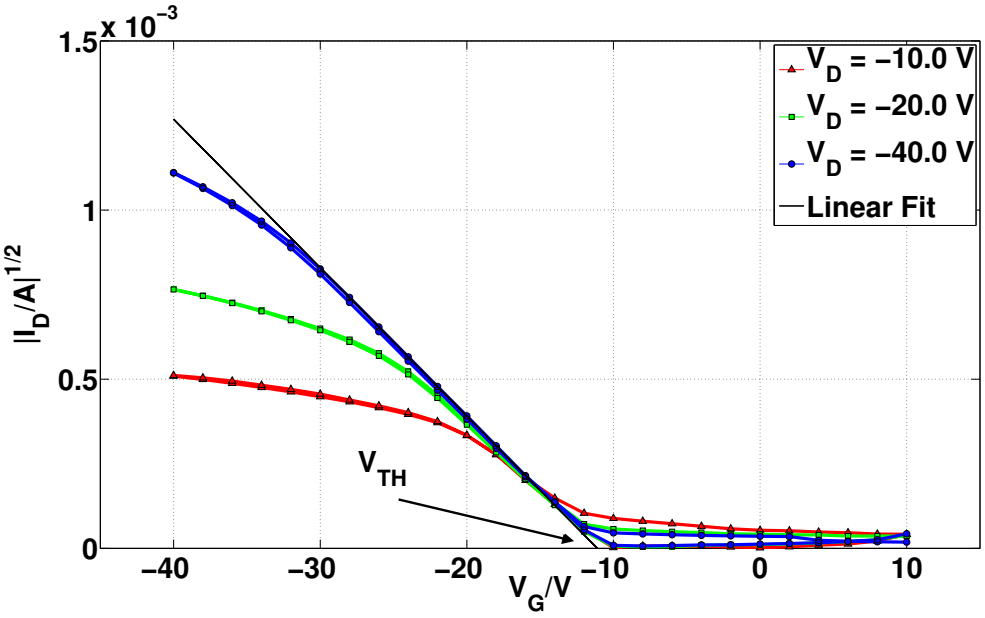


Figure 2.9.: Square root of the drain current over the gate voltage of a spin coated TIPS pentacene device. The threshold voltage (V_{TH}) and the mobility (μ) can be obtained from a linear fit in the saturation regime.

2.3.2. Output Characteristics

In the output characteristics (figure 2.10), the drain voltage is swept and the drain current is measured for different gate voltages.
Out of these characteristics, it can be seen how well the drain current saturates for large (negative) drain voltages. Starting from the pinch-off-point the drain current should not further increase upon increasing the drain voltage.
Moreover, the influence of the contact resistance can be determined by an output characteristic. In the linear regime the "perfect" transistor should behave like an ohmic characteristics, which means linear increase of drain current with drain voltage. This is not the case (deviation of a straight line in the linear regime) if the contact resistance plays a major role.[27]

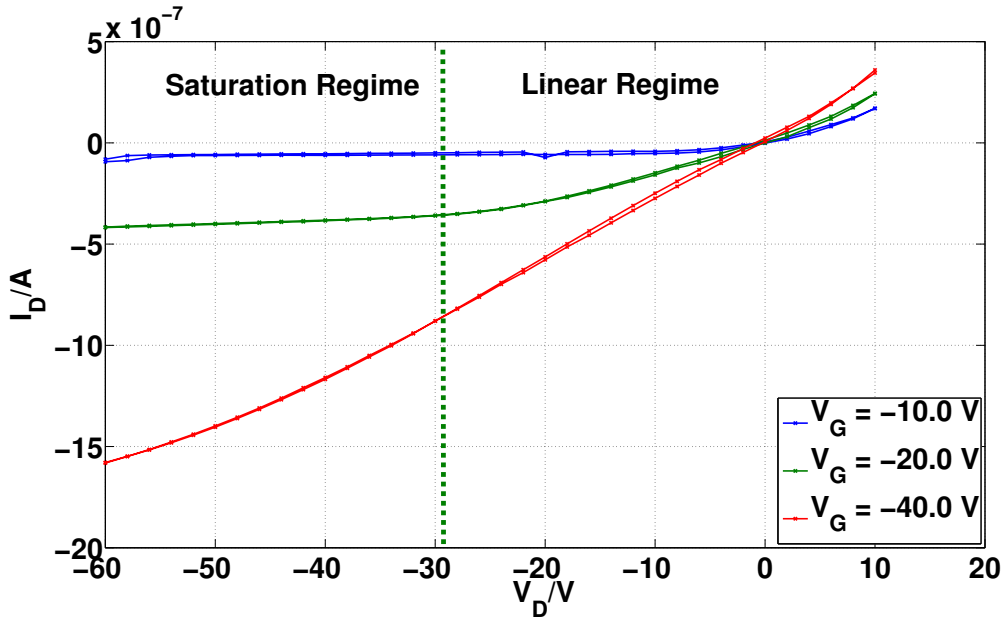


Figure 2.10.: Output characteristics of a spin coated TIPS pentacene device. The dotted line separates the linear and the saturation regime for the gate voltage V_G = -20 V. The threshold voltage lies around V_{TH} = -8 V.

2.4. Charge Transport

There are two common models to describe charge transport in organic materials (basically taken from [28]).
The major difference between metals and conventional semiconductors is that in amorphous or organic semiconductors the charge transport does not occur in delocalized states. In organic semiconductors the conductibility is much lower. Further different kind of models are used to describe the behavior of the charge carries in the material.

2.4.1. Hopping Transport

In most organic materials the transport occurs via hopping of the charges (holes or electrons) between localized states (transport is phonon assisted). The charge mobility increases with temperature and follows the relation in equation 2.3:

$$\mu = \mu_0 \; exp\left[-\left(\frac{T_0}{T}\right)^{1/\alpha}\right] \tag{2.3}$$

with

α ...Integer between 1 and 4
μ_0 ...Mobility at temperature T_0
T ...Actual temperature

The boarder between localized or delocalized transport is often not quite clear and normally mobilities between 0.1 an 1 $cm^2V^{-1}s^{-1}$ are taken for that boundary.[28]

2.4.2. Multiple Trapping and Release

Another method for describing the transportation of charge carries is via the Multiple Trapping and Release (MTR) model. This model is more valid for well-ordered materials, vapor deposited small molecules (e.g. pentacene) or oligothiophenes.[29]
In this model a high concentration of localized energy levels around a band edge acts as traps. The charge carriers (in our case holes) can be trapped and afterwards thermally released. The resulting drift mobility can be expressed as follows (equation 2.4):

$$\mu_{\mathrm{D}} = \mu_0 \ \alpha \ exp\left(-\frac{E_{\mathrm{c}} - E_{\mathrm{t}}}{kT}\right) \tag{2.4}$$

with

α ...Ratio between effective density of delocalized states and concentration of traps
E_{c} ...Energy of the transport band edge
E_{t} ...Energy of single trap level

2.5. Data Extraction

From the characteristics which are explained in section 2.3 important quantities can be determined. This section gives a compact review concerning the most important parameters and the way to extract them.
Table 2.1 lists the parameters and the values we need for parameter extraction.

Table 2.1.: List of parameters and values needed for parameter extraction.

Parameter	**Notation**	**Value**
Type of semiconductor		p-type
Channel length	L	25 µm - 50 µm
Channel width	W	7 mm
Gate insulators capacitance per area	C_i	24 nFcm^{-2}

Calculation of gate insulators capacitance per area:

$$\frac{C_i}{A} = \frac{\epsilon_0 \epsilon_r}{d} \tag{2.5}$$

ϵ_0 ...Dielectric constant in vacuum ($\approx 8.85 \cdot 10^{-12}$ AsV^{-1}m^{-1})
ϵ_r ...Relative permittivity (Silicon dioxide: $\epsilon_r = 3.9$)
A ...Area
d ...Separation between the plates (d = 150 nm)

2.5.1. Field Effect Mobility and Threshold Voltage

The mobility can be calculated in the linear as well as in the saturation regime. The following equations (2.6 and 2.7) describe the behavior of the drain current (I_{D}) in the linear and the saturation regime.[15],[30]

Linear regime:

$$I_{\mathrm{D}} = \frac{W}{L}\, C_i\, \mu\, \left(V_{\mathrm{G}}\, - V_{\mathrm{TH}}\, - \frac{V_{\mathrm{D}}}{2}\right)\, V_{\mathrm{D}} \tag{2.6}$$

Saturation regime:

$$I_{\mathrm{D}} = \frac{W}{2\, L}\, C_i\, \mu\, (V_{\mathrm{G}}\, - V_{\mathrm{TH}})^2 \tag{2.7}$$

- Calculation of the mobility in the saturation regime:

  One way to obtain the mobility is via the square root plot out of the saturation regime. From equation 2.7 it follows:

  $$\sqrt{I_{\mathrm{D}}} = \sqrt{\frac{W}{2\, L}\, C_i\, \mu}\, (V_{\mathrm{G}}\, - V_{\mathrm{TH}}) \tag{2.8}$$

  So when plotting the square root of the drain current over the gate voltage the mobility is obtained from the slope of the linear fit. If further an extrapolation of the linear fit to zero drain current is done, the threshold voltage can be obtained (both shown in figure 2.9)
  In this thesis this was the common way to determine the mobility. Because the effect of the mobility degradation (see chapter 6) in the linear regime makes the parameter extraction in the saturation regime reasonable.

- Calculation of the mobility in the linear regime:

  Another way to calculate the mobility is from the transconductance g_m in the linear regime. For the linear regime equation 2.9 is valid:

$$g_m = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{G}}} = \frac{W}{L} C_i \mu V_{\mathrm{D}} \tag{2.9}$$

  If one calculates the ratio $\frac{g_m}{V_{\mathrm{D}}}$ for each applied gate voltage the mobility can be calculated. If the mobility is gate voltage dependent, which quite often occurs for OTFTs, also the derivative $\frac{\partial \mu}{\partial V_{\mathrm{G}}}$ has to be taken into account.

2.6. Semiconductors

The most important part of each OTFT is the active material. In this thesis p-channel organic semiconductors were used where positive charges (holes) are responsible for the charge transport.[24]
The following section gives an overview of the used semiconductors and lists the main difference between TIPS pentacene and the commonly used, well known semiconductor Poly-(3-hexylthiophene-2,5-diyl) (P3HT).

2.6.1. Pentacene

Figure 2.11 shows the chemical structure of pentacene. Polycrystalline pentacene is nowadays the most common organic semiconductor material and reaches mobilities well above 1 $cm^2V^{-1}s^{-1}$.[15] Because pentacene shows poor solubility, vacuum evaporation is the most common technique for depositing this material.[31]
Pentacene is known for homogeneous and highly ordered films which lead to good hole and electron mobility. The growth conditions during the thermal evaporation process (e.g substrate temperature and evaporation rate) determine the quality of the film and its electronic properties.[32]

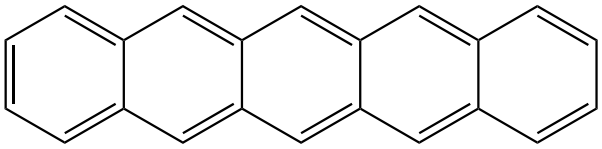


Figure 2.11.: Chemical structure of pentacene.

2.6.2. 6,13-Bis(triisopropylsilylethynyl) (TIPS) Pentacene

TIPS pentacene is a derivative of pentacene and its structure is shown in figure 2.12. At the middle ring of the pentacene molecule two side chains are attached. This modification makes TIPS pentacene soluble amongst others in toluene, anisole and acetone.[22]
In recent years high mobilities up to 2.5 $cm^2V^{-1}s^{-1}$ as well as high on/off ratios (10^8) were achieved with TIPS pentacene as semiconductor material.[19],[20],[21]
As mentioned before, the big advantage of TIPS pentacene is its solubility. This certain

property makes this material so interesting because of the opportunity to access printing techniques.

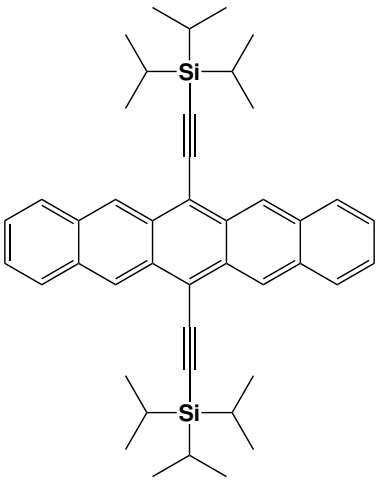


Figure 2.12.: Chemical structure of TIPS pentacene.

2.6.3. Poly-(3-hexylthiophene-2,5-diyl) (P3HT)

As easy to observe from figure 2.13 P3HT is, in contrast to TIPS pentacene, a polymer and not a small molecule. P3HT is known for certain properties like self-organization to form micro crystalline structures. Further, reported mobilities up to 0.1 $cm^2V^{-1}s^{-1}$ and high on/off ratios of up to 10^6 make the semiconductor material quite interesting.[33] P3HT is soluble in chlorinated hydrocarbons such as chloroform or dichlorobenzene. In addition it is reasonably soluble in tetrahydrofuran (THF) and aromatic hydrocarbons such as toluene.[34]
However, bad air stability [35] is a major disadvantage of P3HT in comparison to TIPS pentacene.

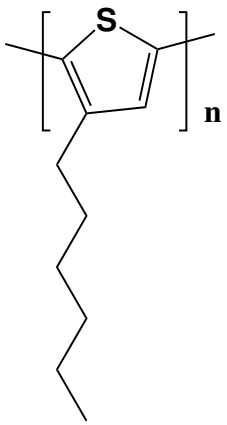


Figure 2.13.: Chemical structure of P3HT.

2.7. Surface Modifications

The motivation behind any kind of surface modification is to control device parameters and further to improve the performance of the devices. In chapter 4 and 5 the methods and the detailed accomplishment of substrate pretreatment and parameter controlling of the devices are explained.

This part should just give a general overview of the methods used in this thesis. The pretreatment of the substrate is important and has the following purposes:

- Cleaning of the substrate (see section 4.1.2)
- Promotion for adhesion (see section 4.1.2)
- Parameter control (see chapter 5)

The following methods were used in this thesis:

- Plasma etching
- Deposition of cleaning-polymers
- Self assembled monolayers (SAMs)

2.7.1. Plasma Etching

Figure 2.14 shows the used plasma etching system.[2] The sample lies on a sample holder in the vacuum chamber under the electrode which is connected to the radio frequency generator. After evacuating the chamber (it takes about five minutes to reach the operating pressure of 2 mbar) oxygen flows through a valve in the chamber. The flow rate[3] (between 8 and 10 $cm^3\ min^{-1}$) has to be adjusted therefore, an equilibrium pressure can be obtained. After reaching the operation pressure (lies at about 4 mbar) the plasma can be ignited.
There are two main reasons for plasma etching in a low pressure environment:[36]

- After the plasma etching procedure the surface of the substrate is cleaned from organic residuals
- Activation of the surface leads to an increase of the number of OH functionalities and as a result to a hydrophilic surface

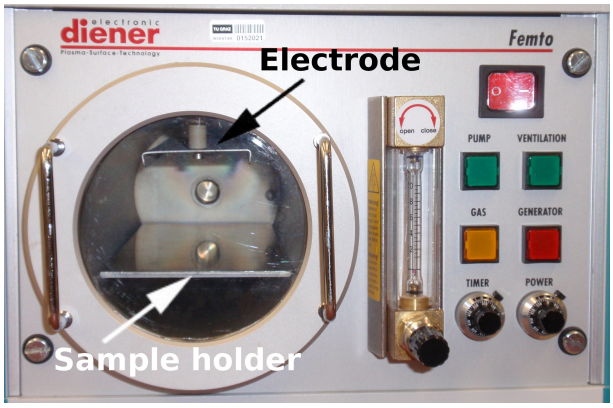


Figure 2.14.: Plasma etching system in a low pressure environment.

[2]Company: Diener electronic; product: "Femto"
[3]Gauging of the flow rate instrument with N_2 gas at 1,013 bar and 20 °C

2.7.2. Cleaning Polymers

Another method to modify the surface is by using cleaning polymers. Those polymers are usually designed for cleaning lenses, but works quite well also for our purposes. The "First Contact"[4] polymer was spread by a brush on the untreated SiO_2 device (see figure 2.15, top). After 15 to 30 minutes (depending on the used amount and ambient conditions) the liquid turns into a solid and can be removed from the wafer using a tweezer (see figure 2.15 bottom).
The main consequence of this pretreatment is to remove the dust and dirt from the surface.

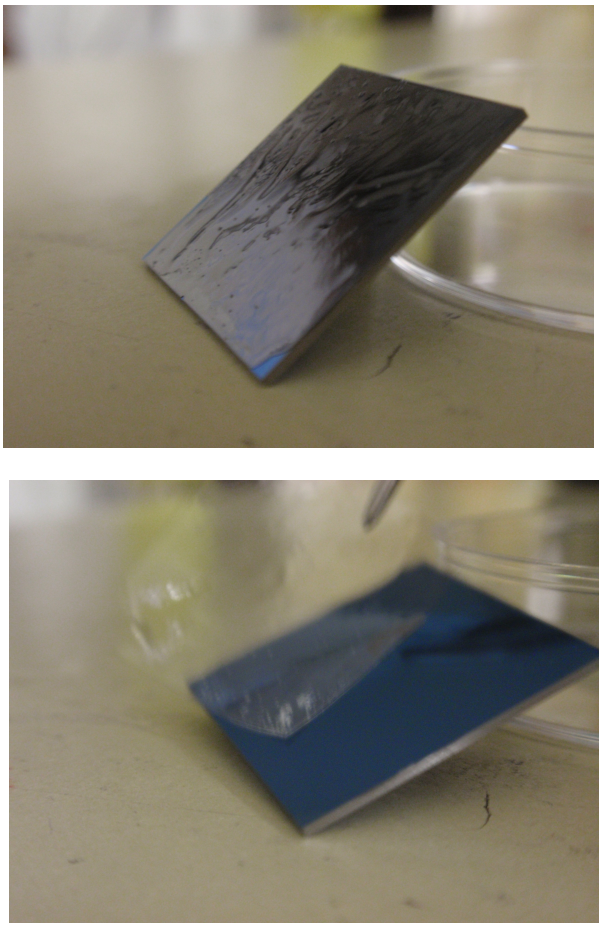


Figure 2.15.: Pretreatment with "First Contact". Top: Substrate with "First Contact" spread on it. Bottom: Removing layer from substrate with a tweezer.

[4]Company: Optoprim GmbH; product: "First Contact"

2.7.3. Self Assembled Monolayers (SAMs)

Talking about interfaces, in this thesis always the interface between dielectric and semiconductor is meant.
Self assembles monolayers (SAMs) are two dimensional objects which form spontaneously on a surface.[37] The process for growing SAMs as well as the different kinds of used molecules are described in detail in chapters 4 and 5.
In this thesis, SAMs with trichlorosilane as docking groups were grown on SiO_2 substrates.

The mechanism of SAM formation is the following:

The first step is called physisorption[5] where the trichlorosilane groups adsorb at the hydrated silicon surface. For this step a hydrophilic surface is needed which can be achieved by oxygen plasma etching.[36] Afterwards the silane head groups dock to the silanol groups $Si(OH)_3$.[38] For this hydrolysis trace amounts of water on the surface is essential.[37] Now a covalent bond forms between the polar $Si(OH)_3$ groups and the hydroxyl groups on the SiO_2 surface.[38]

In general, many parameters (especially the trace amount of water) play an important role for the formation of monolayers.[37] The whole procedure is quite challenging and, therefore, very difficult to reproduce.

[5] bonding through weak physical forces like Van-der-Waals interactions

3. Analytical Methods

This section briefly summarizes the used methods for analyzing the deposited TIPS pentacene layers via x-ray scattering. X-ray scattering is a very powerful technique for determining the orientation of the molecules and gives information about structural properties.

To determine the arrangement of atoms in a crystal, x-ray diffraction (XRD) and grazing incidence x-ray diffraction (GIXRD) measurements were performed. The results can be found in chapter 4 and chapter 6, section 6.1.

The following reviews about XRD and GIXRD are basically taken from [39] and [40].

For detailed information the textbooks [39] and [41] are recommended.

3.1. X-Ray Powder Diffraction (XRD)

In this thesis a Siemens D501 Kristalloflex powder diffractometer (coupled $\Theta/2\Theta$) with a copper x-ray tube was used (99.9 % CuKα radiation, wavelength $\lambda = 1.54$ Å).
Figure 3.1 shows the measurement system as well as the definition of the angles Θ and 2Θ. The x-ray beam out of the copper x-ray tube hits the sample surface with an angle Θ. The diffracted beam passes the monochromator and goes into the detector (right hand side in figure 3.1). The angle between the incident beam and the detected beam is 2Θ.
During the measurements the tube is fixed and the sample moves with an angular velocity of ω. To conserve the ratio of $\Theta/2\Theta$, the detector moves with an angular velocity of 2ω.
Important to mention is that the incident beam as well as the diffracted beam lie in the same plane. The difference between those two is called **scattering vector** $\vec{S}$.
For further alignment of the x-ray beam (reduction of the divergence) two diaphragms in front of and one after the sample are used (slit sizes of diaphragms are 1 degree).

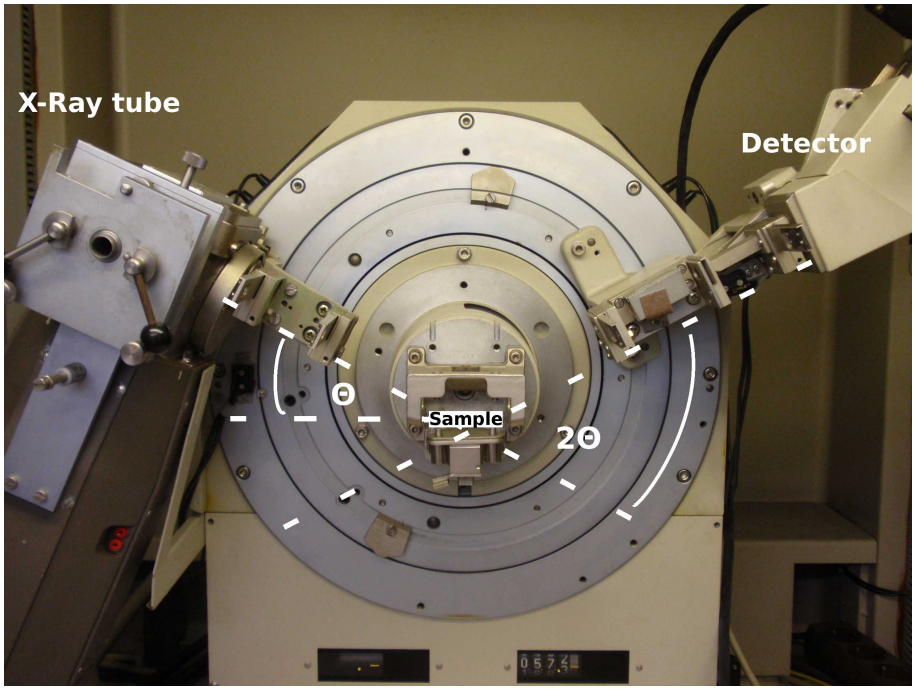


Figure 3.1.: Siemens D501 Kristalloflex powder diffractometer. The sample and the detector are moving relative to the fixed x-ray tube. The angle between the incident beam and the sample surface is called Θ, the angle between the incident beam and the detector is called 2Θ, respectively.

3.1.1. X-Ray Θ/2Θ Scan

To obtain constructive interference, Bragg's law has to be fulfilled (equation 3.1). At certain 2Θ positions of the the detector, intensities which are assigned to certain net planes d_{hkl} will be detected.
The second condition for diffraction is that the scattering vector $\vec{S}$ has to be perpendicular to the net plane. Therefore, the incident angel equals the outgoing angle. As a result, the measured intensities correspond to net planes, which are all parallel to each other. I.e. only net planes parallel to the surface are visible as diffraction peaks. Only the distance between the net planes differs.

$$n\lambda = 2d\ sin\left(\frac{2\Theta}{2}\right) \tag{3.1}$$

n ...Integer
λ ...X-ray wavelength (1.54 Å for CuKα)
d ...Distance of the lattice planes
2Θ ...Angle between incident x-ray beam and detector

3.2. Grazing Incidence X-Ray Diffraction (GIXRD)

To gain structural and phase information about the surface and the semiconductor/ dielectric interface, Grazing Incidence X-Ray Diffraction (GIXRD) measurements have been performed. Out of the GIXRD data it is possible to obtain information on the molecular packing and orientation in the two dimensional crystallites.
Figure 3.2 shows the principle setup of GIXRD. A highly collimated x-ray beam strikes the sample under a very small angle α_i. The incident angle α_i is kept smaller than the critical angle. Therefore, total external reflection occurs, which limits the penetration depth of the x-ray beam. This maximizes the path of the x-rays through the thin film and minimizes unwanted scattering from the substrate. Moreover, lattice planes perpendicular to the surface are probed.
A one dimensional position sensitive detector (1-D PSD) moves along the 2Θ circle and measures the scattered intensity for different α_f (angle of the scattered beam) along the q_z direction, normal to the surface. Out of this, the scattering vector q_{xy} parallel to the surface and q_z normal to the surface can be obtained (see equation 3.2 and 3.3).

The ingoing wave vector is labeled k_i the outgoing wave vector k_f, respectively.

Note: For characterization of thin films, synchrotron radiation, which is very effective because of the parallel and intense beam, should be used.

$$q_{xy} = q_{\parallel} \approx \frac{4\pi}{\lambda} sin(\Theta) \tag{3.2}$$

$$q_z = q_{\perp} = \frac{2\pi}{\lambda}(sin(\alpha_f) + sin(\alpha_i)) \tag{3.3}$$

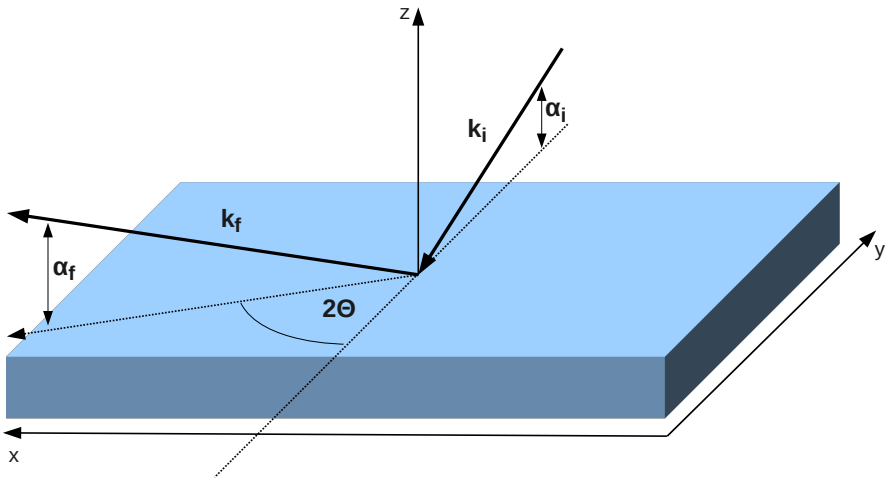


Figure 3.2.: Geometry of a grazing incidence diffraction. The x-ray beam hits the sample under the angle of incidence α_i which is less than the angle of total reflection. The 1-D PSD detector moves on a 2Θ circle. k_i and k_f are the wave vectors for the incident beam and the outgoing beam, respectively. α_f describes the scattered angle. Adapted from [40].

Part II.

Results and Discussion

4. Production Techniques

This chapter concentrates on the experimental procedure as well as on the achieved results during this thesis. As discussed in the introduction, the primary aim of this thesis was the production of OTFTs using soluble TIPS pentacene and testing different kinds of interface layers to control certain device properties.
Advantages and disadvantages of certain production techniques as well as the influence on the device performance of different solvents, will be discussed in this chapter.

For correlating electronic and structural properties, x-ray reflectivity (XRR) and x-ray diffraction (XRD) measurements were used. Further grazing incidence x-ray diffraction (GIXRD) was used to gain knowledge about quality and structure of the semiconductor layer.

Note: The value listed in the following chapters for the chamber pressure in the evaporation chamber is a lower limit of the actual pressure in the evaporation chamber. The reason is that the pressure sensor is located in the tube which connects the turbomolecular pump with the evaporation chamber. The distance between sensor and chamber is approximately 80 cm (cross section of tube is 4 cm).

The following materials were used during this thesis (detailed information about the semiconductors can be found in section 2.6):

Semiconductors

- 6,13-bis(triisopropyl-silylethynyl) pentacene (Sigma Aldrich; Product ID: 7146006; CAS Number: 373596-08-8)
- Pentacene (Sigma Aldrich; Product ID: P1802;
  CAS Number: 135-48-8)

Solvents

Table 4.1 lists important parameters of the two used solvents. Toluene show a much higher vapor pressure than 3,4-Dimethylanisole which has an tremendous impact on the device behavior. Moreover, the solubility of TIPS pentacene is higher in toluene (maximum value 6.57 wt.% at 23 °C) than in 3,4-Dimethylanisole (maximum value 2.03 wt.% at 23 °C).[22]

- Toluene - CHROMASOLV®, for HPLC, 99.9% (Sigma Aldrich; Product ID: 34866; CAS Number: 108-88-3)
- 3,4-Dimethylanisole - 99% (Sigma Aldrich; Product ID: 137499; CAS Number: 4685-47-6)

Table 4.1.: Solvent properties ([42], [43]).

Solvent	**Boiling point** at 760 mm Hg [°C]	**Vapor pressure** [mm Hg (at RT)]	**Molecular weight**
Toluene	111.0	22.0	92.14
3,4-Dimethylanisole	200.0 - 201.0	0.7	136.19

Note: Vapor pressure of 3,4-Dimethylanisole taken from [44].

Gate dielectric/semiconductor interface layers

- n-Hexadecyltrichlorosilane (ABCR; Product ID: SiH5920; CAS Number: 5894-60-0)
- Phenethyltrichlorosilane, contains some alpha-isomer; 97% (ABCR; Product ID: AB111301; CAS Number: 940-41-0)

4.1. Deposition of Soluble TIPS Pentacene via Dip Coating

The controlled deposition of any kind of soluble layer on a substrate is always a challenging problem. Slow drying of the solvent is one way to control film morphology and leads to good molecular ordering. Dip coating offers such a drying process because the substrate is slowly pulled out of the solution. Viscous forces are responsible for the adhesion of the liquid to the substrate. Main conditions for a well adhesion are that the solid surface has to be smooth and energetically homogeneous. The particles get assembled because of convection by the current flow field. In addition the capillary bridges between the particles order those particles in a crystalline structure.[45] Through the change of the withdrawal speed, the film morphology can be controlled.[21]

Many other parameters also influence the growth of molecules on the substrate:
As an example, the concentration of the solution and the used solvent have big impacts on the morphology. Further, one also has to take the ambient conditions into account. Room temperature, humidity, as well as external effects coming from the outside (e.g. acoustic waves, mechanical vibrations from the traffic on the street, etc.) influence the quality of the deposited layer. These problems will be discussed in detail in section 4.1.4.

4.1.1. Setup

Figure 4.1 shows the basic setup of the dip coating machine. The device is held by a Teflon clip and pulled out of the solution very slowly (order of magnitude between mms^{-1} and nms^{-1}).
The whole instrument is located in an extractor hood and on an active vibration/isolation table[1] to compensate for vibrations coupled in through the desk. As a result of the vibrations from the fan of the extractor hood, the whole system is covered with a glass hood to decrease external effects.
One has to make sure that all components (e.g. glass hood) can cope with the solvent vapor. This is the reason why for toluene glass and Teflon have to be used because those materials are resistant against toluene. The control station allows different alignments

[1] Company: Halcyonics; Product:"Micro 40 system"

Figure 4.1.: Basic setup of a dip coating instrument. Left: The dip coater is located on an active isolation/vibration table to decrease outside influences. Right: The device is held by a Teflon clip and pulled out of the solution slowly.

for the instrument:

- Speed: Controlling of pull in and pull out speed in μms^{-1}.
- Stop Point: Depth of immersion; controlling of the path in mm. The size (20 mm) of the used wafer was taken to cover it totally.
- Stop time: Waiting time between two sequenced steps in seconds (e.g. time between the pull in and pull out sequence; zero in our case).

4.1.2. Pretreatment

The devices were handled under ambient conditions. A number of pretreatments of the SiO_2 device were tried to improve the wetting:

1. Pretreatment with "First Contact"[2]: After 15 to 20 min it is possible to remove the cured material with a tweezer form the device

[2]detailed information in chapter 2 section 2.7

2. Pretreatment with Self Assembled Monolayers (SAMs) (see figure 4.2)
    - Phenethyltrichlorosilane
    - n-Hexadecyltrichlorosilane

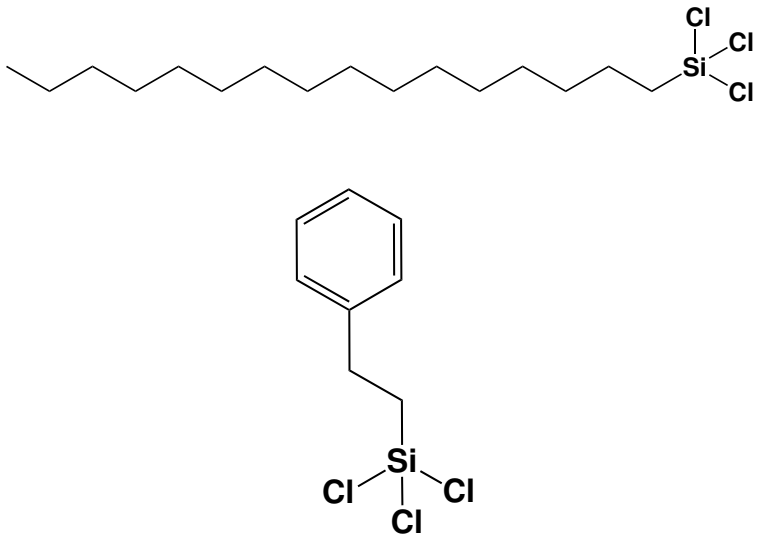


Figure 4.2.: Top: Chemical structure of n-Hexadecyltrichlorosilane. Bottom: Chemical structure of Phenethyltrichlorosilane.

The procedure was the same for both SAMs (following the process optimized by P. Pacher):

- Plasma etching for 30 seconds
    - Power level: maximum
    - Chamber pressure filled with air: 2 mbar
    - Chamber pressure filled with Oxygen: 4 mbar
- CO_2 cleaning
- Ultra sonic bath for 2 minutes in deionized water (18 MΩ)
- CO_2 cleaning
- Preparing solution made of 10 µl Phenethyltrichlorosilane or n-Hexadecyltrichlorosilane in 10 ml toluene

- Leave wafer in solution for 16 hours
- After 16 hours in solution, 2 minutes ultra sonic bath in toluene
- Wafer cleaning with fresh toluene
- Annealing step at 100 °C for 30 minutes in vacuum conditions (rotary vane pump, pressure p $\approx$ 1 mbar)
- Cooling step of the wafer for another 90 minutes

4.1.3. Results

For dip coating TIPS pentacene was always deposited from 1 wt.% solutions in toluene. Sele et al. published the best results with this solution concentration (on/off ratio about 10^8, mobilities between 0.2 and 0.4 $cm^2V^{-1}s^{-1}$).[21]
Park et al. published results using 1 wt.% chlorobenzene solutions reaching mobilities between 0.1 and 0.6 $cm^2V^{-1}s^{-1}$.[46]

Pretreatment with "First Contact"

Figure 4.3 shows one top contact device which was pulled out of solution with a withdrawal speed of 0.07 μms^{-1}. The pretreatment was done with the "First Contact" cleaning polymer. It seems, because of the slight color change, that a homogeneous layer of TIPS pentacene was deposited. However, atomic force microscopy (AFM) measurements showed that no TIPS pentacene was deposited at all. Presumably the color change came from the solvent which slightly changed the substrate color during the long dip coating process (process time approximately 76 hours).
Even by using different kinds of withdrawal speeds it was not possible to deposit TIPS pentacene on the substrate.
The same problem occurred using bottom contact geometry.

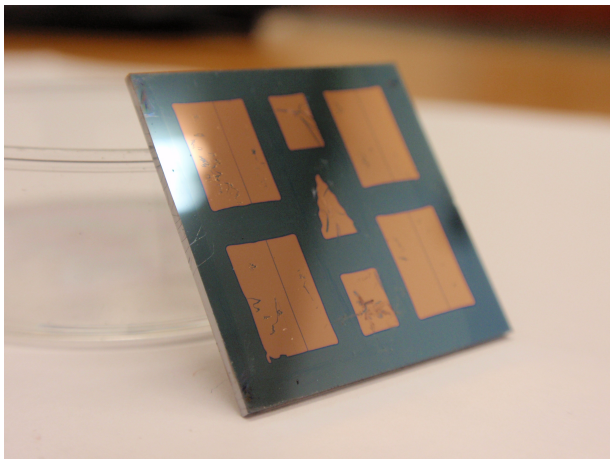
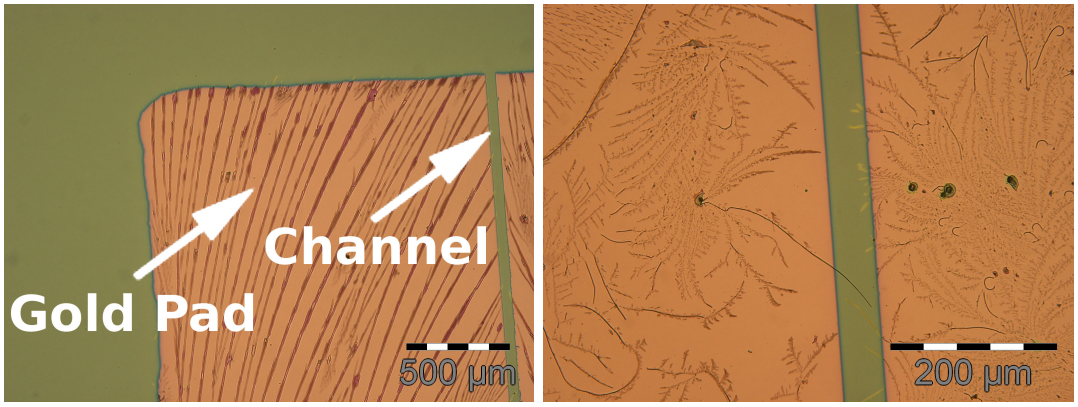


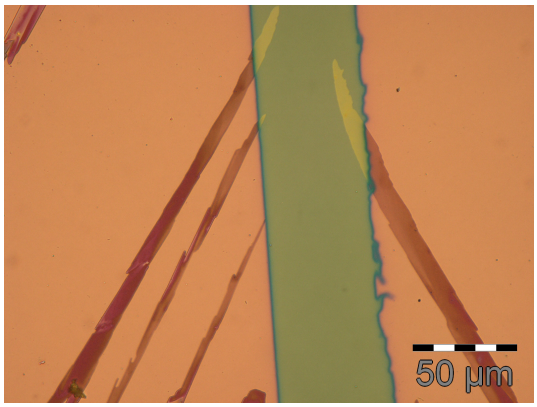
Figure 4.3.: Dip coated device pretreated with "First Contact" (top contact geometry). No TIPS pentacene was deposited (dip coating from 1 wt.% solution in toluene, withdrawal speed was 0.07 μms^{-1}.)

Pretreatment with Phenethyltrichlorosilane

To improve wetting SAMs have been used as pretreatment. Figure 4.4 shows optical light microscope pictures of TIPS pentacene from 1 wt.% solution deposited on a bottom contact device using Phenethyltrichlorosilane as interface layer.
Again it was hardly possible to coat the substrate with TIPS pentacene although the gold electrodes show better film morphology. Therefore, no transistor was operating.
In the channel hardly any TIPS pentacene crystallites are observable. Just a couple of needles are located in the channel which is obviously not enough for charge carrier transport. The density of needles is significantly increased on the gold pads.



(a) magnification 50 times (b) magnification 200 times

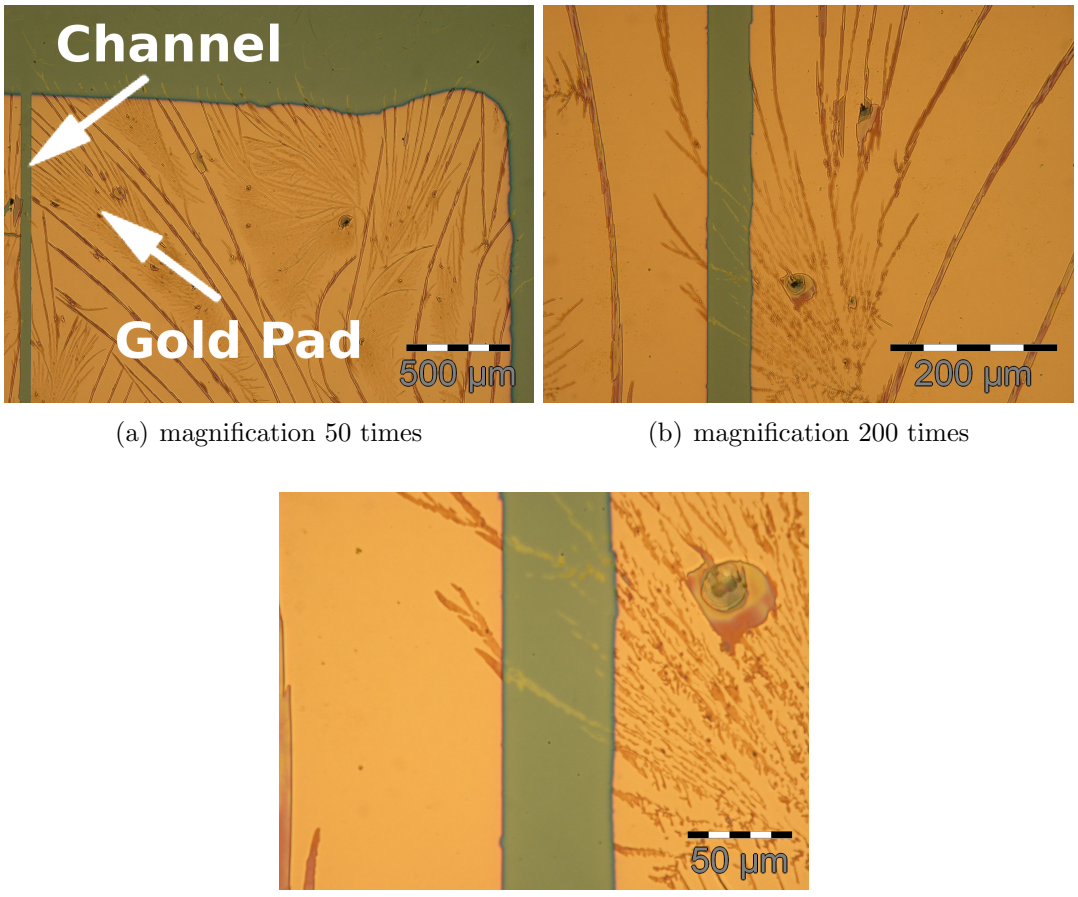


(c) magnification 500 times

Figure 4.4.: Optical light microscope pictures of a dip coated TIPS pentacene device with bottom contact geometry. Hardly any TIPS pentacene crystallites are observable. Pretreatment was done with Phenethyltrichlorosilane. Withdrawal speed 10 μms^{-1}.

Pretreatment with n-Hexadecyltrichlorosilane

Figure 4.5 shows again optical light microscope pictures of the channel and the gold pads. Now n-Hexadecyltrichlorosilane was used as interfacial layer. In this case the density of the needles in the channel is significantly higher further a few needles lie over the channel. This circumstance allow that current can flow from source to drain.
Figure 4.6 shows the linear and logarithmic plots of the transfer characteristics of an operating bottom contact transistor using n-Hexadecyltrichlorosilane as interfacial layer. However, most of the devices were not operating because of the small density of semiconductor needles in most of the channels.



(a) magnification 50 times

(b) magnification 200 times

(c) magnification 500 times

Figure 4.5.: Optical light microscope pictures of a dip coated TIPS pentacene device with bottom contact geometry. Pretreatment was done with n-Hexadecyltrichlorosilane. Withdrawal speed 10 μms^{-1}.

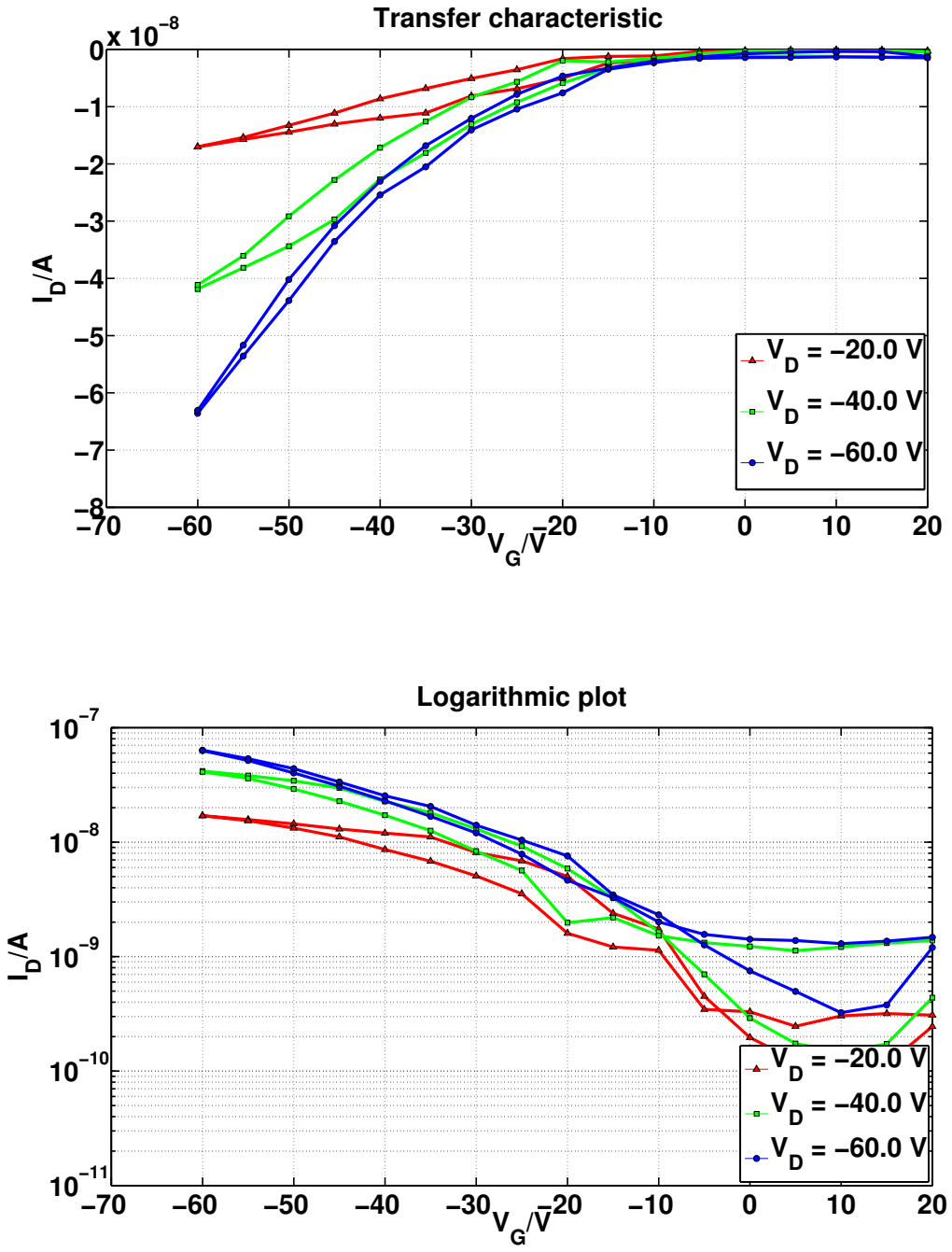
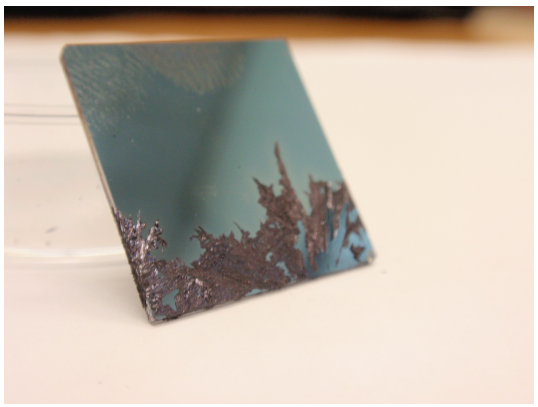


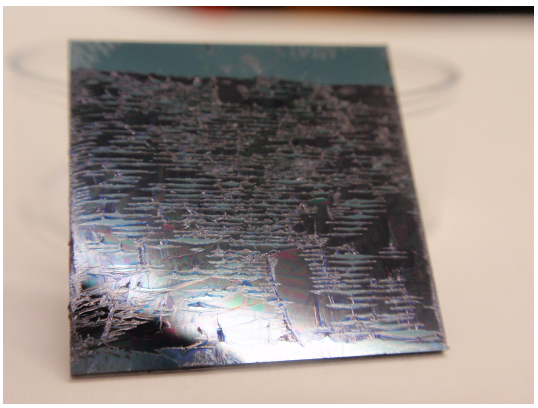
Figure 4.6.: Linear (top) and logarithmic (bottom) plots of the transfer characteristics of a dip coated device (bottom contact geometry) for different drain voltages. n-Hexadecyltrichchlorosilane was used to improve wetting. The mobility (at V_{D} = -60 V), calculated in the saturation regime, is $\mu = 1 \cdot 10^{-5}$ cm^{2}V^{-1}s^{-1}.

4.1.4. Irregularities

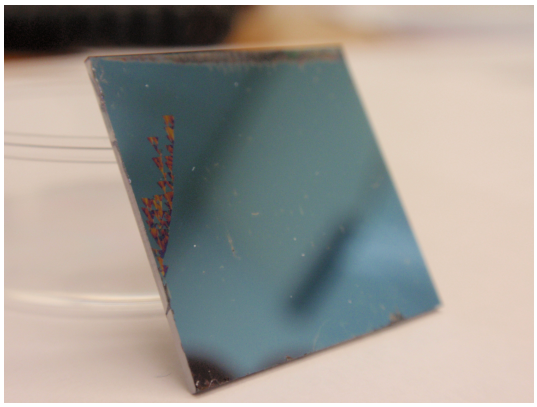
Deposition of a homogeneous film is the most challenging aspect no matter what kind of solution processable method is used. In this section some irregularities of the growth of TIPS pentacene by dip coating are shown. Those "random" crystallizations are most likely due to the (non reproducible) presence of "random" nuclei for crystallization.
On some devices, the crystallization started right after the beginning of the dip coating process and very big crystals occurred (figure 4.7 (a)). The reason for this might be that the clip which holds the substrate damaged the surface or the clip itself is the crystallization point.
In figure 4.7 (b) and (c) the crystallization stared randomly in the middle or near the end of the substrate. Small nuclei like dirt or dust could be the reason for that random crystallization point.
Important to mention is that no relation between the withdrawal speed and the crystallization can be obtained.
As mentioned at the beginning of this section, dip coating is very sensitive to all kinds of external influences. Mechanical vibrations or acoustic waves coming from the environment could also be a reason for such behavior clearly showing that the whole process is very difficult to control.



(a) withdrawal speeds 0.08 µms^{-1}



(b) withdrawal speeds 0.15 µms^{-1}



(c) withdrawal speeds 1.5 µms^{-1}

Figure 4.7.: Examples of random crystallization of TIPS pentacene on devices with different withdrawal speeds. No relation between the withdrawal speed and the crystallization behavior can be obtained. All devices were fixed to the dip coater on the top with a Teflon clip. (Substrate in picture (a) is flipped up side down).

4.1.5. Conclusion

The previous experiments showed that dip coating is a very challenging and difficult process. The pretreatment of the substrate as well as the influences of the environment during the dip coating process have strong impacts on the morphology of the film.

The pretreatment with the used self assembled monolayers was essential to produce operating devices. The obtained results are not comparable to the published ones from Sele et al.[21] The order of the crystals is far from the optimal which leads to very low mobilities (approx. $1 \cdot 10^{-5}$ $cm^2V^{-1}s^{-1}$) and low on/off ratios ($\approx 10^2$). Using different kinds of substrates or other interface layers could be the solution for that specific problem.

It was not possible to deposit TIPS pentacene on the substrate with top contact geometry. Even using bottom contact geometry without SAMs, deposition of the semiconductors was hardly possible. Longer or shorter withdrawal speeds did not change anything. The change of the concentration did not lead to any other results.

For further experiment, the dip coater should be located in a clean room environment without external vibrational influences. Even a closing door or a truck on the street in front of the building can change the morphology and the crystal growth completely.
Toluene was used as solvent which works quite well for fast withdrawal speeds (more than 0.1 mms^{-1}). To avoid fast evaporation of the solvent, solvents with lower vapor pressure should be used for longer withdrawal speeds.
The most challenging parts of the whole process are on the one hand to control the random crystallization and on the other hand the adhesion of the semiconductor to the substrate.

The obtained results were not satisfying and far away from the optimum we wanted to achieve. Our results show however, that it is possible to build operating devices via dip coating.

4.2. Deposition of TIPS Pentacene by Drop Casting

Amongst others, Park et al. [46] and Kim et al. [19] have shown successfully that drop casting is more than a qualified method for the production of TIPS pentacene OTFTs. The production technique is quite straight forward:
A solution is dropped on a substrate and after the solvent has evaporated, a layer is formed. Depending on the solvent, the evaporation needs, because of the lower vapor pressure, longer for 3,4 Dimethylansiole than for toluene. The molecules have enough time to order in a low energy state and form relatively big crystals. The advantage of big crystals is that those have larger grain size (lower grain boundaries) which leads to higher mobilities.[47] The disadvantage is that the formed layers are quite rough which leads to a couple of problems (see below).

The procedure of the drop cast devices was the following:

- Pretreatment with "First Contact" for at least 15 minutes
- Evaporation of the 50 nm thick gold electrodes through a shadow mask (channel length = 25 µm, chamber pressure p $\approx 9 \cdot 10^{-7}$ mbar)
- Annealing step for 5 minutes at 150 °C
- Cooling of the device for about 30 minutes
- Drop casting from solution in toluene containing 1 wt.% of TIPS pentacene
- Annealing step for 10 minutes at 60 °C

Every step (except the evaporation of the gold electrodes) was done under ambient conditions. The solution was mixed with a magnetic stirrer for 15 minutes (600 rpm) before depositing it on the device.
The gold electrodes were evaporated before the semiconductor was deposited (bottom contact geometry).

Figure 4.8 and 4.9 show linear and logarithmic plots of the transfer characteristics of a drop cast devices measured after 15 hours and 48 hours respectively. The performance of that device measured 48 hours later (figure 4.9) is slightly better, mobility as well as on/off ratio increased[3] (see section 6.1).

[3]Gate voltage interval differs between figure 4.8 and figure 4.9

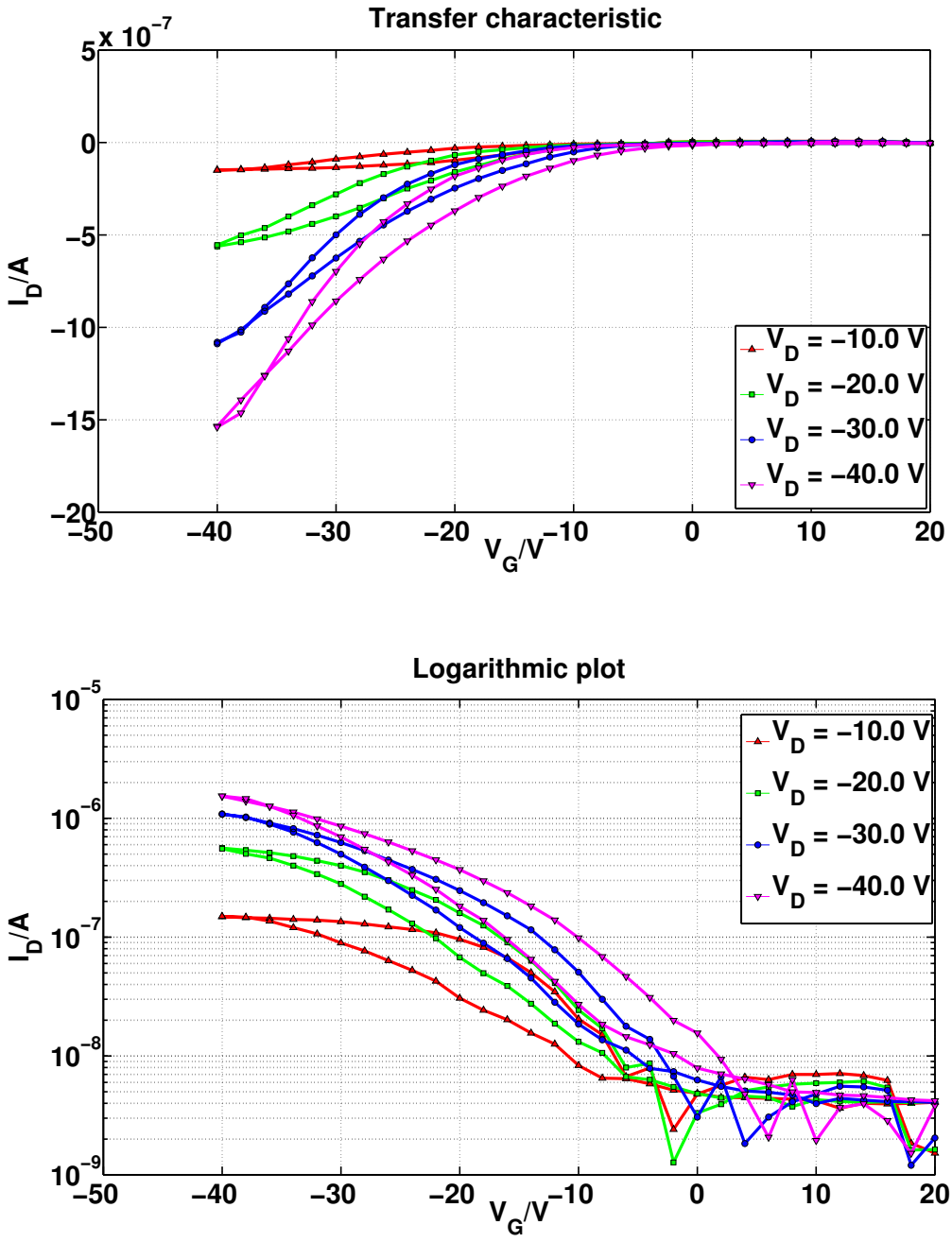


Figure 4.8.: Linear (top) and logarithmic (bottom) plots of the transfer characteristics of a drop cast device from 1 wt.% solution in toluene for different drain voltages (bottom contact geometry). The transistors were measured after 15 hours. The mobility calculated in the saturation regime (at V_D = -40 V) is $\mu = 2 \cdot 10^{-4}$ cm^{2}V^{-1}s^{-1}.

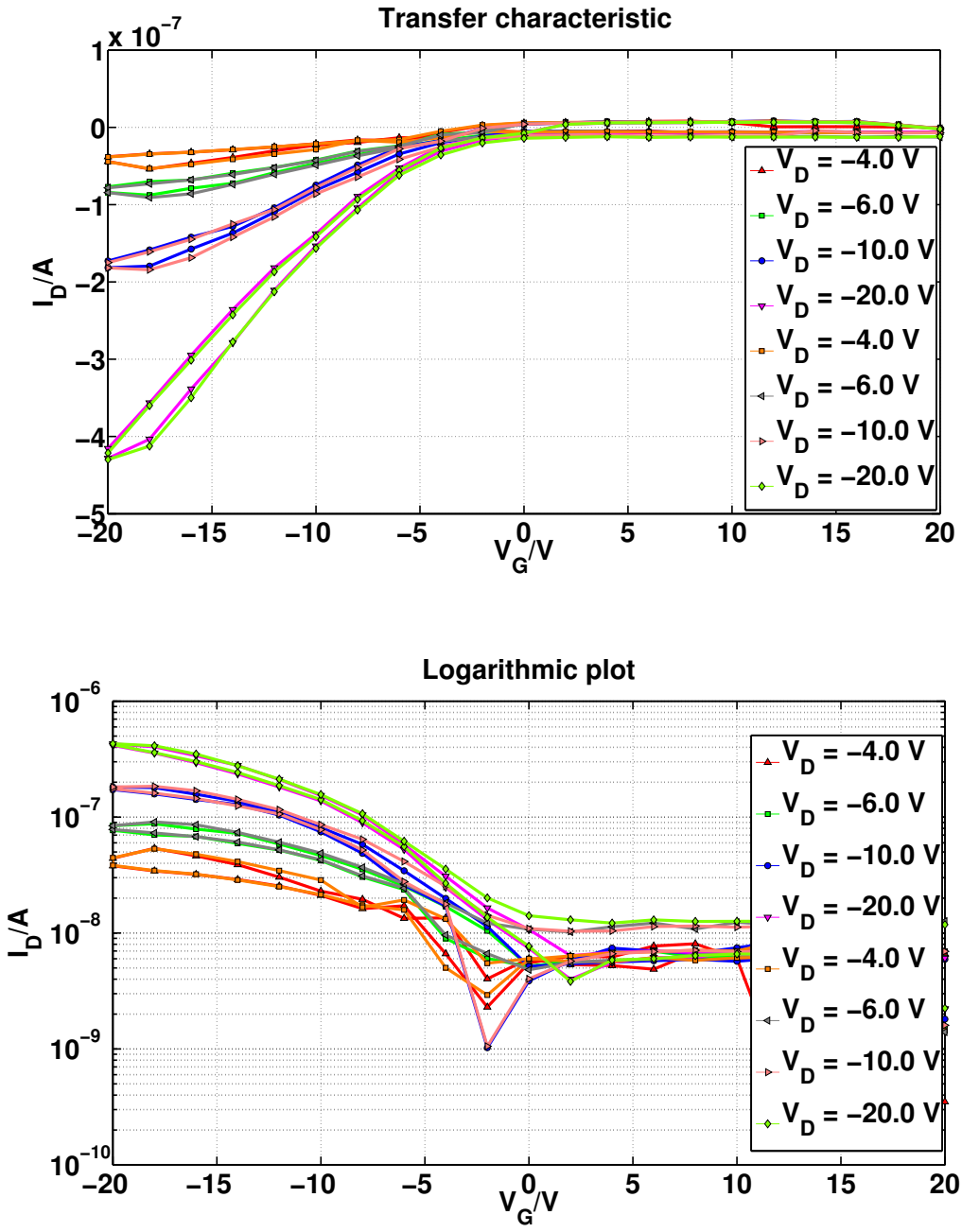


Figure 4.9.: Linear (top) and logarithmic (bottom) plots of a transfer characteristics of a drop cast device from 1 wt.% solution in toluene for different drain voltages. The transistors were measured after 48 hours. The mobility calculated in the saturation regime (at V_D = -20 V) is $\mu = 3 \cdot 10^{-4}$ cm^{2}V^{-1}s^{-1}.

Table 4.2 summarizes the most important parameters of the drop cast device from figure 4.9. Mobility and threshold voltage was extracted in the liner regime (μ_{lin} via transconductance) as well as in the saturation regime (μ_{sat} via slope of the linear fit in the transfer characteristic taking the square root of the drain current, see chapter 2).

Table 4.2.: Device parameters of a drop cast device from 1 wt.% solution in toluene. Note for the empty cells: The calculation of the parameters is not reasonable in this regime.

V_D [V]	μ_{lin} [$cm^2V^{-1}s^{-1}$]	μ_{sat} [$cm^2V^{-1}s^{-1}$]	$V_{TH,lin}$ [V]	$V_{TH,sat}$ [V]
-4	$1.0 \cdot 10^{-4}$		0.2	
-6	$1.2 \cdot 10^{-4}$		1.4	
-10	$1.6 \cdot 10^{-4}$		1.5	
-20	$2.0 \cdot 10^{-4}$	$3.0 \cdot 10^{-4}$	5.0	1.0

Figure 4.10 shows the corresponding output characteristics of the drop cast device from figure 4.9 (measured 48 hours after fabrication). The saturation behavior is quite bad further it is observable that the contact resistance plays an important role.

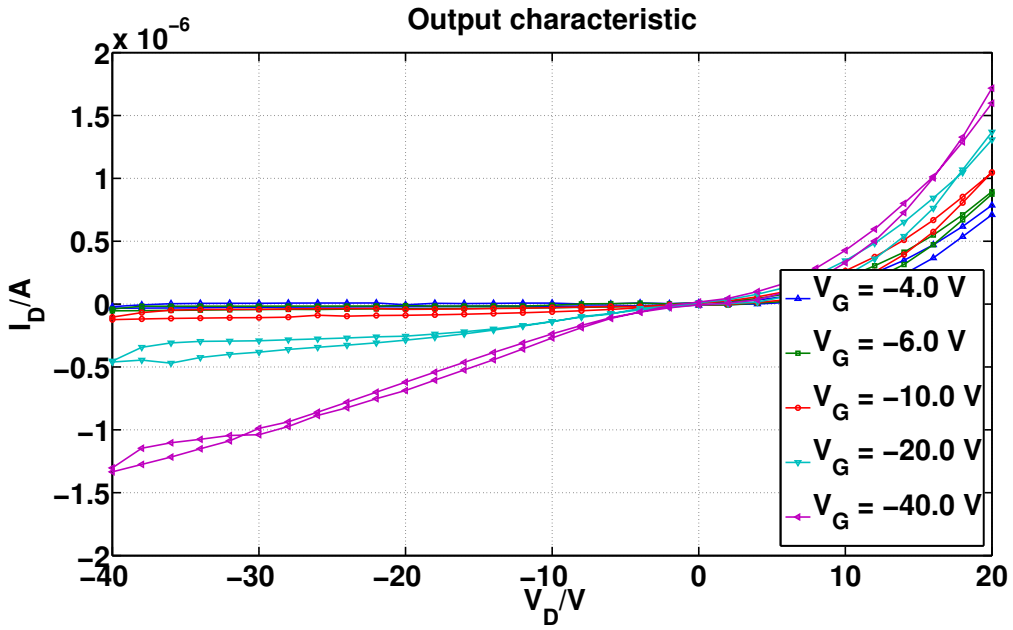


Figure 4.10.: Output characteristics of a drop cast device measured 48 hours after fabrication (1 wt.% solution in toluene). The saturation behavior is quite bad for drop cast devices.

4.2.1. Problems

Figure 4.11 shows a drop cast device (bottom contact geometry). The surface of such drop cast substrates is really rough because of the formation of very big crystallites. Due to these big crystallites it is hardly possible to characterize devices with top contact geometry because the gold gets displaced by the probing tips. Therefore, the characterization can just be done once in the best case.
Moreover, the crystallizations happen differently on each transistor on the same substrate. This leads to the problem that severe fluctuations of the device performance occur on each substrate, which renders the results difficult to reproduce.

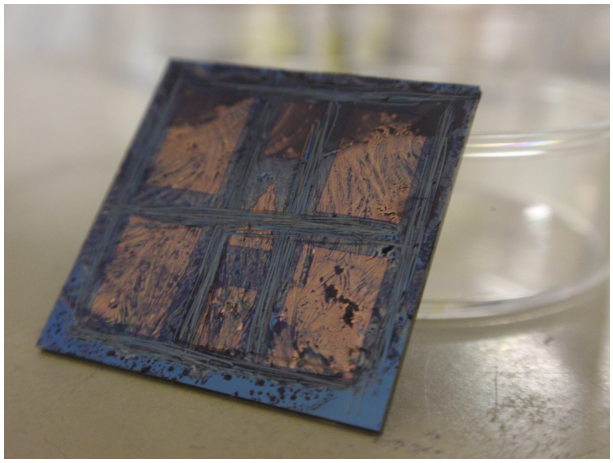


Figure 4.11.: Rough surface of a drop cast device (bottom contact geometry). The semiconductor was drop cast from solution in toluene containing 1 wt.% of TIPS pentacene.

4.2.2. Conclusion

Drop casting is an easy way to form layers on a substrate. The achieved results show medium performance (the mobility of drop cast devices are in a range of $3 \cdot 10^{-4}$ $cm^2V^{-1}s^{-1}$) in comparison to other techniques (see below).
However, the big problem is the more or less the random crystallization of the semiconductor material on each transistor on each substrate. Therefore, the device performance differs significantly from one device to another (factor 10). The next problem is the rough surface therefore, just bottom contact geometry devices can be fabricated.

Important to mention is that no device operates right after depositing the semiconductor on the gold electrodes. The drop cast devices started to operate approximately after after 15 hours past production. If one measures the device before, the characteristics look hardly like transistor characteristics. One reason for that behavior is, that especially in case of the drop cast devices, the solvent has to evaporate totally before the current can flow.
The time evolution of solution processed TIPS pentacene devices will be discussed in detail in section 6.1.

4.3. Deposition of TIPS Pentacene via Spin Coating

Spin coating is a well known technique for depositing thin films on substrates. The big advantages are that the deposited layers are formed homogeneously as well as that the thickness of the layers can be controlled, on the one hand by the spin parameters and on the other hand, by the concentration of the solution deposited on the substrate. Further, with the spin coating process it is relatively simple to reproduce the device performance.

The crystallization of the molecules (ordering of the molecules) through spin coating is not comparable to the other techniques (dip coating or drop casting processes) due to the fast process speed. Compared to drop cast devices, where the molecules have enough time to order in a low energy state, the spin coating process happens so fast and leads to lower ordering (higher entropy).

Figure 4.12 shows the spin coating setup including an infra red (IR) lamp. The IR lamp was used for heating the substrate which leads to operating devices. Without heating the substrate neither top contact nor bottom contact devices with toluene as solvent were operating.

The spin coater was located in a laminar flow box to ensure the cleanness of the substrate. The whole process was done under ambient conditions.
To keep the temperature of the spin coater during the heating process low, a fan was located next to the spin coater. Spin coaters usually stop operating if their temperature becomes too high.

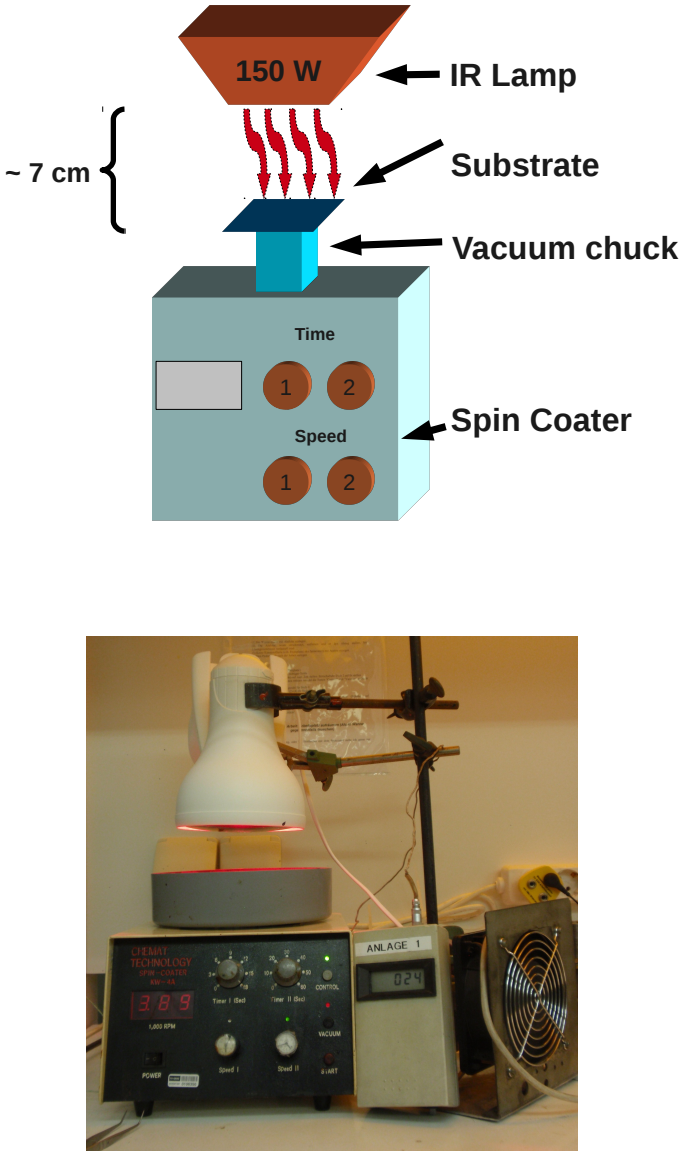


Figure 4.12.: Top: Schematic illustration of the spin coating setup including an IR lamp to heat the substrate. Bottom: Picture of the real setup. The fan on the right hand side is responsible for cooling the spin coater to reduce its temperature.

Procedure

The IR lamp was located 7 cm above the substrate to assure 60 °C substrate temperature in a moderate time (between 3 and 5 minutes).

Two different solutions were used during the process.

- Toluene containing 1 wt.% of TIPS pentacene (approximately 10 mg/ml)
- 3,4 Dimethylanisole containing 1.5 wt.% of TIPS pentacene (approximately 15 mg/ml)[4]

The following parameters turned out to yield to the best device performances:

- Mixing of the solvent for at least 15 minutes with a magnetic stirrer at 600 rpm to ensure high solubility
- Deposition of "First Contact" for at least 20 minutes
- Detaching of "First Contact" layer
- Evaporation of the 50 nm thick gold electrodes (channel length 25 µm, chamber pressure p $\approx 9 \cdot 10^{-7}$ mbar)
- Spin coating of solution at 60 °C substrate temperature
  - First 18 s at 2000 rpm
  - Afterwards 20 s at 4000 rpm
  - Amount of solution: 150 µl (substrate is totally covered with solution)

[4]This optimized concentration yields to homogeneous wetting of the substrate

4.3.1. Effects of Substrate Heating on the Device Performance

Figure 4.13 shows the Θ/2Θ scans of a spin coated layer fabricated on a substrate at room temperature (RT) and at 60 °C, respectively. Toluene was used as solvent for both cases. The peak intensities change (higher intensities for the heated substrate) which correlates with a change of the ordering of the TIPS pentacene molecules in the bulk. From figure 4.13 it can also be seen that the deposited layer is textured because only the (00L) and the (011) Bragg peaks are observed (two dimensional powder); i.e. two species of differently oriented crystallites are present in the film.[48]

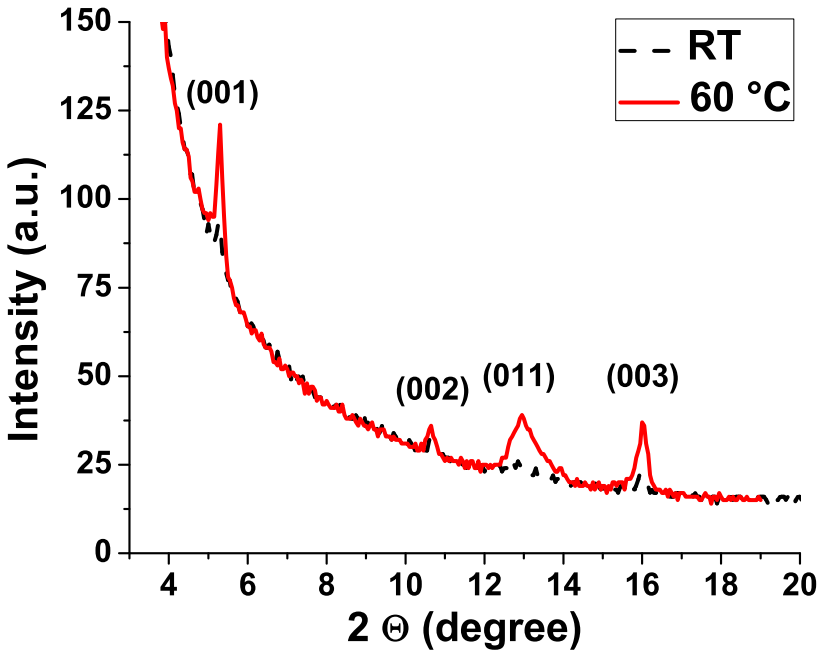
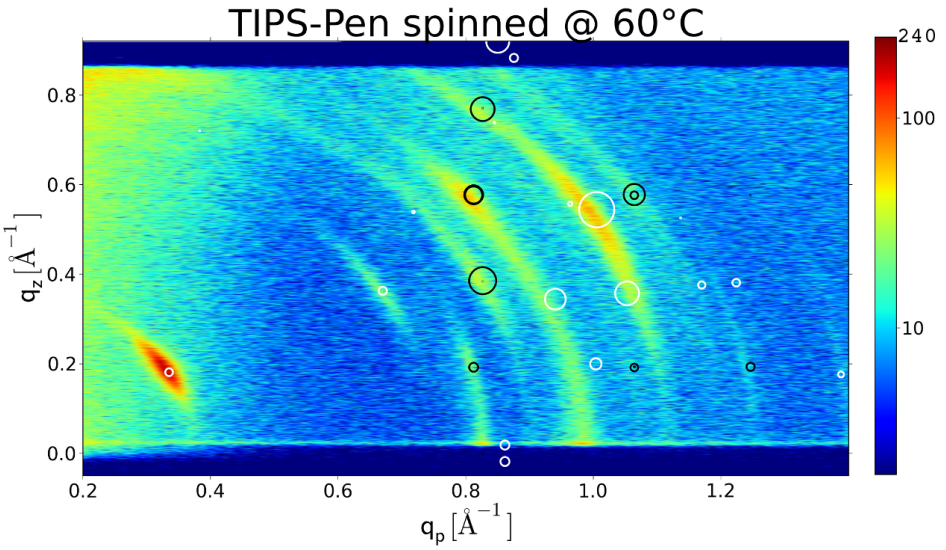
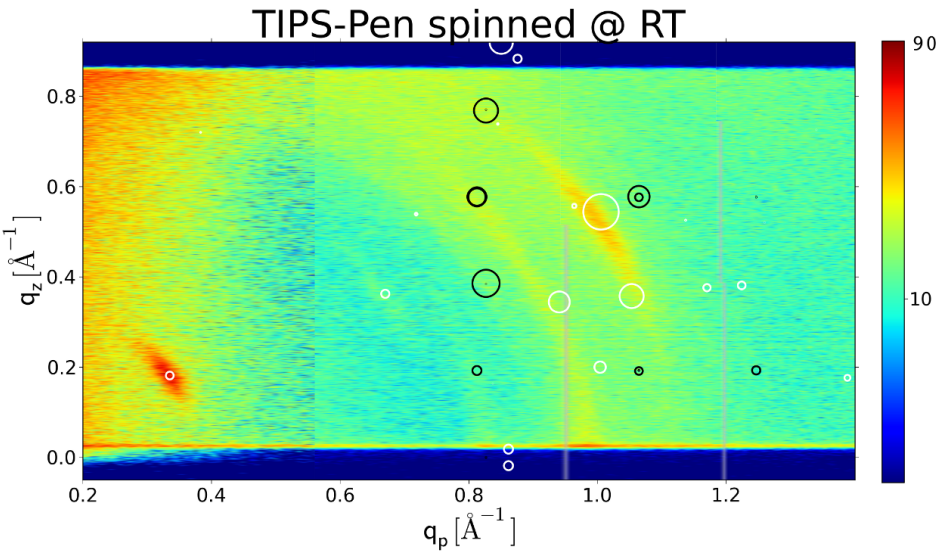


Figure 4.13.: Θ/2Θ scan of a spin coated TIPS pentacene layer (solved in toluene) deposited on a silicon substrate at room temperature (RT) and at 60 °C substrate temperature, respectively.

To further clarify the structure, GIXRD measurements (measured and analyzed by A. Moser) on spin coated TIPS pentacene layers have been performed (figure 4.14). The layers were spin coated from a solution containing 1 wt.% TIPS pentacene dissolved in toluene. The substrate temperature during the spin coating process was kept at room temperature and at 60 °C, respectively.



(a)



(b)

Figure 4.14.: GIXRD image of a TIPS pentacene layer spin coated from toluene. Substrate temperature was kept at 60 °C (a) and at room temperature (b) during the spin coating process. The white rings indicate the expected Bragg peak positions of the bulk phase with (011) orientation, the black rings the expected Bragg peak positions of the thin film phase with (001) orientation. The measured intensity is shown with a logarithmically scaled color map. Courtesy of Armin Moser.

The absolute intensity of the peaks is higher when the TIPS pentacene layer is spun at 60 °C. This correlates with crystallinity; i.e. higher intensity means higher degree of crystallinity, which is always preferable for the device performance.
Next, two different phases occur in the GIXRD images, namely the thin film phase and the the bulk phase. I.e. the unit cells as well as the packing of the molecules within the unit cell are different.[49] Also from the GIXRD images it can be determined which lattice plane of the crystallites are parallel to the substrate surface. While this is the (001) plane for the thin film phase, the bulk phase is oriented with the (011) plane parallel to the substrate surface. This agrees with the $\Theta/2\Theta$ experiment, where exclusively (001) and (011) peaks are observed.[48]
Those substrates which have been spin coated at room temperature show hardly any (001) oriented thin film phase but just (011) orientated bulk phase. This can be identified in figure 4.14 (b) were the black rings indicate the (001) thin film phase (more or less no peak intensity), the white rings the (011) bulk phase.
On the other hand the 60 °C spin coated substrates shows (001) orientated thin film phase which can be identified from the good correlation of the black rings with the diffraction peaks in figure 4.14 (a).
From the knowledge of the crystal structure and the unit cell orientation, the orientation of the molecules with respect to the substrate can be analyzed (figure 4.15 and 4.16). In the first case (figure 4.15, substrate temperature 60 °C) the side chains of the TIPS pentacene do not disturb the overlap of the pentacene rings in the needed direction. Therefore, a current can flow parallel to the substrate from source to drain because of the preferable overlap of the delocalized π orbitals in this direction.
This situation is different in figure 4.16. The orientation of the TIPS pentacene molecules is not preferable for good charge transport, parallel to the substrate. Therefore, the charge carrier mobility is lower.

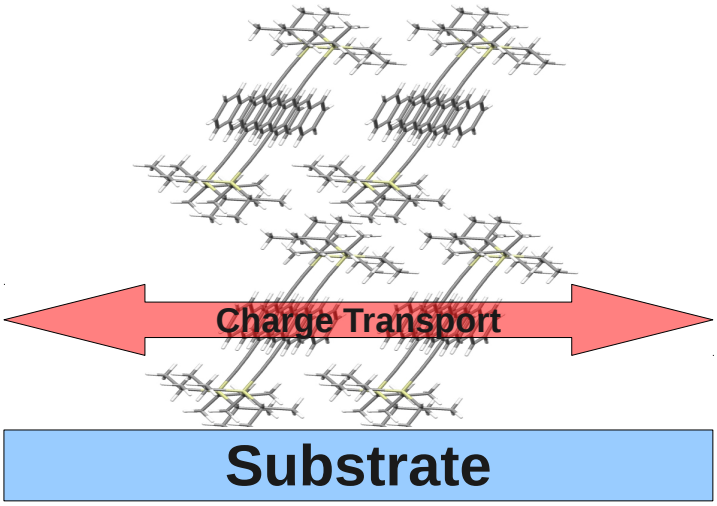


Figure 4.15.: (001) orientation of the TIPS pentacene molecules spin coated on a substrate with a temperature of 60 °C. The overlap of the delocalized π orbitals allows the preferable charge transport from source to drain. Courtesy of Armin Moser.

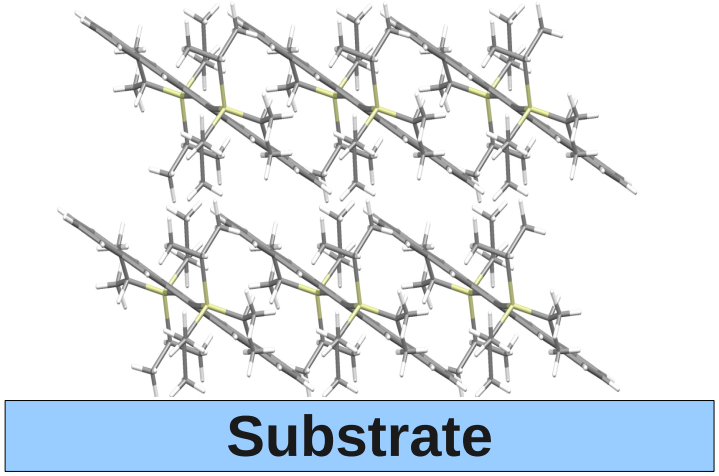


Figure 4.16.: (011) orientation of the TIPS pentacene molecules spin coated on a substrate kept at room temperature. This orientation is not the preferred one for charge transport parallel to the substrate. Courtesy of Armin Moser.

4.3.2. Toluene as Solvent - Device Performance

Top contact as well as bottom contact were used as device geometry. In general it can be seen that bottom contact devices show better device performance than top contact.

Toluene as Solvent

Figure 4.17 shows linear and logarithmic plots of the transfer characteristics of a top contact device. The substrate temperature during the spin coating process was 60 °C. The results show transistor behavior but the performance is very bad. Those devices show big hysteresis and very low currents. However, without heating the substrate no operating devices were built at all.
Figure 4.18 shows again linear and logarithmic plots of the transfer characteristics of a spin coated device. The substrate temperature during the spin coating process was again 60 °C but now bottom contact geometry was used.
The device performance is much better compared to the top contact devices:
Hardly any hysteresis is observable and the on/off ratio increased by 1000. The achieved mobility is in the same range as published one from Choi et al. [50] an lies around $\mu = 7 \cdot 10^{-4}$ $cm^2V^{-1}s^{-1}$. Important to mention is that this result is totally reproducible.

Table 4.3 lists the obtained results of spin coated, bottom contact devices using toluene as solvent.

Table 4.3.: Device parameters of a bottom contact, spin coated TIPS pentacene device from 1 wt.% solution in toluene. The substrate temperature was 60 °C during the spin coating process.

$V_{\mathbf{D}}$ [V]	$\mu_{\mathbf{lin}}$ [$\mathbf{cm^2V^{-1}s^{-1}}$]	$\mu_{\mathbf{sat}}$ [$\mathbf{cm^2V^{-1}s^{-1}}$]	$V_{\mathbf{TH,lin}}$ [V]	$V_{\mathbf{TH,sat}}$ [V]
-80	$2 \cdot 10^{-4}$	$7 \cdot 10^{-4}$	-6.3	-28.4

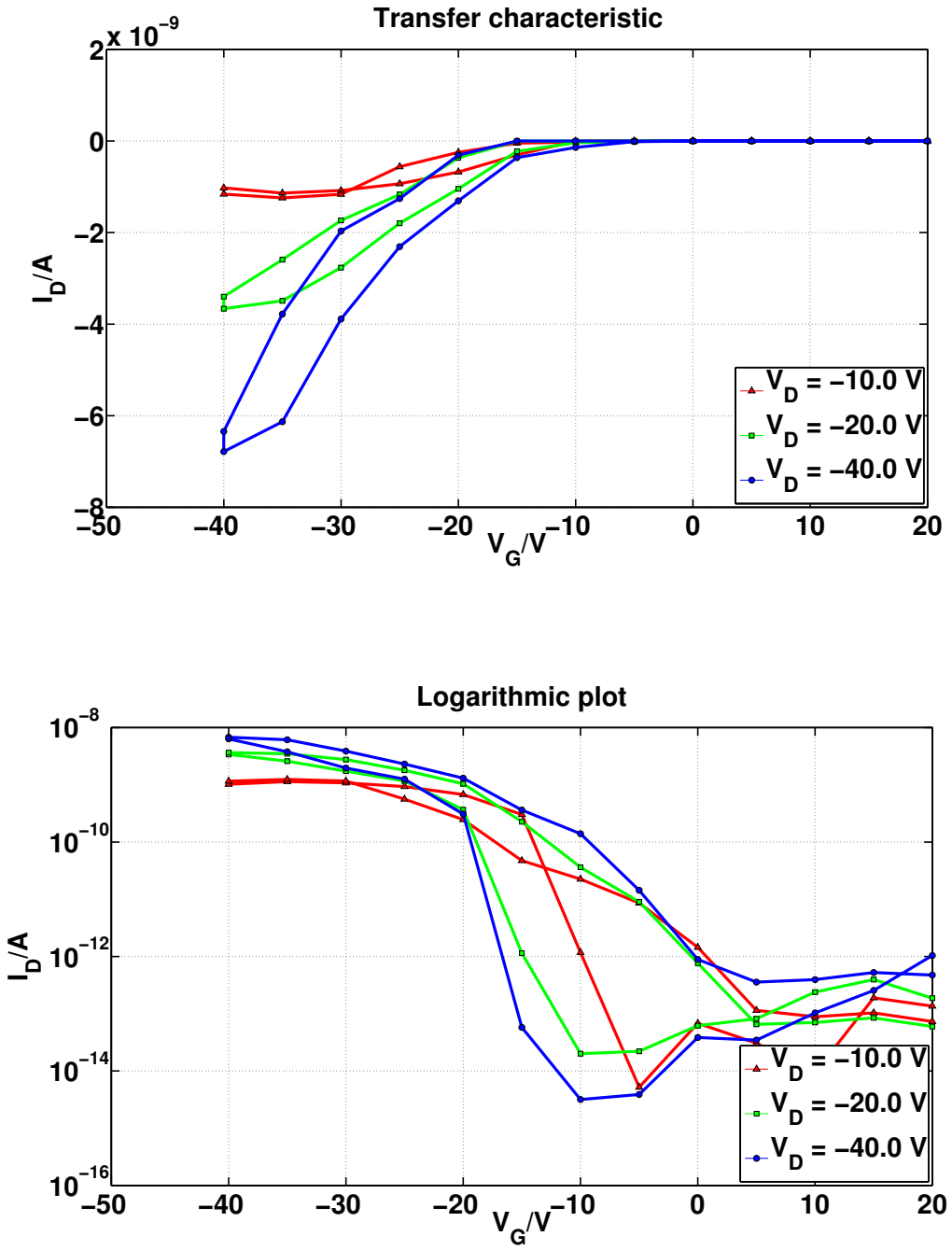


Figure 4.17.: Linear (top) and logarithmic (bottom) plots of the transfer characteristics of a TIPS pentacene device (top contact geometry), spin coated from 1 wt.% solution in toluene for different drain voltages. The substrate temperature was 60 °C during the spin coating process. This device was measured after seven days of storage under ambient conditions.

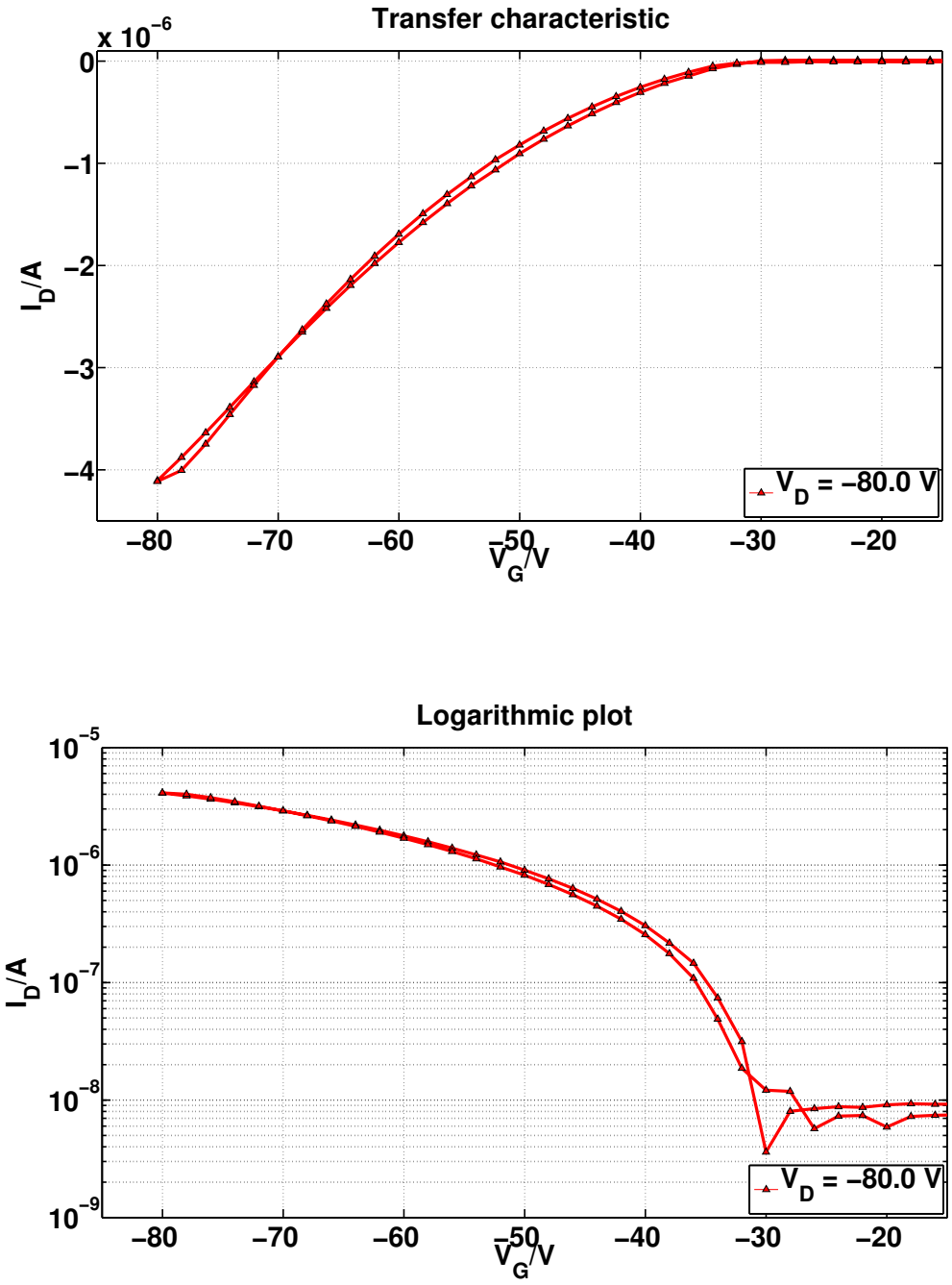


Figure 4.18.: Linear (top) and logarithmic (bottom) plots of the transfer characteristics of a TIPS pentacene device (bottom contact geometry), spin coated from 1 wt.% solution with toluene for different drain voltages. The mobility calculated in the saturation regime is $\mu = 7 \cdot 10^{-4}$ cm^{2}V^{-1}s^{-1}.

Negative Turn On Voltage

In general, spin coated devices using toluene as solvent show quite negative threshold voltages (see table 4.3). There are two reasons for that behavior:

- **Bias stress effect:**

  By applying high voltages (gate and drain) a shift of several volts occur because of space charges or filled traps. If high (negative) gate voltages (between -60 and -80 V) are applied the threshold voltage is sifted to more negative values. In case of spin coated TIPS pentacene devices this shift is not going backwards with time. This shift remains constant after the first measurement.
  If gate voltages in a range of maximum -40 V are applied, this shift is hardly observable.

- **Contact resistance:**

  The charge carriers have to overcome a quite high injection barrier to get into the conducting channel. A higher field is needed which can be achieved by applying higher voltages. Especially when using bottom contact geometry the contact resistance plays an important role.[51] Figure 4.19 shows the output characteristic of a spin coated TIPS pentacene device. The substrate temperature was again 60 °C. There is a deviation from a straight line in the linear regime (indicated by the arrows) which means that the contact resistance has an impact on the device performance (compare with section 2.3.2).[27]

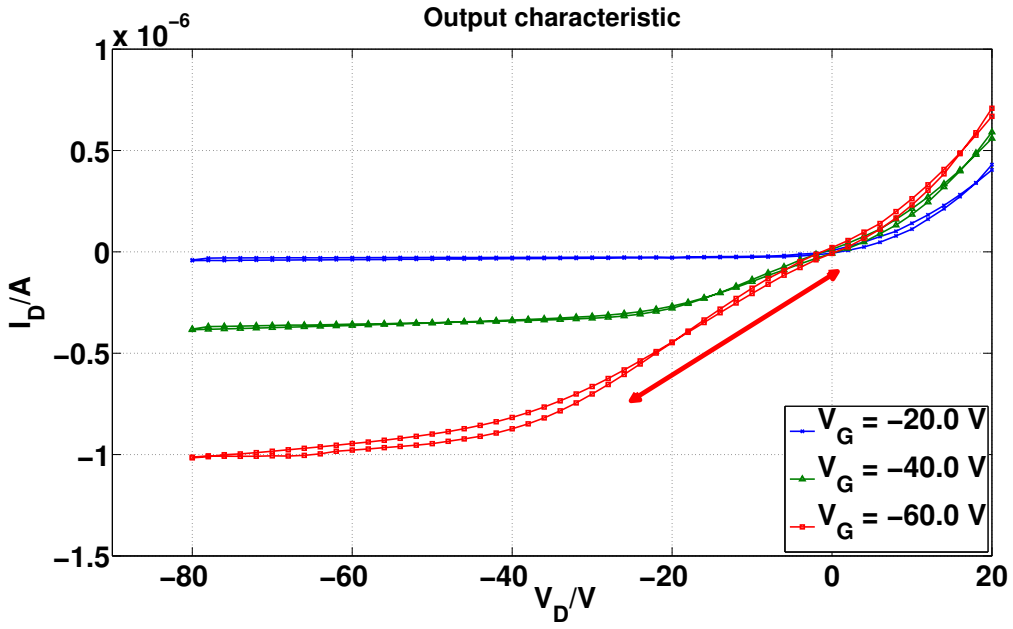


Figure 4.19.: Output characteristics of a spin coated TIPS pentacene device. The substrate temperature was 60 °C during the spin coating process. The arrows indicate the deviation from the straight line, ergo the contact resistance plays an important role in the device performance.

Layer Thickness of Spin Coated Devices

To gain more information about the deposited spin coated semiconductor material, X-Ray Reflectivity (XRR) measurements (measured by A. Neuhold) were performed. Figure 4.20 shows the result including the fit. Table 4.4 sums up the obtained values.

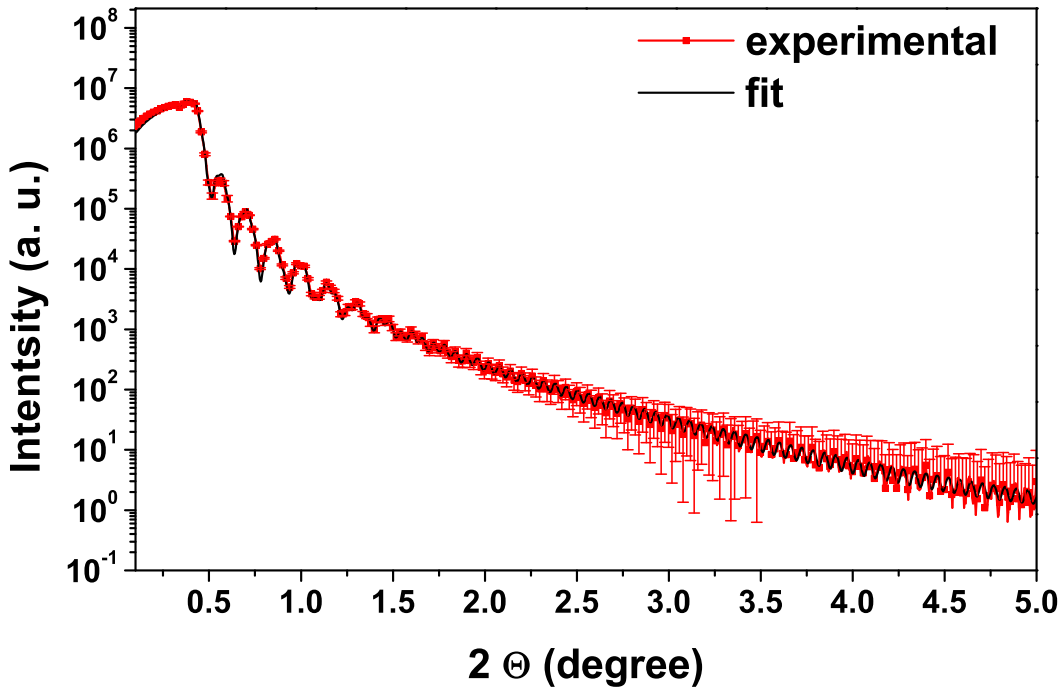


Figure 4.20.: XRR measurement of a spin coated TIPS pentacene device with 1 wt.% solution in toluene (substrate temperature 60 °C). Measured and analyzed by Alfred Neuhold.

Table 4.4.: Layer thickness and roughness of a spin coated (substrate temperature 60 °C) TIPS pentacene device with 1 wt.% solution in toluene.

Parameter	Value [nm]	Lower error [nm]	Upper error [nm]
Thickness	55.7	55.5	55.9
Roughness	2.2	1.9	2.6

4.3.3. XRD Measurements - 3,4-Dimethylanisole

The reason for performing XRD measurements on spin coated 3,4-Dimethylanisole devices (substrate temperature 60 °C) was primary to understand why those devices show better performance (see below).
Figure 4.21 shows a Θ/2Θ scan of a spin coated TIPS pentacene substrate using 3,4-Dimethylanisole as solvent (concentration 1.5 wt.%). The substrate temperature was kept at 60 °C during the spin coating process.
The (00L) oriented peaks show higher intensities than when using toluene as solvent, which is an evidence for a higher degree of order. Important to mention is that the (011) peak is hardly observable, which means that this orientation, which limits the current from source to drain, does not occur. This is the reason why devices using 3,4-Dimethylanisole as solvent show better device performance than using toluene as solvent.

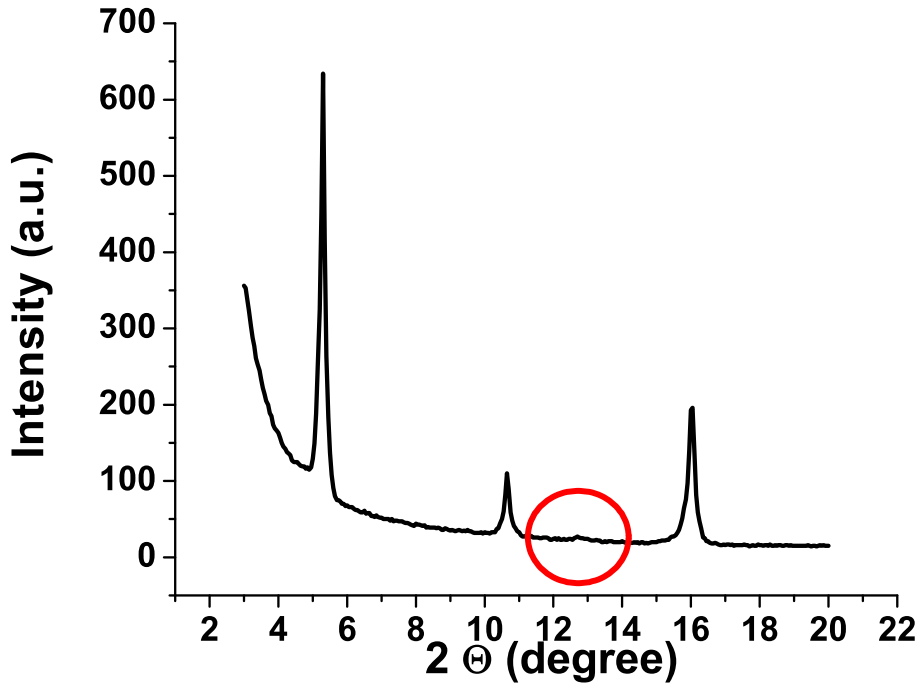


Figure 4.21.: Θ/2Θ scan of a spin coated substrate using 3,4-Dimethylanisole as solvent (substrate temperature 60 °C, concentration 1.5 wt.%).

4.3.4. 3,4-Dimethylanisole as Solvent - Device Performance

Figure 4.22 shows the linear and logarithmic plots of the transfer characteristics of a bottom contact device spin coated from 1.5 wt.% solution with 3,4-Dimethylanisole for different drain voltages. The substrate temperature was 60 °C during the spin coating process. Table 4.5 lists the mobilities and the threshold voltages.

The device performance is much better than when using toluene as solvent. The reason for this behaviors is that 3,4-Dimethylanisole has a much lower vapor pressure and the molecules have more time to go in a lower energy state which correlates with higher ordering. As explained above the (011) direction, which limits the current in the toluene based devices, is not observable in the XRD measurements.

Bottom contact devices are favorable, because it is very difficult to spin a homogeneous layer on the substrate without gold electrodes on it.

Table 4.5.: Device parameters of a bottom contact, spin coated device from 1 wt.% solution in 3,4-Dimethylanisole. The substrate temperature was 60 °C during the spin coating process. Note for the empty cells: The calculation of the parameters is not reasonable in this regime.

$V_{\mathbf{D}}$ [V]	$\mu_{\mathbf{lin}}$ [$\mathbf{cm^2V^{-1}s^{-1}}$]	$\mu_{\mathbf{sat}}$ [$\mathbf{cm^2V^{-1}s^{-1}}$]	$V_{\mathbf{TH,lin}}$ [V]	$V_{\mathbf{TH,sat}}$ [V]
-10	$1.0 \cdot 10^{-3}$		-0.1	
-20	$1.3 \cdot 10^{-3}$	$1.8 \cdot 10^{-3}$	-5.3	-8.3
-40	$1.7 \cdot 10^{-3}$	$2.8 \cdot 10^{-3}$	-3.1	-11.3
-60	$2.1 \cdot 10^{-3}$	$3.5 \cdot 10^{-3}$	-1.0	-12.9

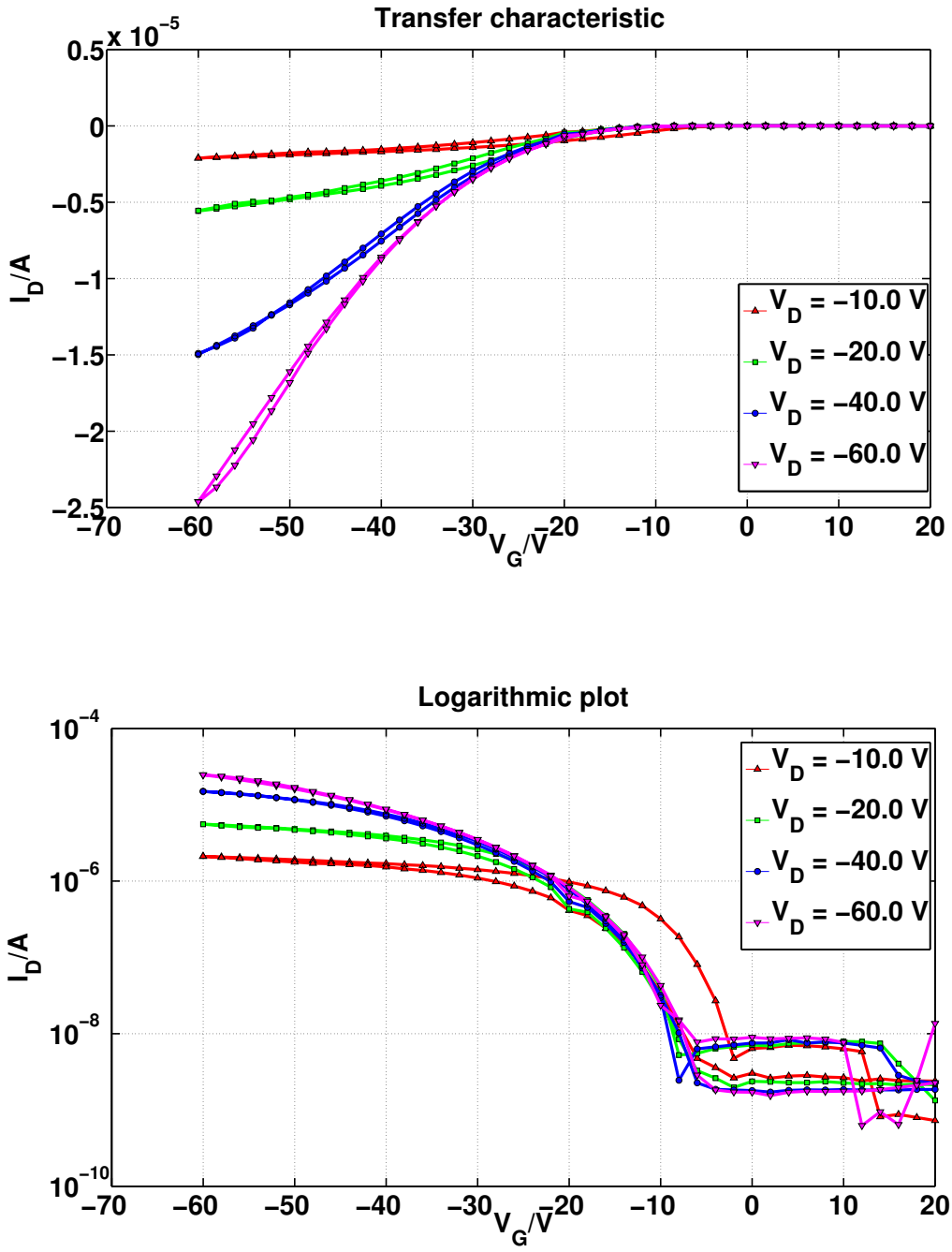


Figure 4.22.: Linear (top) and logarithmic (bottom) plots of the transfer characteristics of a TIPS pentacene device (bottom contact geometry), spin coated from 1 wt.% solution with 3,4 Dimethylanisole for different drain voltages. The mobility fitted in the saturation regime (at V_{D} = -60 V) is $\mu = 3.5 \cdot 10^{-3}$ $\mathrm{cm^2V^{-1}s^{-1}}$.

Figure 4.23 shows the corresponding output characteristic of a spin coated TIPS pentacene device using 3,4-Dimethylanisole as solvent. Such devices show a really good saturation behavior.

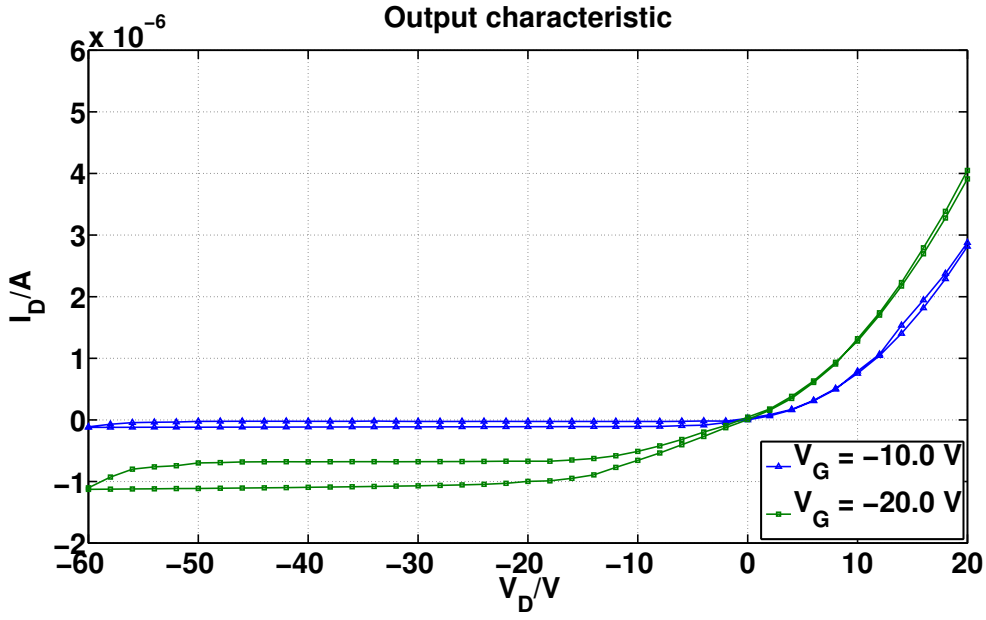


Figure 4.23.: Output characteristics of a spin coated TIPS pentacene device using as 3,4-Dimethylanisole solvent (concentration 1.5 wt.%). The substrate temperature was 60 °C during the spin coating process.

4.3.5. Conclusion

Spin coating enable to produce a homogeneous layer on a substrate. Using toluene as solvent does not lead to operating devices without heating of the substrate. Therefore, the whole spin coating setup was changed and an IR lamp was included in the production process.

Top contact devices show very bad over all performance. However, bottom contact devices show quite good performance and are totally comparable with recent published results from Choi et al.[50] The mobilities of bottom contact devices are in the order of 10^{-4} using toluene as solvent and in the order of 10^{-3} using 3,4-Dimethylanisole as solvent, respectively.

The reason for the better performance of 3,4-Dimethylanisole devices is that the (011) orientation which limits the current is not observable in the XRD measurements. The (001) direction is more intense and the alignment of the molecules is more preferred, therefore more current can flow from source to drain through the channel.

Important to mention is that in both cases 90% of the transistors are operating and that all of the result are fully reproducible. All devices show similar performance and hardly any hysteresis.

4.4. Thermal Evaporation of TIPS Pentacene

As mentioned a couple of times before, one of the main advantage of TIPS pentacene compared to pentacene is that TIPS pentacene is soluble. Therefore, it can be used for solution processed techniques which is not possible for usual pentacene. However, Sheraw et al. published promising results of thermally evaporated TIPS pentacene with mobilities up to 0.4 $cm^2V^{-1}s^{-1}$ and on/off ratios of about 10^5.[52]
One big advantage of thermal evaporation is that the evaporated layers are homogeneous and distributed uniformly over the substrate. The roughness of the deposited layers is low which is beneficial for device production. Therefore, both kinds of geometries (bottom or top contact) are realizable, and the thickness of the layer can be adjusted and controlled.
The reason for the use of thermal evaporation of TIPS pentacene in this thesis was to compare solution based techniques to the standard evaporation technique.

4.4.1. Setup

To evaporate organic materials with the available equipment, a couple of changes of the evaporation chamber had to be made. Instead of the tungsten boat used for evaporating the gold electrodes, a simplified Knudsen cell was made out of glass (length 1.5 cm, inner cross section 4.8 mm, outer cross section 6.8 mm). Around this glass tube a “kanthal” wire was coiled and fixed to the electrodes of the vacuum chamber. The current flows through the wire, heats the glass tube and the substance in it.
With these changes the outgoing particle beam is much more directed than with a normal tungsten boat. Therefore, less material is needed which makes the whole process much more efficient. In this way controlled deposition of the semiconductor material is possible.
Major disadvantages of this certain setup is that the substrate can not be heated. Moreover, the control of the evaporation rate can not be done precisely with the available equipment.

Figure 4.24 shows the improved setup of the evaporation chamber including the Knudsen cell.

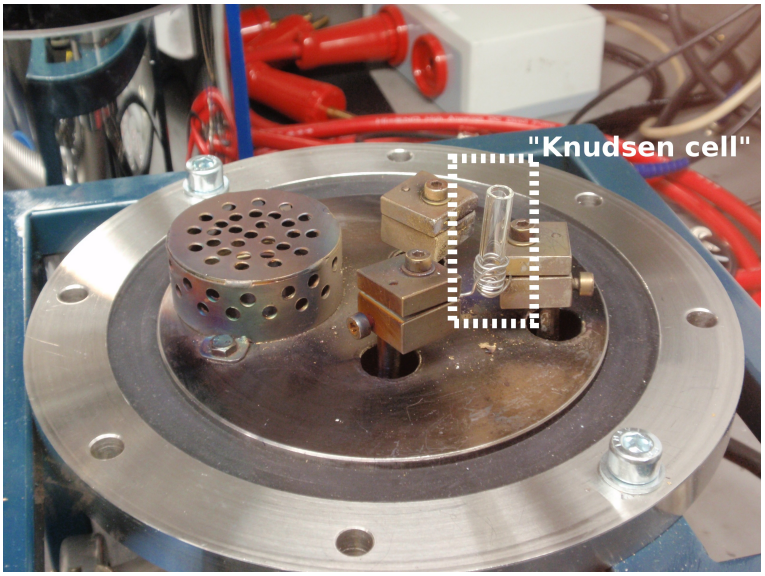


Figure 4.24.: Setup of the modified thermal evaporation chamber. The substance is filled in the glass cell and gets heated through the "kanthal" wire coiled around. The outgoing beam is directed and allows controlled deposition of the semiconductor material.

Procedure

The sample were produced as follows:

- Plasma etching for 20 seconds
  - Power level: maximum
  - Chamber pressure filled with air: 2 mbar
  - Chamber pressure filled with Oxygen: 4 mbar
- CO_2 cleaning
- Evaporation of the TIPS pentacene layer
- Change to another evaporation chamber in the argon glove box
- Evaporation of the gold electrodes through a shadow mask

4.4.2. XRD Measurements - Thermal Evaporation

Figure 4.25 shows the XRD measurement for a thermally evaporated TIPS pentacene layer. The layer thickness was approximately 40 nm (evaporation chamber pressure p $\approx 2 \cdot 10^{-6}$ mbar). The peaks are very sharp and show high intensities which again correlates with higher ordering.
As seen in section 4.3.3, only the (001) orientations, and not the (011) orientations, are observable. Therefore, the thermally evaporated TIPS pentacene devices show the best device performance (see below) because they provide the highest ordering which correlates with the peak intensities. Moreover, the current limiting (011) orientation is not observed.

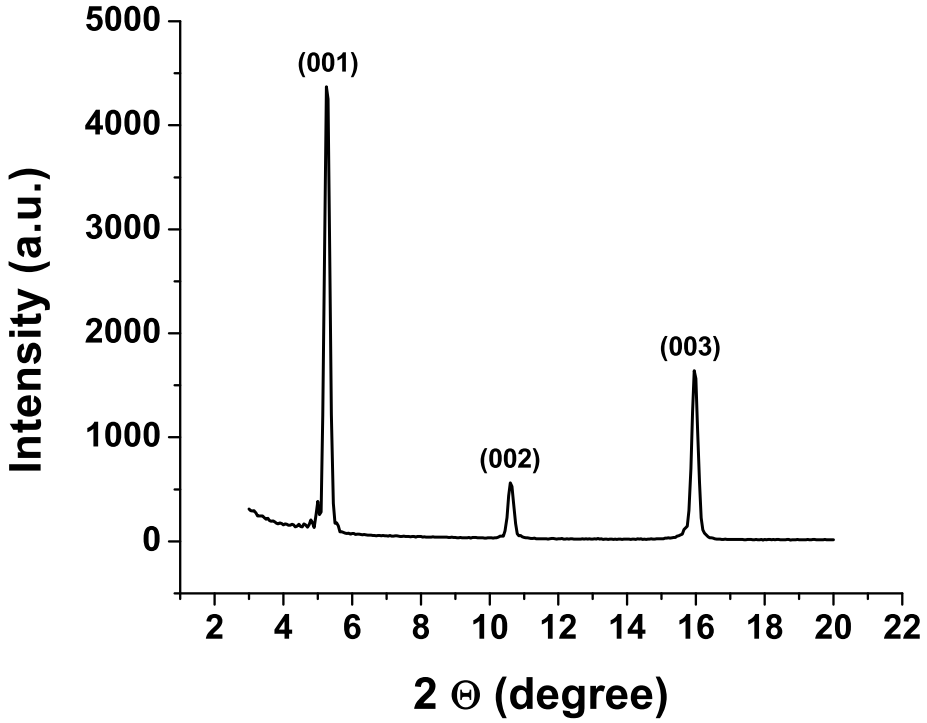


Figure 4.25.: $\Theta/2\Theta$ scan of a thermally evaporated TIPS pentacene layer in a silicon substrate.

4.4.3. Device Performance

Figure 4.26 shows the linear as well as the logarithmic plots of the transfer characteristics of a thermally evaporated TIPS pentacene device. The devices start to operate right after finishing of the fabrication. The following parameters were chosen for those devices:

- Top contact geometry
- TIPS pentacene layer with approximately 85 nm (chamber pressure $p \approx 3 \cdot 10^{-6}$ mbar)
- Gold electrodes (50 nm) were evaporated through a shadow mask with 50 µm channel length (chamber pressure $p \approx 2.5 \cdot 10^{-6}$ mbar)

Table 4.6 lists the important parameters of a thermally evaporated TIPS pentacene device. Top contact geometry was used. This device was stored under ambient condition (exposure to light and air).

Table 4.6.: Device parameters of a top contact, thermally evaporated TIPS pentacene device.

$V_{\mathbf{D}}$ [V]	$\mu_{\mathbf{lin}}$ [$\mathbf{cm^2V^{-1}s^{-1}}$]	$\mu_{\mathbf{sat}}$ [$\mathbf{cm^2V^{-1}s^{-1}}$]	$V_{\mathbf{TH,lin}}$ [V]	$V_{\mathbf{TH,sat}}$ [V]
-40	0.01	0.02	-3.2	-11.6
-60	0.01	0.02	-1.5	-15.8

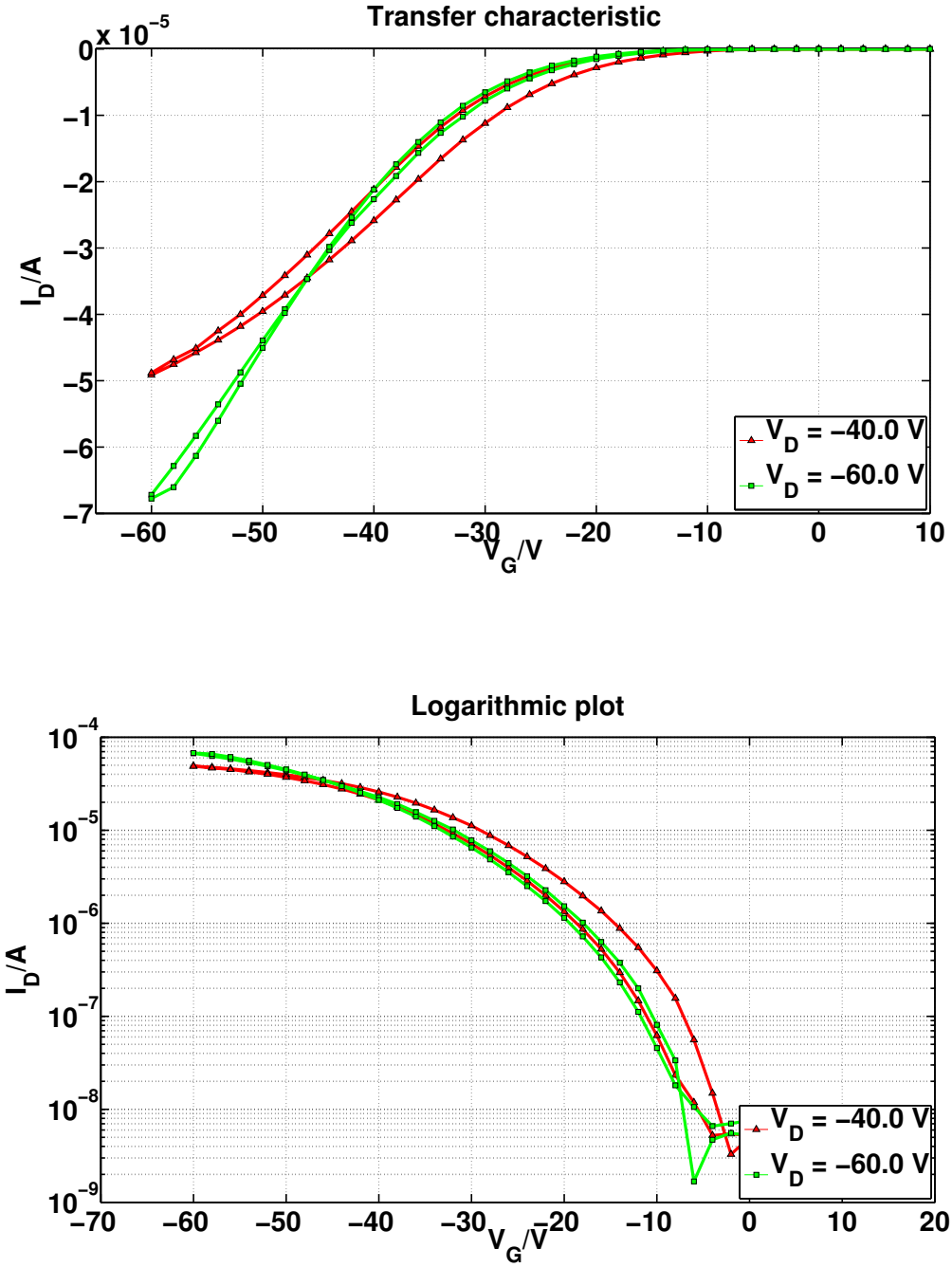


Figure 4.26.: Linear (top) and logarithmic (bottom) plots of the transfer characteristics of a thermally evaporated TIPS pentacene device for different drain voltages measured after one week. The mobility fitted in the saturation regime (at V_D = - 60 V) is μ = 0.02 $cm^2V^{-1}s^{-1}$, the on/off ratio is about 10^4.

4.4.4. Conclusion

The evaporated TIPS pentacene devices showed very good overall performance. The mobility as well as the on/off ratios are significantly larger than those of other techniques. The XRD measurements showed that for thermally evaporated TIPS pentacene the peak intensities and therefore the crystallinity is much better. Again the charge transport limiting (001) orientation is not observable.

The threshold voltage is much closer to zero and not as negative as the threshold voltage from the devices constructed with dip coating or drop casting. The reason for that is probably the contact resistance which is lower in this case (because of the top contact geometry).

These results are really impressive taking into account that the substrate was not heated during the evaporation process. Further, the evaporation rate was very fast ($\approx$ 2 nm per seconds) because of the unoptimized process.

These results show the prospect of TIPS pentacene as active semiconductor material.

4.5. Thermal Evaporation of Pentacene

Pentacene is the most used semiconductor for OTFTs and is the state of the art material for organic electronics. Pentacene as semiconductor layer leads to high mobilities as well as high on/off ratios.
As mention above, pentacene is not soluble and therefore pentacene usually gets evaporated in a vacuum camber.[31]

In this thesis the reason for evaporating pentacene was to compare the results and find the advantages and the disadvantages of different semiconductor materials. Further, it is very interesting to compare such similar materials and their quite different behavior. The setup of the evaporation chamber was the same as shown in figure 4.24.

Procedure

To compare the evaporated TIPS pentacene devices with the evaporated pentacene devices the treatment was done similar:

- Plasma etching for 20 seconds (same parameters as in section 4.4)
- CO_2 cleaning
- Evaporation of the pentacene layer (30 nm, chamber pressure p $\approx 2 \cdot 10^{-5}$ mbar)
- Evaporation of the gold electrodes (50 nm) through a shadow mask with 50 µm channel length (chamber pressure p $\approx 9 \cdot 10^{-6}$ mbar)

4.5.1. Results

Figure 4.27 shows linear and logarithmic plots of the transfer characteristics of a thermally evaporated pentacene device. Compared to published results those devices show a reasonable performance if one take into account that the Knudsen cell was home made and the pentacene was not purified (as delivered).
Those devices show high on/off ratios and mobilities up to 0.1 $cm^2V^{-1}s^{-1}$. Pentacene devices started to operate right after finishing the device fabrication. Similar like the TIPS pentacene devices they stayed very stable for weeks under inert gas conditions.

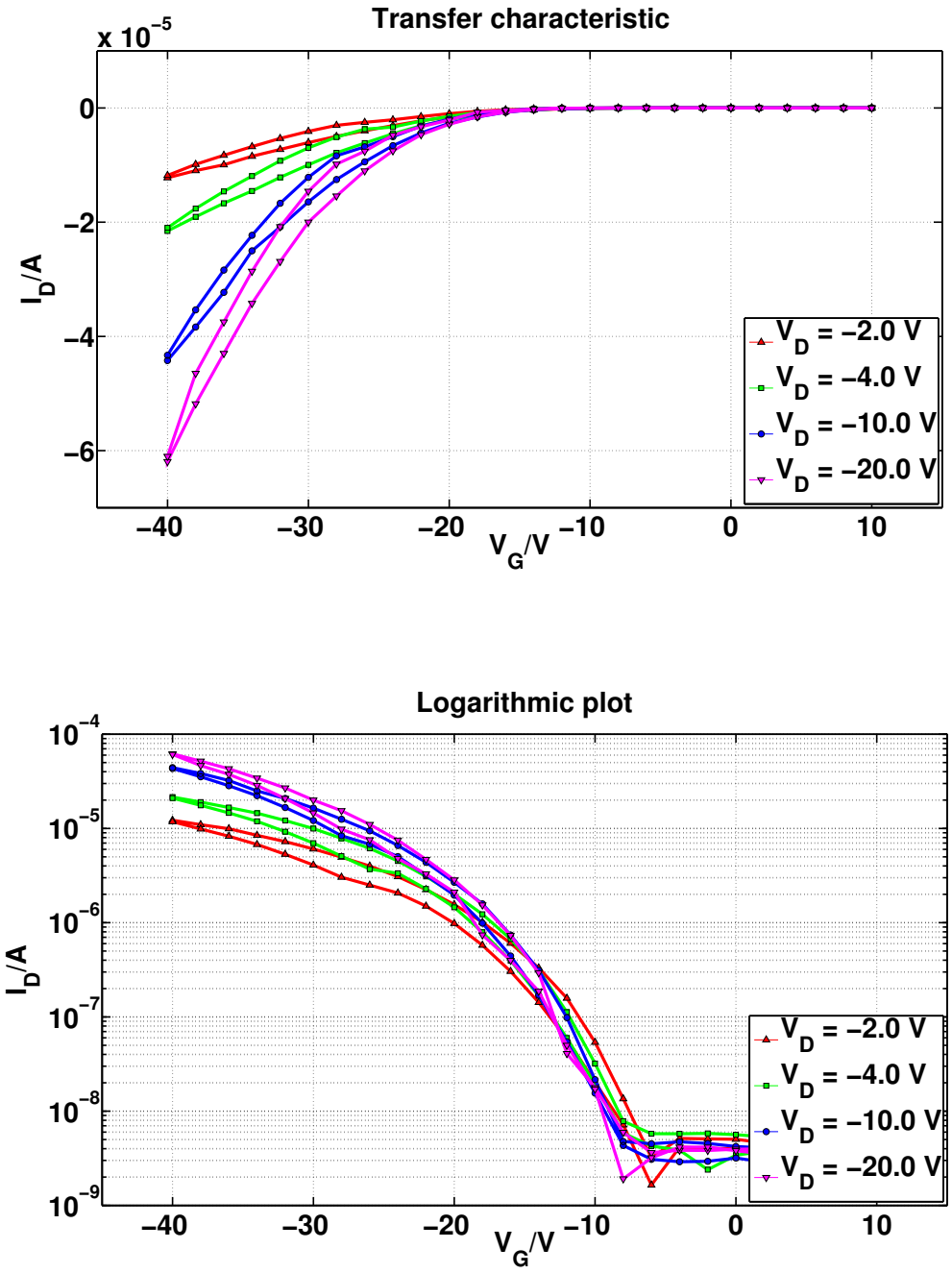


Figure 4.27.: Linear (top) and logarithmic (bottom) plots of the transfer characteristics of a thermally evaporated pentacene device for different drain voltages. The mobility fitted in the saturation regime is $\mu = 0.06$ cm^{2}V^{-1}s^{-1} (at V_D = -20 V)

Table 4.7 lists the device parameters for the shown transfer characteristics in figure 4.27. Figure 4.28 shows the corresponding output characteristics of the same device.

Table 4.7.: Device parameters of a top contact, thermally evaporated pentacene device. Note for the empty cells: The calculation of the parameters is not reasonable in this regime.

V_D [V]	μ_{lin} [$cm^2V^{-1}s^{-1}$]	μ_{sat} [$cm^2V^{-1}s^{-1}$]	$V_{TH,lin}$ [V]	$V_{TH,sat}$ [V]
-2	0.09		-19.2	
-4	0.09		-19.4	
-10	0.08	0.01	-19.6	-8.5
-20	0.06	0.06	-15.5	-15.3

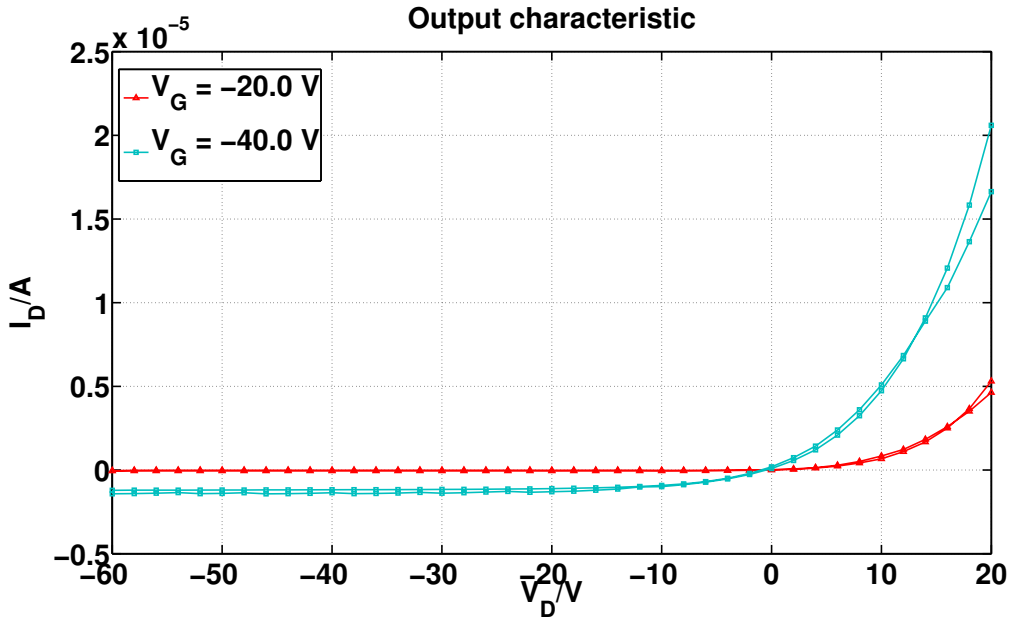


Figure 4.28.: Output characteristics of a thermally evaporated pentacene device (top contact geometry). The thickness of the pentacene layer is approximately 30 nm.

4.5.2. Conclusion

As expected, pentacene showed the best overall performance. The results are worse but in the same magnitude of order of those which were published ([31]). However, as mentioned before, taking the evaporation conditions into account (home made Knudsen cell, triggering of the evaporation rates via insulating transformer, chamber pressure, etc.) the results are more than satisfying.

Moreover, the pentacene was not purified before evaporation and no special pretreatment via interface modification was made.

Compared to evaporated TIPS pentacene devices, evaporated pentacene devices show higher current by even much lower drain voltages. Further, they show significant higher mobilities and on/off ratios.

5. Interface Modifications

The main reasons for performing interface modifications are to pave ways for improving and controlling device parameters.
One major point of interest is the shift of the threshold voltage. Via a certain doping process it was shown that the threshold voltage can be shifted to positive values in P3HT devices. [25],[53],[54] Moreover, it is also possible to shift the threshold voltage in pentacene devices.[55]

This section shows the behavior of TIPS pentacene OTFTs using different self assembled monolayers or other gate dielectric/semiconductor interface layers.
Based on the results for TIPS pentacene, a doping mechanism in pentacene OTFTs is proposed and effects of interfacial modifications on TIPS pentacene devices are explained.

Interfacial layers

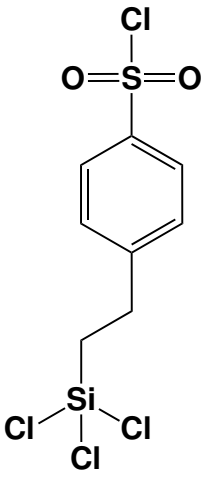
The following layers were used. Figure 5.1 shows their chemical structures.

- 2-(4-Chlorosulfonylphenyl)ethyltrichlorosilane
  (30 % 4-(2-(trichlorosilyl)ethyl)benzenesulfonic acid); 50% in toluene (ABCR; Product ID: AB129108; CAS Number: 79793-00-3)

- Poly(4-styrenesulfonic acid), Mw 75,000, 18 wt.% in H_2O (Sigma Aldrich; Product ID: 561223; CAS Number: 28210-41-5)

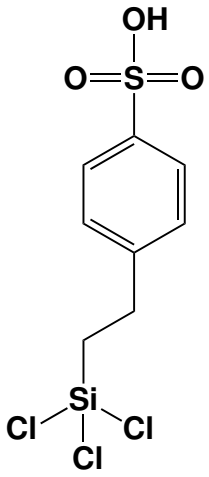
- Poly(acrylic acid) solution, Mw 100,000, 35 wt.% in H_2O (Sigma Aldrich; Product ID: 523925; CAS Number: 9003-01-4)

TSC



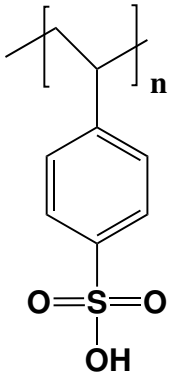
4-(2-(Trichlorosilyl)ethyl)benzene -1-sulfonyl chloride

TSA



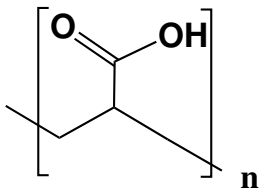
4-(2-(Trichlorosilyl)ethyl) benzenesulfonic acid

PSSA



Poly(4-styrenesulfonic acid)

PAA



Poly(acrylic acid)

Figure 5.1.: Chemical structure of 2-(4-Chlorosulfonylphenyl)ethyltrichlorosilane (TSC/TSA), Poly(4-styrenesulfonic acid) (PSSA) and Poly(acrylic acid) (PAA).

5.1. Threshold Voltage Shift in Pentacene Devices

Figure 5.2 shows the threshold voltage shift of a thermally evaporated pentacene device using a TSC/TSA SAM as interface modification (these curves were measured by S. J. Ausserlechner). Because of the interfacial layer the threshold voltage moved to $V_{\mathrm{TH}} = +70$ V. When one exposes the devices to ammoniac gas (NH_3), the transfer characteristics are shifted back to the state one observes in devices without interface modifications. These effects are explained in detail in section 5.3.

The formation of a space charge layer is held responsible for the threshold voltage shift.[25]

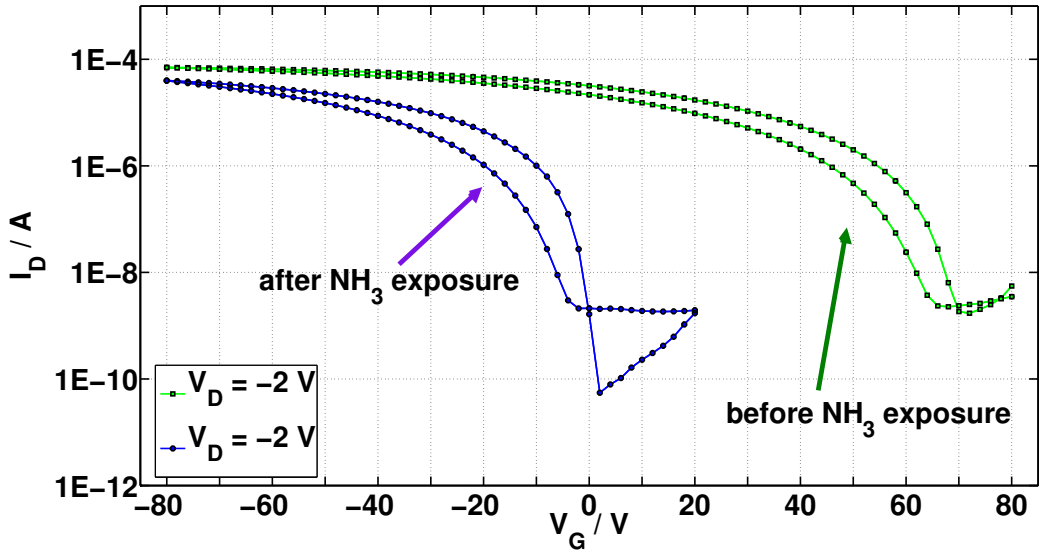


Figure 5.2.: Linear plots of the transfer characteristics of a thermally evaporated pentacene OTFT. The threshold voltage is shifted up to $V_{\mathrm{TH}} = +70$ V because of a TSC/TSA interfacial layer. After exposure to NH_3 gas, the curves are shifted back to the initial state $V_{\mathrm{TH}} = 0$ V . These curves were measured by S. J. Ausserlechner.

5.2. Behavior of the Threshold Voltage in TIPS Pentacene Devices

5.2.1. 2-(4-Chlorosulfonylphenyl)ethyltrichlorosilane (TSC/TSA)

First of all the TSC/TSA layer was deposited with the following procedure:

- Plasma etching for 30 seconds (maximum power level)
- CO_2 cleaning
- Ultra sonic bath for 2 min in deionized water (18 MΩ)
- CO_2 cleaning
- Preparation of solution made of 10 µl TSC/TSA in 10 ml toluene
- Wafer for 30 minutes in solution
- After 16 hours wafer treatment in solution, ultra sonic bath for 2 min in toluene
- Wafer cleaning with fresh toluene
- Annealing at 100 °C for 30 minutes under vacuum conditions (rotary vane pump, pressure p ≈ 1 mbar)
- Cooling step of the wafer for 90 minutes

In general, the procedure followed for the production of the devices described below was the following:

- Deposition of the TSC/TSA SAM as described above
- Evaporation of the 50 nm thick gold electrodes (channel length 25 µm, chamber pressure p ≈ $2 \cdot 10^{-6}$ mbar)
- Spin coating of TIPS pentacene from 1 wt.% solution in toluene at 60 °C substrate temperature
    - First 18 s at 2000 rpm

- Afterwards 20 s at 4000 rpm

Figure 5.3 shows the logarithmic plots of the transfer characteristics of a spin coated device including a TSC/TSA self assembled monolayer. **No shift of the threshold voltage** occurred. The reason for this behavior is explained in section 5.3.

Table 5.1 lists the device parameters for the corresponding device in figure 5.3.

Table 5.1.: Device parameters of a bottom contact, spin coated TIPS pentacene device including a TSC/TSA interfacial layer.

V_D [V]	μ_{lin} [$cm^2V^{-1}s^{-1}$]	μ_{sat} [$cm^2V^{-1}s^{-1}$]	$V_{TH,lin}$ [V]	$V_{TH,sat}$ [V]
-40	$3 \cdot 10^{-5}$	$1 \cdot 10^{-4}$	4.8	-9.0
-60	$3 \cdot 10^{-5}$	$1 \cdot 10^{-4}$	9.9	-10.6

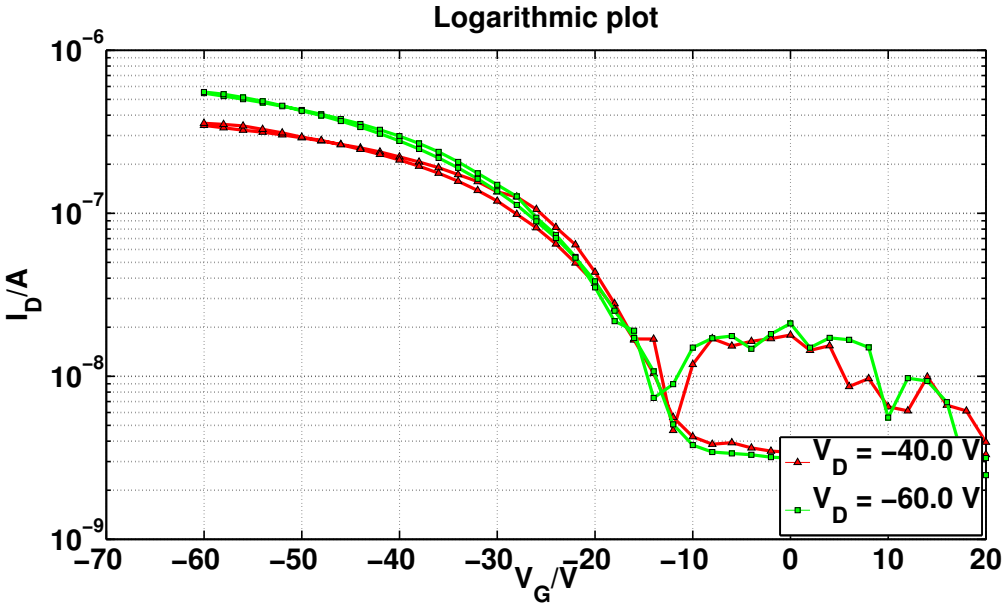


Figure 5.3.: Logarithmic plots of the transfer characteristics of a TIPS pentacene device (bottom contact geometry), spin coated from 1 wt.% solution in toluene for different drain voltages. Further a TSC/TSA SAM was included. The mobility is $\mu = 1 \cdot 10^{-4}$ $cm^2V^{-1}s^{-1}$, the threshold voltage is $V_{TH} \approx$ -11 V (both calculated in the saturation regime for V_D = -60 V).

5.2.2. Poly(4-styrenesulfonic acid) (PSSA)

The acidic part of the TSC/TSA layer is responsible for the threshold voltage shift (see section 5.3). Therefore, also acidic polymers were tested as interfacial layers.
The deposition of this kind of interfacial layers happens via spin coating and is much easier to accomplish.
The procedure for the devices was the following:

- Plasma etching for 30 seconds (maximum power level)
- Evaporation of the 50 nm thick gold electrodes (channel length 25 µm, chamber pressure p $\approx 2 \cdot 10^{-7}$ mbar)
- Spin coating of PSSA (200 µl, concentration 2.5 mg/ml); substrate kept at room temperature
  - First 9 s at 2000 rpm
  - Afterwards 40 s at 3500 rpm
- Spin coating of TIPS pentacene from 1.5 wt.% solution with 3,4-Dimethylanisole at 60 °C substrate temperature
  - First 18 s at 2000 rpm
  - After 20 s at 4000 rpm

Figure 5.4 shows the logarithmic plots of the transfer characteristics of a spin coated TIPS pentacene device including an interfacial layer out of PSSA. In this case 3,4-Dimethylanisole was used as solvent. Again no shift of the threshold voltage occurs. The same experiment was performed using toluene as solvent which led to an equivalent result.

A disadvantage in the present is that the hysteresis became much bigger which we attributed to residual water at the interface (18 wt.% PSSA is dissolved in H_2O).

Table 5.2 summarize the most important parameters for the plot shown in figure 5.4. The forward sweep was taken for parameter extraction.

Table 5.2.: Device parameters of a bottom contact, spin coated TIPS pentacene device including a spin coated PSSA interfacial layer. The forward sweep was taken for parameter extraction. Note for the empty cells: The calculation of the parameters is not reasonable in this regime.

V_{D} [V]	μ_{lin} [$\mathrm{cm^2V^{-1}s^{-1}}$]	μ_{sat} [$\mathrm{cm^2V^{-1}s^{-1}}$]	$V_{\mathrm{TH,lin}}$ [V]	$V_{\mathrm{TH,sat}}$ [V]
-10	$1 \cdot 10^{-3}$		4.8	
-20	$1 \cdot 10^{-3}$	$2 \cdot 10^{-3}$	5.4	2.3
-30	$1 \cdot 10^{-3}$	$2 \cdot 10^{-3}$	7.9	2.0

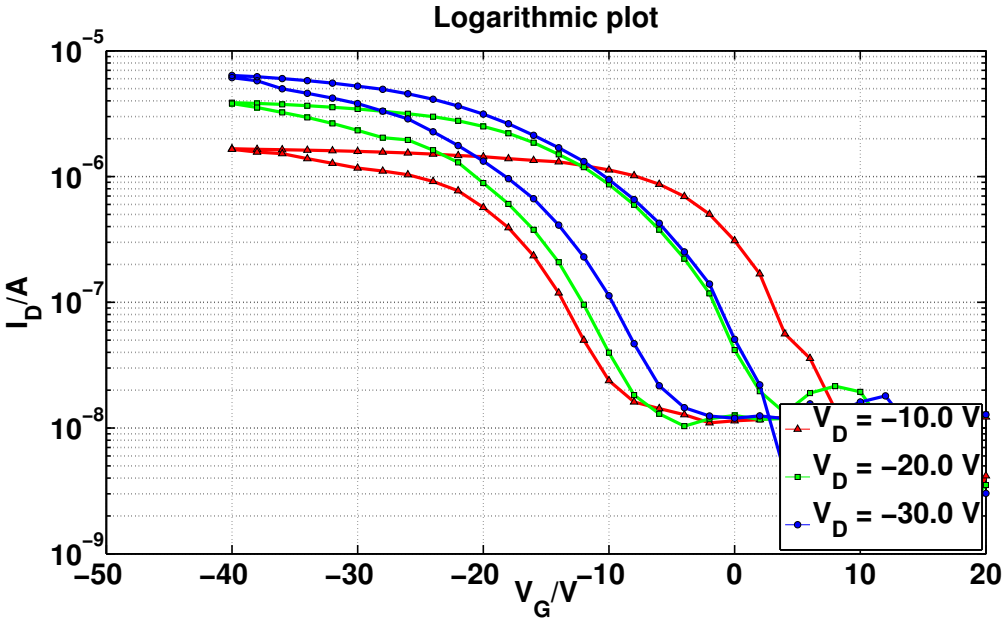


Figure 5.4.: Logarithmic plots of the drain current over the gate voltage of a TIPS pentacene device (bottom contact geometry), spin coated from 1.5 wt.% solution in 3,4-Dimethylanisole for different drain voltages. PSSA layer (concentration 2.5 mg/ml) was included. The mobility is $\mu = 2 \cdot 10^{-3}$ $\mathrm{cm^2V^{-1}s^{-1}}$, the threshold voltage is $V_{\mathrm{TH}} \approx 2$ V (both calculated in the saturation regime and for the forward sweep, at $V_{\mathrm{D}} = -30$ V).

5.2.3. Poly(acrylic acid) (PAA)

The same experiment was performed using another kind of acid. This led to the same result as seen before: No shift of the threshold voltage occurs.
The procedure for device fabrication was the following:

- Plasma etching for 30 seconds (maximum power level)
- Evaporation of the 50 nm thick gold electrodes (channel length 25 µm, chamber pressure p $\approx 2 \cdot 10^{-7}$ mbar)
- Spin coating of PAA at room temperature (200 µl, concentration 1 mg/ml)
  - First 9 s at 2000 rpm
  - Afterwards 40 s at 3500 rpm
- Spin coating of TIPS pentacene from 1 wt.% solution with toluene at 60 °C substrate temperature
  - First 18 s at 2000 rpm
  - Afterwards 20 s at 4000 rpm

Figure 5.5 shows the logarithmic plots of the transfer characteristics of a spin coated TIPS pentacene device including an interface layer out of PAA. Toluene was used as solvent. Again no threshold voltage shift occurred.

Table 5.3 lists the device relevant parameter of the transistor shown in figure 5.5. Again the forward sweep was taken for parameter extraction.

Table 5.3.: Device parameters of a bottom contact, spin coated TIPS pentacene device including a spin coated PAA interfacial layer. The forward sweep was taken for parameter extraction.

V_{D} [V]	μ_{lin} [$\mathrm{cm^2V^{-1}s^{-1}}$]	μ_{sat} [$\mathrm{cm^2V^{-1}s^{-1}}$]	$V_{\mathrm{TH,lin}}$ [V]	$V_{\mathrm{TH,sat}}$ [V]
-40	$1.5 \cdot 10^{-3}$	$3.6 \cdot 10^{-4}$	1.7	-9.8
-60	$1.5 \cdot 10^{-3}$	$4.4 \cdot 10^{-4}$	0.8	-17.9

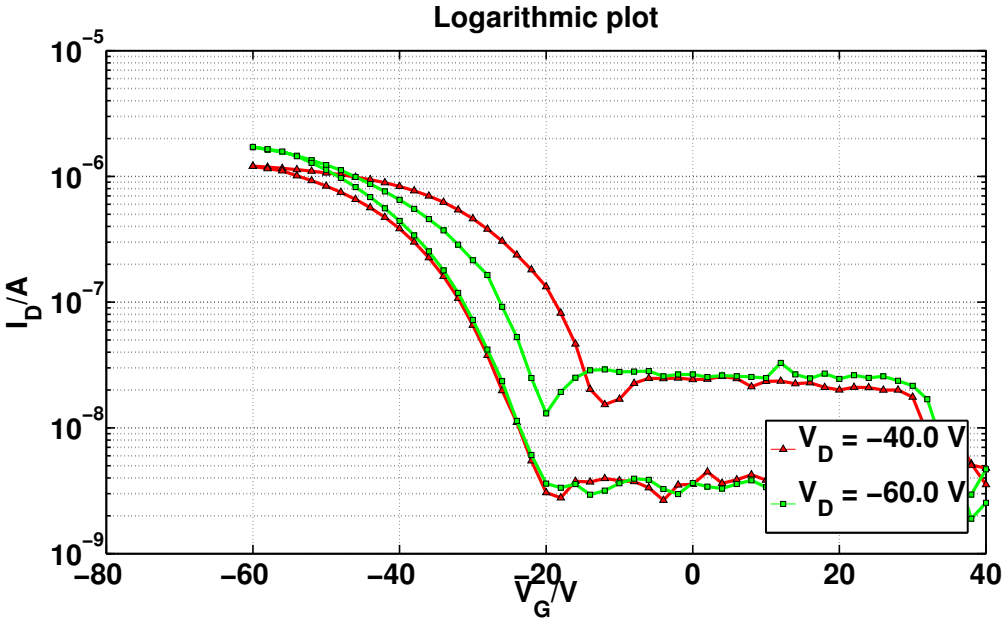


Figure 5.5.: Logarithmic plots of the transfer characteristics of a TIPS pentacene device (bottom contact geometry), spin coated from 1 wt.% solution with toluene for different drain voltages. The PAA concentration is 1 mg/ml. The mobility is $\mu = 4 \cdot 10^{-4}$ $\mathrm{cm^2V^{-1}s^{-1}}$ and the threshold voltage lays at $V_{\mathrm{TH}} \approx$ -18 V (both calculated in the saturation regime and for the forward sweep, at $V_{\mathrm{D}} =$ -60 V).

5.3. Doping Process & Conclusion

Figure 5.6 shows the proposed pentacene doping process at the interface (by S. J. Ausserlechner). Responsible for the shift is just the acid (TSA) of the TSC/TSA molecule blend.
Acids are proton donors where the H^+ leaves the acid and docks at the carbon atoms of the middle pentacene ring. One reason that the H^+ docks exactly at the carbon atoms of the middle pentacene ring is because of the proton affinity.[56] Further the behavior of the TIPS pentacene devices (no threshold voltage shift) leads to the same assumption (explanation see below).
Therefore, a proton surface transfer doping occurs. The left acidic residual forms the space charge layer at the interface. The combination of both effects, the space charge layer as well as the proton doping, shift the threshold voltage.

An acid-base reaction happens by exposure to NH_3 gas which dedopes the pentacene and further the space charge layer disappears. Therefore, the threshold voltage shift disappears and the device operates again in the "normal" state.

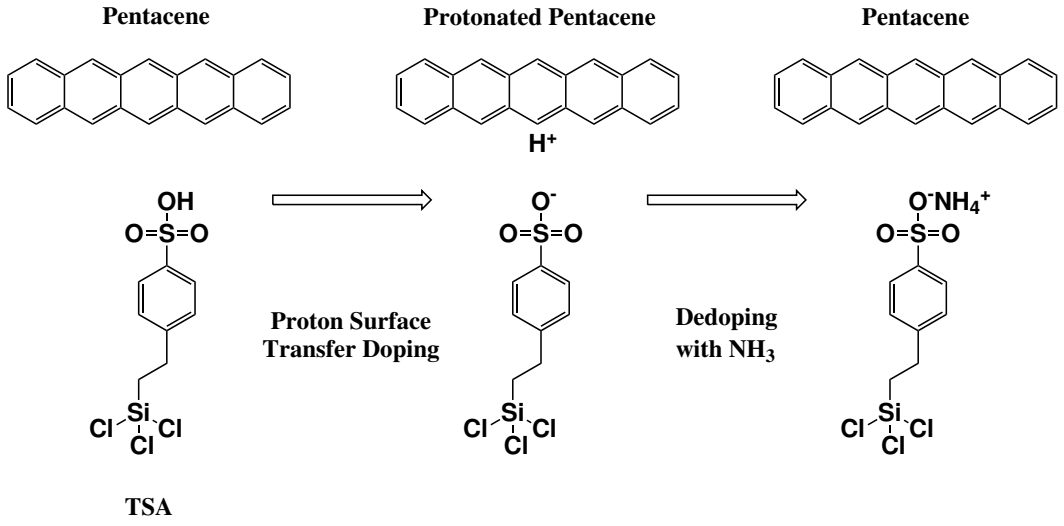


Figure 5.6.: Proton surface transfer doping effect by S. J. Ausserlechner. The H^+ docks at the central pentacene ring. A space charge layer is formed by the acidic residual. By exposure to NH_3 gas the whole system is shifted back to the initial state.

It is not possible to shift the threshold voltage of TIPS pentacene devices using the same doping mechanism as in pentacene. From the figures 5.3, 5.4 and 5.5 it is clear to see that no threshold shift occurs. The reason for this is that in case of TIPS pentacene the carbon atoms at the middle ring of pentacene are substituted by the side chains. This apparently prevents a docking of the H^+ protons from the acid to that position. No space charge layer and no proton doping process occurs.

From these results one can conclude that the H^+ dock to the carbon atoms of the **central** pentacene ring and not somewhere else. Otherwise a reaction between the TIPS pentacene and the acid would occur.

6. Additional Aspects regarding TIPS Pentacene Devices

6.1. Time Evolution

The device performance of TIPS pentacene OTFTs improves slightly with increasing time. E.g. by comparison of figure 4.8 and 4.9, which show transfer characteristics of drop cast devices measured at different times (1 wt.% TIPS pentacene in toluene), the improvement of the device performance is observable.

In addition, figure 6.1 demonstrates the time dependent improvement of the device performance for spin coated TIPS pentacene transistors (solution out of 1 wt.% TIPS pentacene in toluene). During the spin coating process the substrate temperature was 60 °C.

The device was measured after 15 hours, 24 hours and 72 hours, respectively. The mobility as well as the maximum current increased significantly. Moreover the hysteresis got slightly smaller. Table 6.1 summarizes the time dependent mobilities of the device.

Table 6.1.: Mobilities of a spin coated, bottom contact TIPS pentacene device determined in the linear and saturation regime. The device was measured after 15 hours, 24 hours and 72 hours. The drain voltage is V_D = -40 V.

Time elapsed after manufacturing	μ_{lin} [$cm^2V^{-1}s^{-1}$]	μ_{sat} [$cm^2V^{-1}s^{-1}$]
15 hours	$2.3 \cdot 10^{-5}$	$5.3 \cdot 10^{-5}$
24 hours	$1.0 \cdot 10^{-4}$	$2.3 \cdot 10^{-4}$
72 hours	$1.4 \cdot 10^{-4}$	$2.7 \cdot 10^{-4}$

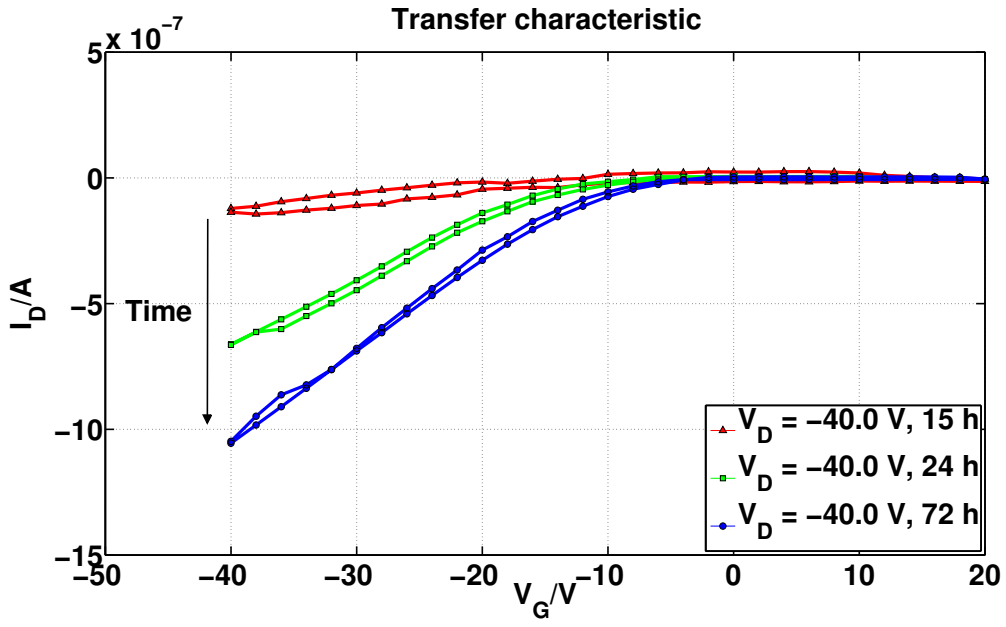


Figure 6.1.: Linear plots of the transfer characteristics of a TIPS pentacene device (bottom contact geometry), spin coated from 1 wt.% solution in toluene for a drain voltage of V_D = -40 V. The device was measured after 15 hours, 24 hours and 72 hours. The mobilities are $\mu = 5.3 \cdot 10^{-5}$ $cm^2V^{-1}s^{-1}$ after 15 hours, $\mu = 2.3 \cdot 10^{-4}$ $cm^2V^{-1}s^{-1}$ after 24 hours and $\mu = 2.7 \cdot 10^{-4}$ $cm^2V^{-1}s^{-1}$ after 72 hours, respectively. All values were calculated in the saturation regime.

6.1 Time Evolution

In general[1] the situation is the following:

- Devices using toluene as solvent start to operate approximately after 5 to 8 hours and reach their best performance within 3 days (example see figure 6.1)
- Devices using 3,4-Dimethylanisole as solvent start to operate after approximately 2 days and reach their best performance within 4 days
- Thermally evaporated devices operate right after fabrication

An obvious explanation would be that the solvent has to evaporate completely before the devices start to operate. This would explain the different time behavior between the two solvents because both have different vapor pressure.

Hence, time depended XRD measurements to explain these effects have been performed (see below).

[1] In case of solution processed OTFTs (drop cast or spin coting), the time scales are process dependent but within the listed values

6.1.1. Time Dependent XRD Measurements on Films Spin Coated from a Toluene Solution

Figure 6.2 shows a $\Theta/2\Theta$ scan of spin coated TIPS pentacene device using toluene as solvent. The substrate temperature during the spin coating process was 60 °C and the spin parameter was 2000 rpm for the first 18 seconds and 4000 rpm for the next 20 seconds respectively.

Observable from figure 6.2 is that the (00L) peaks do not change over time. The only difference occurs at the 2Θ peak at approximately 12.9°. Figure 6.3 shows a zoom into the region of that peak. One can observe that the full width at half maximum (FWHM) decreases slightly with increasing time. This peak refers to the (011) direction. So in fact a small change in the bulk happens.
Table 6.2 shows the time steps in which the XRD measurements have been performed.

Table 6.2.: Schedule of the XRD measurements on a spin coated substrate using toluene as solvent. The substrate temperature was 60 °C during the spin coating process.

Measurement #	**Time elapsed after manufacturing**
M1	1 hour
M2	6 hours
M3	11 hours
M4	25 hours
M5	32 hours
M6	48 hours

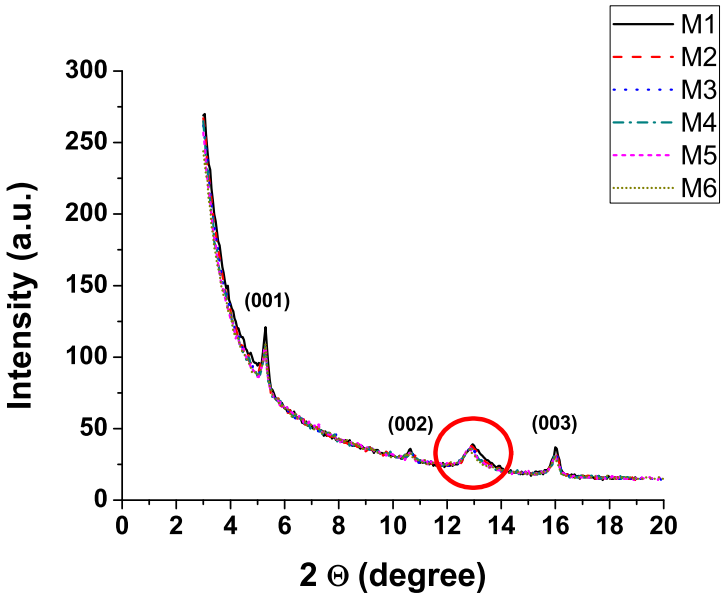


Figure 6.2.: Time dependent $\Theta/2\Theta$ scan of a spin coated substrate using toluene as solvent (substrate temperature 60 °C).

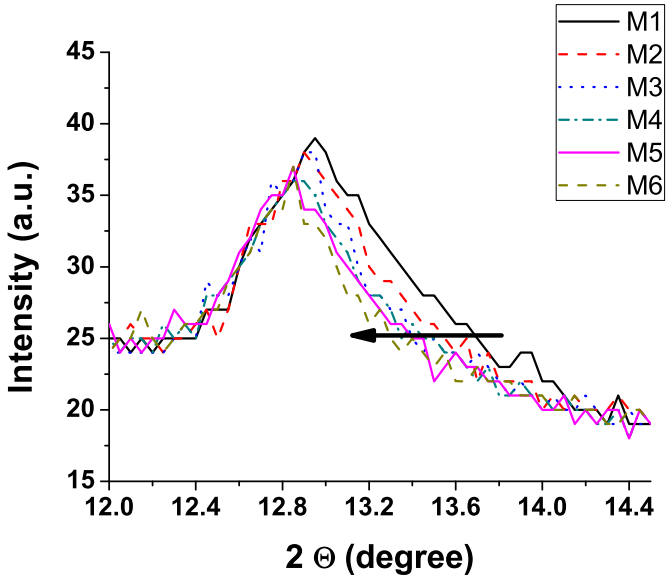


Figure 6.3.: Detailed view of the 12.9° (011) peak. With increasing time the FWHM decreases.

6.1.2. Time Dependent XRD Measurements on Films Spin Coated from a 3,4-Dimethylanisole Solution

Also for films spun from 3,4-Dimethylanisole time resolved XRD measurements have been perfomed.
Table 6.3 shows the time steps for which the XRD diffractograms have been measured and figure 6.4 presents the results.
The (00L) peaks stay constant over time which does not answer the question why devices start operating after a certain time. The (011) peak is hardly observed, which makes the analysis of its evolution impossible.

Table 6.3.: Schedule of the XRD measurements on a spin coated substrate using 3,4-Dimethylanisole as a solvent. The substrate temperature was 60 °C during the spin coating process.

Measurement #	**Time elapsed after manufacturing**
M1	right after process
M2	5.5 hours
M3	23 hours
M4	28 hours
M5	33 hours
M6	47 hours
M7	52 hours
M8	57.5 hours
M9	71 hours
M10	76 hours
M11	81 hours

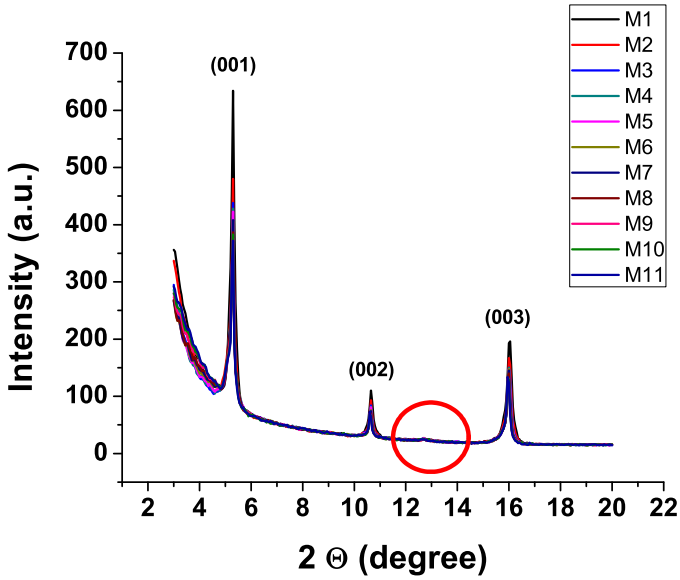


Figure 6.4.: Time dependent XRD measurement of a spin coated substrate using 3,4-Dimethylanisole as solvent (substrate temperature 60 °C during the spin coating process).

6.1.3. Conclusion

It is still unknown what is really happening in the first couple of hours. However, it is possible that all of the solvent has to evaporate before the devices can operate properly. This would match that spin coated 3,4-Dimethylanisole devices need, other than toluene devices, a longer time before they start to operate. This is supported by the result that thermally evaporated devices start to operate right after their production and the fact that drop cast devices need much longer to start to operate.
The XRD measurements however, did not yield to further insights.

Table 6.4 sums up the measured 2Θ (00L) peak positions of TIPS pentacene.

Table 6.4.: 2Θ peak positions of TIPS pentacene.

Orientation	2Θ **angle** [°]
(001)	5.3
(002)	10.6
(003)	15.9

6.2. Influence of Air and Light

One big advantage TIPS pentacene is known for is its great air stability.[23] This section will discuss the sensitivity of TIPS pentacene to air exposure and light illumination.

6.2.1. Results

We produced three groups of devices. All of them were built at the same time with the same treatment. The procedure for all devices was the following:

- Bottom contact geometry
- Spin coating at 60 °C substrate temperature
- 1 wt.% TIPS pentacene solution in toluene

One group of devices was stored in air and in a dark room so no light was illuminating the devices. The second group was kept in an argon glove box without light illumination as well. The third group was stored in air and was illuminated by light during the whole experimental procedure (fluorescent lamps of the laboratory lighting).
Figure 6.5 shows the logarithmic plots of the transfer characteristics for the different situations. The devices were measured after 8 days.
The mobilities for all three groups differ just slightly (see table 6.5) within the scattering of solution processed TIPS pentacene devices. The logarithmic plots shows that all devices have similar performance. Those devices which were kept in air have a slightly larger hysteresis than the devices in the glove box. This effect can be explained by oxygen doping effects and oxidation of molecules inside the film which leads to introduced traps or defects.[23]

Table 6.5.: Parameters of spin coated devices out of solution containing 1 wt.% TIPS pentacene in toluene. The drain voltage is V_D = -40 V.

Environment	μ_{lin} [$cm^2V^{-1}s^{-1}$]	μ_{sat} [$cm^2V^{-1}s^{-1}$]	$V_{TH,lin}$ [V]	$V_{TH,sat}$ [V]
Dark + Argon	$1.5 \cdot 10^{-4}$	$4.3 \cdot 10^{-4}$	3.7	-9.5
Dark + Air	$2.1 \cdot 10^{-4}$	$5.3 \cdot 10^{-4}$	3.5	-8.5
Light + Air	$2.0 \cdot 10^{-4}$	$4.5 \cdot 10^{-4}$	0.1	-11.2

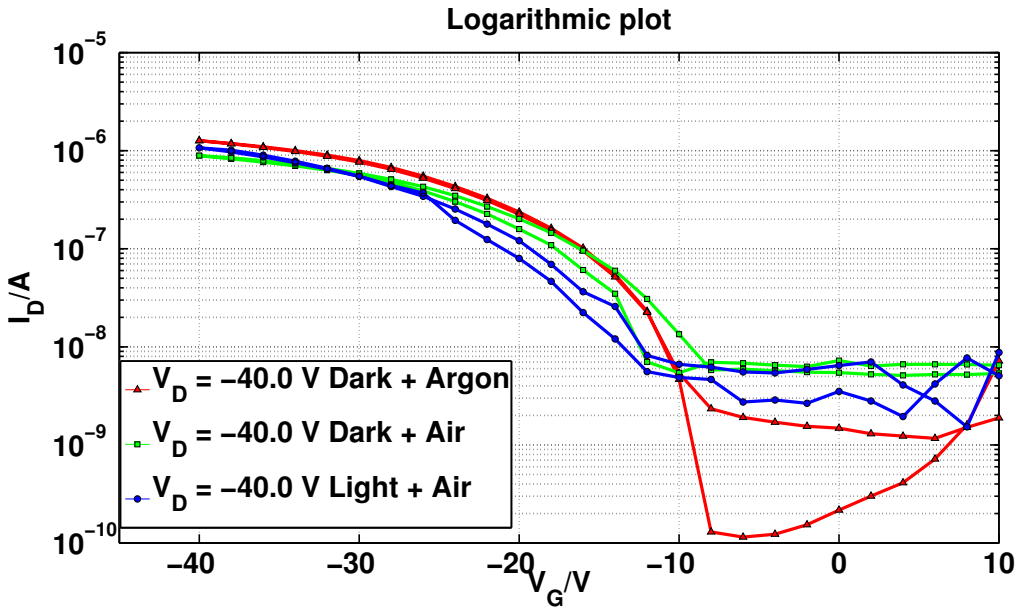


Figure 6.5.: Logarithmic plots of the transfer characteristics of spin coated devices out of solution containing 1 wt.% TIPS pentacene in toluene. The influence and impact of air and light exposure measured after 8 days is shown. All devices show more or less the same performance. The mobilities differ between $\mu = 4 \cdot 10^{-4}$ $cm^2V^{-1}s^{-1}$ in air and $\mu = 5 \cdot 10^{-4}$ $cm^2V^{-1}s^{-1}$ in argon glove box (extracted in the saturation regime for a drain voltage of V_D = -40 V).

6.3. Mobility Degradation in TIPS Pentacene Devices

Mobility as well as contact resistance play an important role in organic semiconductor devices.

Figure 6.6 shows the particular effect of the field induced mobility degradation. The devices in figure 6.6 were spin coated using a solution containing 1 wt.% TIPS pentacene in toluene. The substrate temperature was 60 °C during the spin coating process.

At the transition from the saturation regime into the linear regime ($|V_D| = |V_G - V_{TH}|$) the drain current starts to saturate instead of increasing linearly with the applied gate voltage. Hence the mobility decreases.

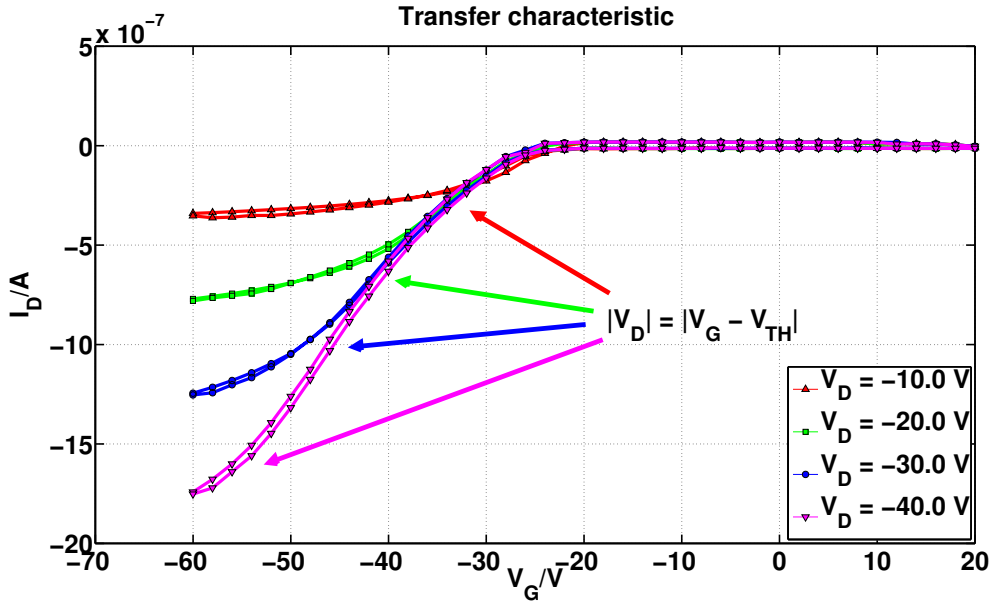


Figure 6.6.: Mobility degradation in a spin coated device containing 1 wt.% TIPS pentacene in toluene. The drain current starts to saturate at the transition from saturation into linear regime.

This effect has been explained by Horowitz and co-workers and is shown in figure 6.7.[57] In this figure the charge distribution is plotted over the number of layers in the semiconductor, beginning with 1 at the dielectric/semiconductor interface up to 20 in the bulk. This was done for different gate voltages (Top: $V_G = 1$ V; Middle: $V_G = 5$ V; Bottom: $V_G = 25$ V) and led to the following result:

For low gate voltages, more molecular layers are involved in the charge carrier transport process. By applying higher voltages, the charge carrier distribution concentrate in the

first few molecular layers. There the mobility is usually lower than in the bulk which leads to the saturation of the drain current and further to a mobility decrease.[57]

This effect can be reduced in TIPS pentacene devices by improving the production technique. In case of evaporated TIPS pentacene devices this effect influences the device performance to a much lower extent. We attribute this that the first layers show a better ordering and therefore, higher mobility (see figure 4.26). Moreover, the use of a different solvent reduces the effect as well (see figure 4.22).
However, the effect can be identified in each TIPS pentacene device.

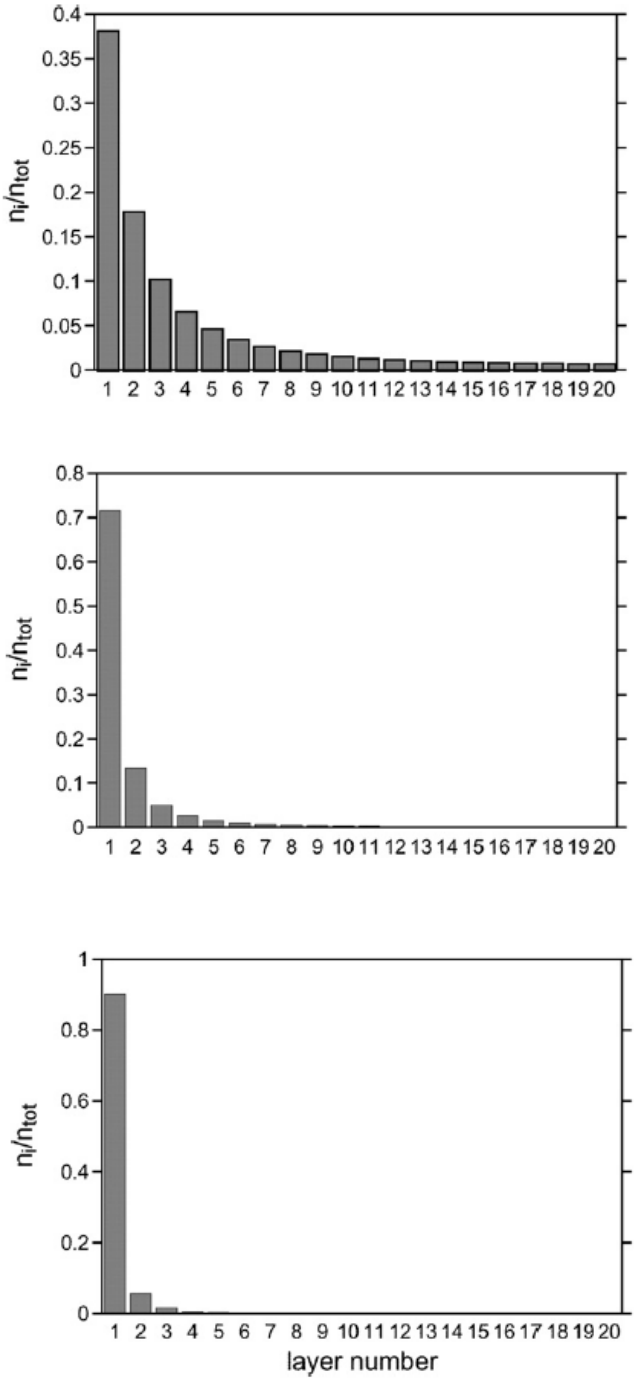


Figure 6.7.: Charge carrier distribution plotted over number of interfacial layers for different gate voltages (Top: $V_G = 1$ V; Middle: $V_G = 5$ V; Bottom: $V_G = 25$ V) to explain the effect of mobility degradation. Taken from [57].

6.3.1. Simulations

To see if mobility degradation is really the reason for the saturation behavior in our devices, simulations have been performed (by M. Gruber from the institute of theoretical and computational physics). Figure 6.8 shows transfer characteristics of simulated and measured[2] TIPS pentacene devices. The dotted lines are the experimental curves of a spin coated TIPS pentacene device using toluene as solvent (60 °C substrate temperature during the spin coating process). In the simulations, (solid lines in figure 6.8) the mobility in the preferable charge transport direction (parallel to the substrate) of the first four molecular layers was set to zero. This leads to the expected mobility degradation effect.

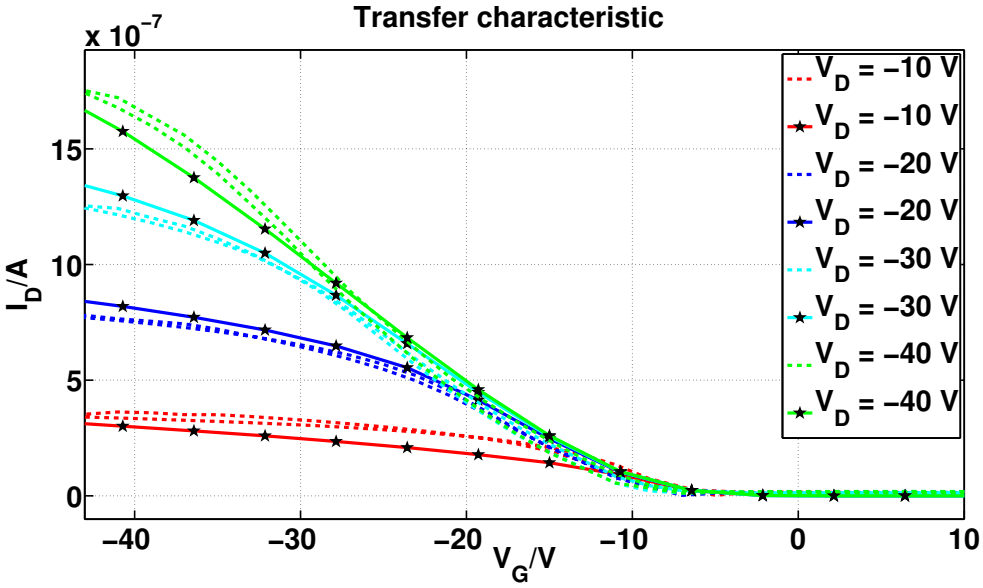


Figure 6.8.: Experimental (dotted lines) and simulated (solid lines) linear plots of the transfer characteristics to show the effect of mobility degradation in TIPS pentacene devices. Experimental: Spin coated, bottom contact device with 1 wt.% TIPS pentacene in toluene. Substrate temperature was 60 °C during the spin coating process. Simulation: Mobility of the first four molecular layers is set to zero in the direction parallel to the substrate. Courtesy of Manfred Gruber

[2]same device fabrication as in figure 6.6

7. Conclusion

This thesis supports the importance of TIPS pentacene as semiconductor material for OTFTs. Methods to deposit semiconductor layers out of solution on a substrate were demonstrated successfully. Especially spin coated devices illustrate great over all performance and show hardly any hysteresis. Further the device performance is completely reproducible, which is essential for performing sophisticated research.

The effects of substrate heating on spin coated TIPS pentacene devices and the consequences on the molecular ordering are discussed and explained.

Thermally evaporated TIPS pentacene devices exhibit the prospects this certain material has, especially by comparison to standard pentacene devices.

The reason that 3,4-Dimethylanisole show better performance is that the current limiting (011) orientation is not observed. Moreover, the crystallinity in case of 3,4-Dimethylanisole devices is higher, which can be seen in x-ray $\Theta/2\Theta$ scans.

It is also shown that, other than in pentacene and P3HT devices, it is not possible to shift the threshold voltage of TIPS pentacene devices with acids. The reason is that the side chains of the TIPS pentacene prohibit the proton surface doping of the central pentacene ring.

Light illumination as well as air exposure influence the device performance just slightly indicating high ambient stability of the devices.

A couple of phenomena are still unresolved, especially the question why devices start to operate only after a certain time.

Part III.

Appendix

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