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Voltage Probe Circuit Technology for Measurements in Power Electronics

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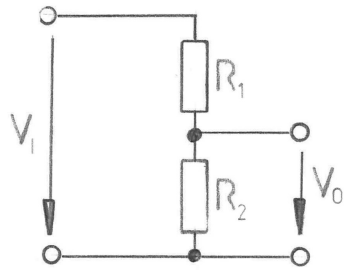
VOLTAGE PROBE CIRCUIT TECHNOLOGY FOR MEASUREMENTS IN POWER ELECTRONICS



GRUBMÜLLER, 2019

To little Paul,

You turned my life upside down - And I love it!

Abstract

Power electronics are the key to highly efficient power converter systems, like electric vehicles or photovoltaic systems. In these systems an inverter, the actual power electronics device, is used to transform a dc voltage into a variable-frequency, multi-phase ac voltage with fast-switching pulse-width modulation (PWM) techniques. Thus, voltage signals not only contain the fundamental wave, but also a high-frequency PWM carrier and intermodulation components. For development and optimization of power converter systems it is essential to measure these signals with wide bandwidth, high linearity and low noise. Since measurement instruments like oscilloscopes are low voltage devices, but inverter voltages are in the range of several hundred volts, a high voltage probe is needed to connect an instrument to the circuit under measurement. This thesis describes the development and characterization of different high voltage probe circuits for highly precise measurements in power electronics. It starts with an analysis of frequency-dependent behavior of passive components, based on literature and measurements. With the help of these findings, the design of a voltage divider with a flat frequency response and high linearity is presented. In a final step, this divider is implemented as an input stage for a high voltage differential probe and an isolated high voltage probe. Prototypes are built and characterized for both probes. In the last chapter, an appropriate measurement setup with low uncertainty to characterize the passband frequency response of a voltage probe is presented.

Kurzfassung

Leistungselektronik ist eine wesentliche Komponente in hocheffizienten Energiewandler Systemen, wie z. B, Elektrofahrzeuge oder Photovoltaikanlagen. In diesen Systemen wird ein Wechselrichter mit Leistungselektronikkomponenten verwendet, um eine Gleichspannung in eine mehrphasige Wechselspannung mit variabler Frequenz zu transformieren. Hierbei wird schnell schaltende Pulsweitenmodulation (PWM) eingesetzt. Die Spannungssignale enthalten somit nicht nur die Grundwelle, sondern auch einen hochfrequenten PWM-Träger und Intermodulationskomponenten. Für die Entwicklung und Optimierung von Leistungselektronik ist es somit unerlässlich, Spannungen mit hoher Bandbreite, hoher Linearität und geringem Rauschen zu messen. Da Messgeräte wie Oszilloskope Niederspannungsgeräte sind, die zu messenden Signale jedoch einige hundert Volt betragen, wird ein Tastkopf benötigt. Diese Arbeit beschreibt die Entwicklung und Charakterisierung verschiedener Hochspannungstastköpfe für hochpräzise Messungen in der Leistungselektronik. Zuerst wird das frequenzabhängige Verhalten passiver Komponenten analysiert. Mit Hilfe dieser Erkenntnisse wird ein Spannungsteiler mit flachem Frequenzgang und hoher Linearität entwickelt. In einem weiteren Schritt werden ein differentieller Hochspannungstaskopf und ein isolierter Tastkopf entwickelt, welche beide den Spannungsteiler als Eingangsstufe verwenden. Im letzten Kapitel wird ein geeigneter Messaufbau zur Charakterisierung des Frequenzganges von Spannungstastköpfen vorgestellt.

Affidavit

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly indicated all material which has been quoted either literally or by content from the sources used. The text document uploaded to TUGRAZonline is identical to the present doctoral thesis.

Date	Signature (Michael Grubmüller)

Contents

Glossary

Acronyms

ADC	Analog-to-digital converter
AWG	Arbitrary waveform generator
CMRR	Common-mode rejection ratio
CVD	Capacitive voltage divider
DFT	Discrete Fourier transform
DUT	Device under test
EDA	Electronic design automation
ESL	Equivalent series inductance
ESR	Equivalent series resistance
FEM	Finite element method
FET	Field-effect transistor
FPGA	Field-programmable gate array
FSR	Full-scale range
GBW	Gain-bandwidth product
GUM	Guide to the Expression of Uncertainty in Measurement
GUM-S2	GUM Supplement 2
IC	Integrated circuit
INA	Instrumentation amplifier
IVD	Inductive voltage divider
LTI	Linear time-invariant

MFB	Multiple-feedback
MV	Medium voltage
op-amp	Operational amplifier
PCB	Printed circuit board
PE	Protective earth
PGA	Programmable gain amplifier
PWM	Pulse-width modulation
RMS	Root mean square
R&D	Research and develpment
RVD	Resistive voltage divider
SAR	Successive approximation
SMD	Surface-mounted device
SNR	Signal-to-noise ratio
UART	Universal asynchronous receiver-transmitter
USB	Universal serial bus

Symbols

C	Capacitor (component), capacitance (value), (F)
$\boldsymbol{C}$	Matrix containing sensitivity coefficients
$\cos\theta$	Power factor, (-)
e_n	Voltage noise density, $(\mathrm{V}/\sqrt{\mathrm{Hz}})$
E_n	RMS voltage noise, (V)
ϵ	Permitivity, (F/m)
η	Efficiency coefficient, (-)
f	Frequency, (Hz)
G, $G(f)$	Frequency response magnitude, also referred as gain or attenuation, (-)
G_0	Gain/attenuation at dc, (-)
$\underline{G}$	Complex transfer function, (-)
H, $H(s)$	Transfer function of a filter in the Laplace domain, (-)
$h(X)$	Coefficient of contribution of $u(X)$ to the combined uncertainty, (-)
I	Constant dc current or RMS value of ac current, (A)
i, $i(t)$	Time domain current, (A)

j	Imaginary unit, (-)
L	Inductor (component), inductance (value), (H)
ω	Radian frequency, (rad^{-1})
P	Power, (W)
ϕ, $\phi(f)$	Frequency response angle (rad)
Q	Filter quality factor, (-)
R	Resistor (component), resistance (value), (Ω)
$\sigma(X)$	Standard deviation of X, ($[X]$)
t	Time, (s)
τ	Time constant, (s)
ϑ	Temperature, (K)
$u(X)$	Uncertainty of X, ($[X]$)
V	Constant dc voltage or RMS value of ac voltage, (V)
v, $v(t)$	Time domain voltage, (V)
$\boldsymbol{V}$	Covariance matrix
$w(t)$	Additive Gaussian noise, (V)
Z	Absolute value of the complex impedance $\underline{Z}$, (Ω)
$\underline{Z}$	Complex impedance, (Ω)
$:=$	Denotation

1
Introduction

To reduce greenhouse gas emissions and air pollution, new technologies are needed to replace fossil fuels in transportation and energy production. Power electronics will therefor play a dominant role in the 21st century, as they are the key to high efficient power converter systems [Bos13]. Two well-known examples for power electronic systems are electric cars or photovoltaic systems (Figure 1.1 and Figure 1.2).

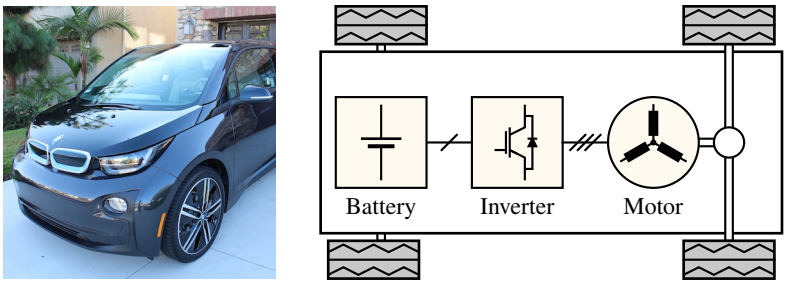


Figure 1.1: Electric car (left) and main components of the electric drivetrain (right). A battery provides the energy, further the inverter generates a 3-phase system to power the motor. [**GSW18**]

In an electric vehicle an inverter, the actual power electronic device, is used to transform a dc voltage (supplied by a battery or a fuel cell) into a 3-phase ac voltage of variable frequency to power a motor. In a photovoltaic system an inverter is used

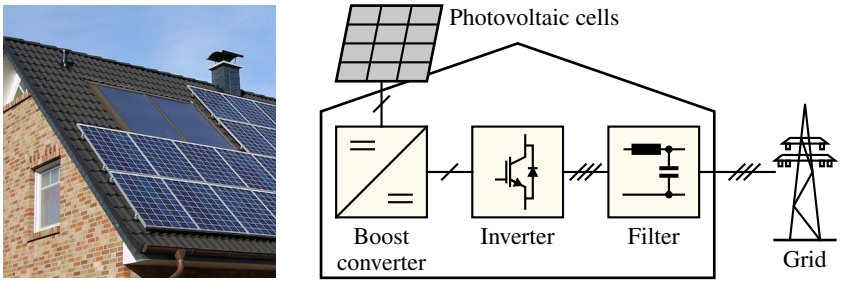


Figure 1.2: Photovoltaic cells on a roof (left) and main components of the photovoltaic system (right). First the small dc voltage of the photovoltaic cells is increased by a boost converter. Afterwords the inverter builds a three-phase ac voltage. The inverter output voltage gets filtered and may be consumed by in-house electric loads or is distributed to the grid. [**GSW18**]

to transform the dc voltage (delivered by the photovoltaic cells) into a constant-frequency 3-phase voltage to supply in-house loads or connect to the grid. For the development and optimization of power electronic systems, it is essential to precisely measure in- and output power of the inverter.

1.1 Problem Statement and Motivation

Figure 1.3 shows a simplified schematic of an inverter and the associated power flow. The input of the inverter is the dc system described by the battery voltage v_{dc} and the inverter input current i_{dc}. The output is a 3-phase ac system with the phase-to-phase voltages v_{12}, v_{23}, v_{31} and the phase currents i_1, i_2, i_3.

The following calculation demonstrates the importance of precise voltage and current measurements. As an example, an engineer must know the power dissipation P_{loss} of an inverter with a certain relative uncertainty in order to design the required cooling system. The calculation of the power dissipation P_{loss} is done by measuring the dc input power P_{dc} and the ac output power P_{ac},

$$P_{\mathrm{loss}} = P_{\mathrm{dc}} - P_{\mathrm{ac}}\,. \tag{1.1}$$

The uncertainty of the measurement can be calculated by the Guide to the Expression of Uncertainty in Measurement (GUM) *law of propagation of uncertainties* [JCG08]. The according uncertainty $u(P_{\mathrm{loss}})$ and the relative uncertainty $u(P_{\mathrm{loss}})/P_{\mathrm{loss}}$ of the

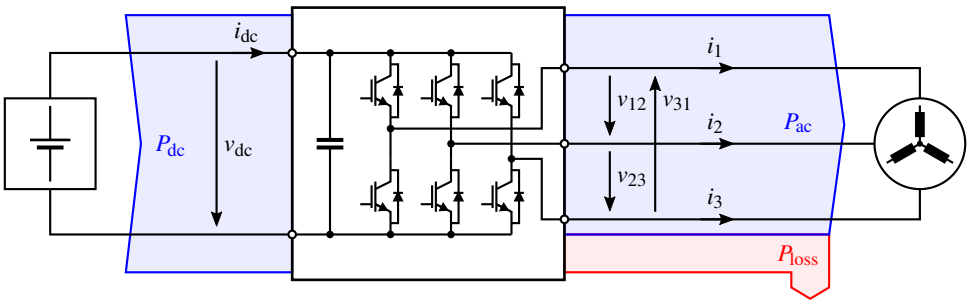


Figure 1.3: The inverter is a power electronics device which converts a dc input voltage into a 3-phase ac voltage. Due to power losses P_{loss}, mainly caused by the semiconductors, the output ac power P_{ac} is slightly smaller than the input dc power P_{dc}.

power loss estimation results to

$$u(P_{loss}) = \sqrt{\left(\frac{\partial P_{loss}}{\partial P_{dc}} u(P_{dc})\right)^2 + \left(\frac{\partial P_{loss}}{\partial P_{ac}} u(P_{ac})\right)^2} \tag{1.2}$$

$$= \sqrt{u(P_{dc})^2 + u(P_{ac})^2} \tag{1.3}$$

$$u(P_{loss}) \Rightarrow \frac{u(P_{loss})}{P_{loss}} = \sqrt{\left(\frac{u(P_{dc})}{P_{loss}}\right)^2 + \left(\frac{u(P_{ac})}{P_{loss}}\right)^2}, \tag{1.4}$$

where $u(P_{dc})$ and $u(P_{ac})$ are the uncertainties of the dc and ac power measurements P_{dc} and P_{ac}. By introducing the efficiency factor η

$$\eta = \frac{P_{ac}}{P_{dc}} = \frac{P_{ac}}{P_{ac} + P_{loss}} = \frac{P_{dc} - P_{loss}}{P_{dc}} \tag{1.5}$$

$$\Rightarrow P_{loss} = P_{ac} \frac{1-\eta}{\eta} = P_{dc}(1-\eta) \tag{1.6}$$

formulation (1.4) can be rewritten to

$$\frac{u(P_{loss})}{P_{loss}} = \sqrt{\left(\frac{u(P_{dc})}{P_{dc}} \frac{1}{1-\eta}\right)^2 + \left(\frac{u(P_{ac})}{P_{ac}} \frac{\eta}{1-\eta}\right)^2}. \tag{1.7}$$

The power measurement P_{dc} on the dc side is done indirectly by voltage and current measurements of V_{dc} and I_{dc}

$$P_{dc} = V_{dc} \cdot I_{dc}, \tag{1.8}$$

where the according uncertainty $u(P_{\mathrm{dc}})$ and the relative uncertainty $u(P_{\mathrm{dc}})/P_{\mathrm{dc}}$ is calculated by

$$u(P_{\mathrm{dc}}) = \sqrt{\left(\frac{\partial P_{\mathrm{dc}}}{\partial V_{\mathrm{dc}}} u(V_{\mathrm{dc}})\right)^2 + \left(\frac{\partial P_{\mathrm{dc}}}{\partial I_{\mathrm{dc}}} u(I_{\mathrm{dc}})\right)^2} \tag{1.9}$$

$$= \sqrt{(I_{\mathrm{dc}}\, u(V_{\mathrm{dc}}))^2 + (V_{\mathrm{dc}}\, u(I_{\mathrm{dc}}))^2} \tag{1.10}$$

$$\Rightarrow \frac{u(P_{\mathrm{dc}})}{P_{\mathrm{dc}}} = \sqrt{\left(\frac{I_{\mathrm{dc}}\, u(V_{\mathrm{dc}})}{P_{\mathrm{dc}}}\right)^2 + \left(\frac{V_{\mathrm{dc}}\, u(I_{\mathrm{dc}})}{P_{\mathrm{dc}}}\right)^2} = \sqrt{\left(\frac{u(V_{\mathrm{dc}})}{V_{\mathrm{dc}}}\right)^2 + \left(\frac{u(I_{\mathrm{dc}})}{I_{\mathrm{dc}}}\right)^2}. \tag{1.11}$$

Thus the relative uncertainty $u(P_{\mathrm{dc}})/P_{\mathrm{dc}}$ of the dc power measurement is the square sum of the relative uncertainties $u(V_{\mathrm{dc}})/V_{\mathrm{dc}}$ and $u(I_{\mathrm{dc}})/I_{\mathrm{dc}}$ of the dc voltage and current measurements. On the ac side an additional phase measurement is necessary to calculate the power factor $\cos\theta$. The output of the inverter is assumed balanced so that all phase-to-phase voltages V_{12}, V_{23} and V_{31} have the same root mean square (RMS) value, denoted (=:) by the ac voltage V_{ac}

$$V_{12} = V_{23} = V_{31} =: V_{\mathrm{ac}} \tag{1.12}$$

and all phase currents I_1, I_2 and I_3 have the same RMS value denoted by the ac current I_{ac}

$$I_1 = I_2 = I_3 =: I_{\mathrm{ac}}, \tag{1.13}$$

resulting to an ac power P_{ac} of

$$P_{\mathrm{ac}} = \sqrt{3} \cdot V_{\mathrm{ac}} \cdot I_{\mathrm{ac}} \cdot \cos\theta\,. \tag{1.14}$$

The according uncertainty $u(P_{\mathrm{ac}})$ is calculated by

$$u(P_{\mathrm{ac}}) = \sqrt{\left(\frac{\partial P_{\mathrm{ac}}}{\partial V_{\mathrm{ac}}} u(V_{\mathrm{ac}})\right)^2 + \left(\frac{\partial P_{\mathrm{ac}}}{\partial I_{\mathrm{ac}}} u(I_{\mathrm{ac}})\right)^2 + \left(\frac{\partial P_{\mathrm{ac}}}{\partial \cos\theta} u(\cos\theta)\right)^2} \tag{1.15}$$

$$= \sqrt{\left(\sqrt{3}\, I_{\mathrm{ac}} \cos\theta\, u(V_{\mathrm{ac}})\right)^2 + \left(\sqrt{3}\, V_{\mathrm{ac}} \cos\theta\, u(I_{\mathrm{ac}})\right)^2 \ldots}$$

$$\overline{+ \left(\sqrt{3}\, V_{\mathrm{ac}}\, I_{\mathrm{ac}}\, u(\cos\theta)\right)^2} \tag{1.16}$$

$$\Rightarrow \frac{u(P_{\mathrm{ac}})}{P_{\mathrm{ac}}} = \sqrt{\left(\frac{u(V_{\mathrm{ac}})}{V_{\mathrm{ac}}}\right)^2 + \left(\frac{u(I_{\mathrm{ac}})}{I_{\mathrm{ac}}}\right)^2 + \left(\frac{u(\cos\theta)}{\cos\theta}\right)^2}. \tag{1.17}$$

Further, the relative uncertainty of all voltage and current measurement instruments is assumed equal and are denoted by $u(X)/X$

$$\frac{u(V_{\mathrm{dc}})}{V_{\mathrm{dc}}} = \frac{u(V_{\mathrm{ac}})}{V_{\mathrm{ac}}} = \frac{u(I_{\mathrm{dc}})}{I_{\mathrm{dc}}} = \frac{u(I_{\mathrm{ac}})}{I_{\mathrm{ac}}} = \frac{u(\cos\theta)}{\cos\theta} =: \frac{u(X)}{X}. \tag{1.18}$$

By inserting (1.11) and (1.17) into (1.7) and using assumption (1.18) the resulting relative uncertainty $u(P_{\mathrm{loss}})/P_{\mathrm{loss}}$ of the power dissipation measurement can be written to

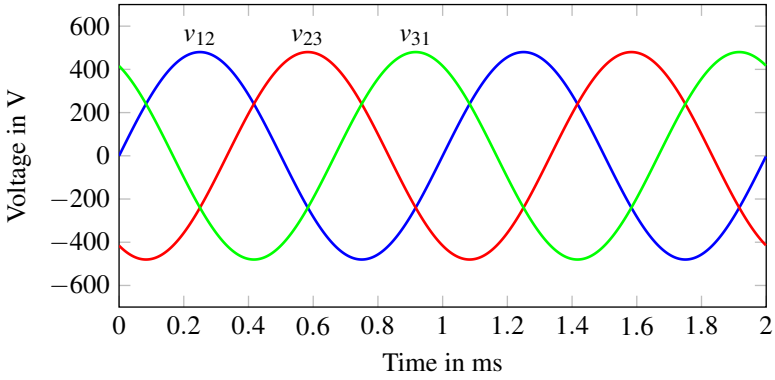
$$\frac{u(P_{\mathrm{loss}})}{P_{\mathrm{loss}}} = \frac{u(X)}{X} \cdot \frac{\sqrt{2+3\eta^2}}{1-\eta}. \tag{1.19}$$

Therefore, voltage, current and $\cos\theta$ measurements with a relative uncertainty of about 0.1 % are necessary to perform a power loss estimate P_{loss} with a relative uncertainty of 10 % on a modern automotive inverter with an efficiency of $\eta = 98\,\%$. The calculation example shows that high-precision voltage and current measurements are necessary to carry out power loss estimates with sufficient accuracy. In many cases, a current measurement can also be traced back to a voltage measurement. The focus of this work is on voltage measurement.

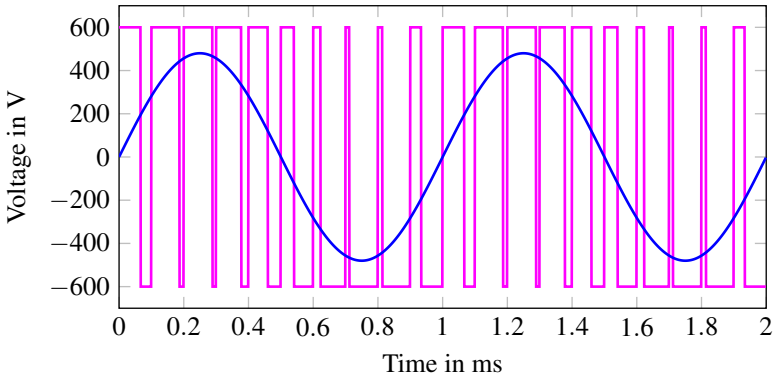
Since inverters use fast-switching pulse-width modulation (PWM) techniques to approximate a sinusoidal output, the output voltage signals v_{12}, v_{23} and v_{31} not only contain the fundamental wave but also a high-frequency PWM carrier and intermodulation components (Figure 1.4). Especially for power and efficiency measurements of inverters it is very important to have a high precision measurement over a wide bandwidth. Therefore, high voltage[1] measurements with high accuracy over wide bandwidth are required [DCJ97], [LB15], [MHM90].

[1] The International Electrotechnical Commission (IEC) defines *high voltage* by means of voltages greater than 1000 Vac or 1500 Vdc. However in the field of electric measurement and power electronics the term high voltage is used for voltages in the range of a few hundreds of volts.

(a) Fundamental waves of a 3-phase system



(b) Fundamental wave and PWM modulated signal



(c) Frequency domain of PWM voltage

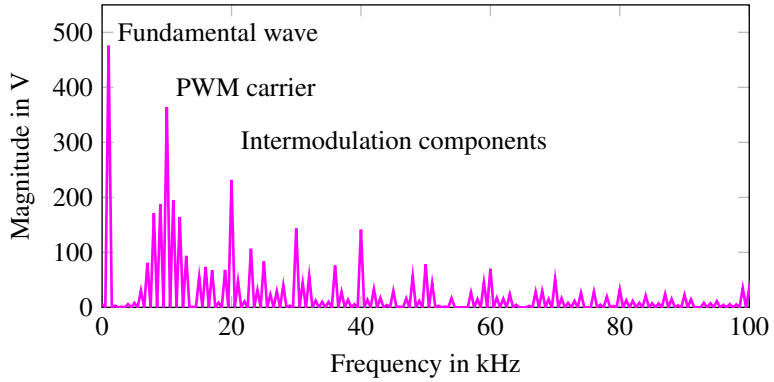


Figure 1.4: Time domain simulation of a 3-phase voltage system (a). The fundamental wave has a frequency of 1 kHz and is modulated with a PWM frequency of 10 kHz (b). The resulting frequency spectrum of the PWM modulated signal contains the fundamental wave, the PWM carrier and high-frequency intermodulation components.

1.2 State of the Art and Related Work

Since measurement channels of instruments like oscilloscopes and transient recorders are limited to a few volts, a probe is needed to measure high voltage signals. The probe is the physical and electrical connection between the circuit under test and the measuring instrument. Probes for the measurement of time varying high voltage signals can be divided into three groups:

- Single-ended probes
- Differential probes
- Isolated probes

Single-ended probes, like the well-known passive oscilloscope probe or a voltage divider as shown in Figure 1.5 are the simplest way to scale down a high voltage signal. However, the measurement is limited to ground related signals. Differential probes, like shown in Figure 1.6, overcome the limitation of single-ended probes by using two voltage dividers and a differential amplifier. Thus floating measurements, as required in power electronics, can be made. The third group are isolated probes as shown in Figure 1.7. An advantage of isolated probes is the galvanic isolation of the circuit under test from the measuring instrument. The following sections summarize the state of the art and related work regarding all three groups of voltage probes.

1.2.1 Single-ended Measurements

1.2.1.1 Passive Oscilloscope Probes

The common method for measuring time varying voltages is to use the proven passive probe like in Figure 1.8 connected to an oscilloscope. The limitation of using a passive probe in conjunction with an oscilloscope is, that only ground related measurements are possible. Since the inverter output voltages are floating, a differential measurement is necessary. It would be possible to use two passive probes, which perform two ground related measurements, and get the difference with a differential preamplifier like the *Tektronix ADA400A*. But this method would require that both probes are exactly equal. The differential voltage of both probes could also be calculated with an oscilloscope's math channel. But this would further require that

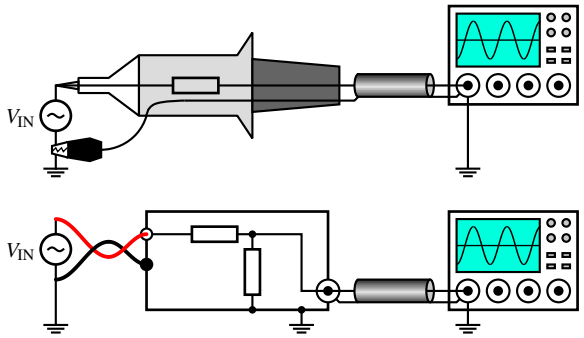


Figure 1.5: Passive oscilloscope probe (top) and voltage divider (bottom). The passive oscilloscope probe builds a voltage divider with the input impedance of the oscilloscope. Both, the passive oscilloscope probe as well as the voltage divider can only be used for single-ended measurements of the input voltage V_{IN}.

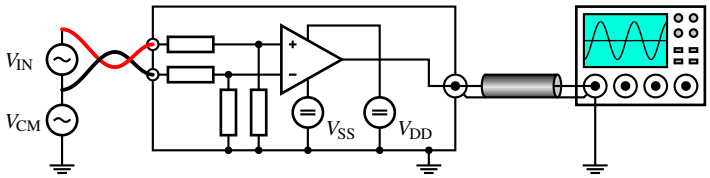


Figure 1.6: The high voltage differential probe consists of two matched voltage dividers connected to the system ground with a following differential amplifier. The high voltage differential probe is suitable for floating voltage measurements of the input voltage V_{IN} superimposed by the common-mode voltage V_{CM}.

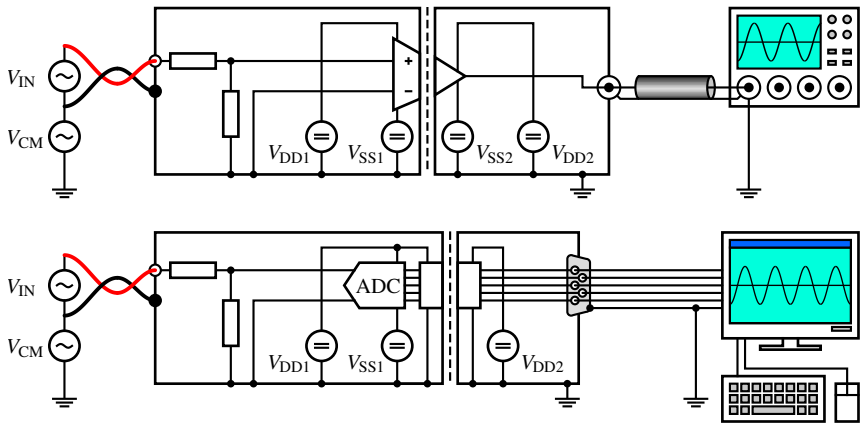


Figure 1.7: Analog isolated voltage probe (top) and digital isolated voltage probe (bottom). After scaling down the voltage by a voltage divider the signal is isolated by means of an isolation amplifier or already digitized in the probe and digitally isolated.

there is no channel mismatch between the oscilloscope input impedances [PC07]. Since no channel mismatch and equal probes are hardly feasible, passive oscilloscope probes should not be used for differential measurements in power electronics.

Figure 1.8: Standard passive oscilloscope probe for wide-band, single-ended voltage measurements (Photo: SparkFun, licensed under CC BY-SA 4.0).

1.2.1.2 Voltage Dividers

Although voltage dividers cannot be used directly for measurements in power electronics, as they cannot be used for floating measurements, they are the basic input stage of any high voltage probe concept. It is well known that inductive voltage dividers (IVDs) provide the lowest amplitude and phase errors for power line voltage measurements at 50 Hz with harmonics up to 1 kHz [HD68], [Sma+05], [Kyr+12]. However the performance of IVDs strongly decreases outside the audio and power line frequency range. Furthermore IVDs are a kind of special transformers, therefore they cannot be used for dc voltage measurements either [PTS14]. Capacitive voltage dividers (CVDs) can also be used to measure high ac voltages. CVDs for very high voltages and wide bandwidths can be achieved by using gas pressure capacitors [KZK00, Chapter 3.6]. However, like IVDs, CVDs cannot be used for dc voltage measurements. Therefore, only resistive voltage dividers (RVDs) are listed hereafter. Many metrological institutes and researchers are working on high accuracy RVDs that are designed for wide-band power measurements:

- *SP Swedish National Testing and Research Institute, Sweden:*
  Rydler, Svensson, and Tarasso built a set of resistive voltage dividers for a wide-band power measuring system for frequencies up to 20 kHz. The dividers cover voltages up to 1000 V. A verification measurement is shown at 50 Hz and 1.5 kHz, where the phase angle errors are within ±50 µrad. [RST02]

- *Physikalisch-Technische Bundesanstalt (PTB), Germany:*
  Mohns and Kürten Ihlenfeld present a precise active voltage divider, based on an inverting amplifier. The resistors for the divider are oil filled and hermetically sealed to limit the self-heating effect. The divider has 100 kΩ input resistance and is built for voltages up to 120 V. The small-signal bandwidth of the active divider is approximately 1 MHz. Combined with an oscilloscope the amplitude error is about 1 % at 100 kHz and full-scale input voltage. [MK04]

- *National Measurement Institute Australia (NMI), Australia:*
  Hagen and Budovsky developed a resistive voltage divider and a precision buffer amplifier for for low frequency metrology applications. The divider has an uncertainty of 100 ppm for amplitudes up to 240 V. To improve the stability, the used resistors are tested and handpicked for self heating. The divider is designed to work together with the precison buffer amplifier, also presented by the authors, to avoid any loading of the divider output. [BH10], [HB10]

- *Instituto Nacional de Metrologia, Qualidade e Tecnologia (INMETRO), Brazil:*
  Kyriazis et al. constructed a resistive voltage divider for the measurement of harmonics of power line frequencies. The ratio flatness of the divider is within 4 ppm up to 4 kHz. The ratio flatness is reached by using an shield around the divider that is driven by an auxiliary voltage divider. The ratio variation due to self heating at 240 V input voltage is about 5 ppm. The input resistance is given with 120 kΩ. [Kyr+12]

- *Istituto Nazionale di Ricerca Metrologica (INRiM), Italy:*
  Pogliano et al. built a set of resistive dividers for a three-phase power analyzer. The dividers consist of a serial-parallel structure with equal elements. Thus no compensation is necessary in theory. Practically some compensation is needed, due to the slightly different parasitic effects of the single components. The accuracy of the divider is better than 180 ppm for ratio and 20 µrad for phase up to 20 kHz. The maximum input voltage for the dividers is 600 V, the input resistance is 50 kΩ. (Figure 1.9) [PTS13], [PTS14], [Pog+14]

- *Van Swinden Lab. (VSL), Dutch National Metrology Institute, Netherlands:*
  Houtzager, Rietveld, and Brom present their work on a single-phase power meter for frequencies up to 1 MHz. The authors state that the limiting factor of the power measurement is the accuracy of their voltage divider, used to scale down the input voltage to the level of the digitizer. However, further details on the voltage dividers used are not contained in their papers. [Rie+11], [HRB13]

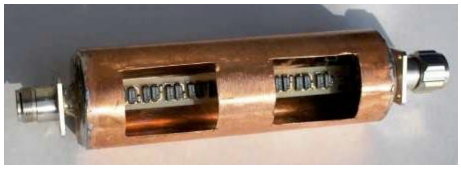


Figure 1.9: Voltage divider for a three-phase power analyzer at INRiM by Pogliano et al. [Pog+14], © 2014 IEEE.

- *Institute of Electrical Power Engineering, Lodz University of Technology, Poland:* Kaczmarek and Szatilo built a resistive voltage divider with capacitive compensation for determining voltage error and phase displacement of voltage transformers. The constructed divider shows 2 MΩ input resistance and was tested for input voltages up to 5 kV. The ratio error is smaller than 0.25 % at 2 kHz and increases to about 2.5 % at 20 kHz. [KS15]

- *Instituto Nacional de Metrologia, Qualidade e Tecnologia (INMETRO), Brazil, Instituto Nacional de Tecnología Industrial (INTI), Argentina, Administración Nacional de Usinas y Transmisiones Eléctricas (UTE), Uruguay:* Slomovitz et al. constructed three identical power measurement systems to be used in Brazil, Argentina and Uruguay. For the systems they also work on a voltage divider for input voltages up to 1024 V, covering frequencies from 50 Hz to 100 kHz. The input resistance of the divider is 256 kΩ. For compensation of parasitic effects, different shield geometries are tested. (Figure 1.10) [Slo+16a], [Slo+16b]

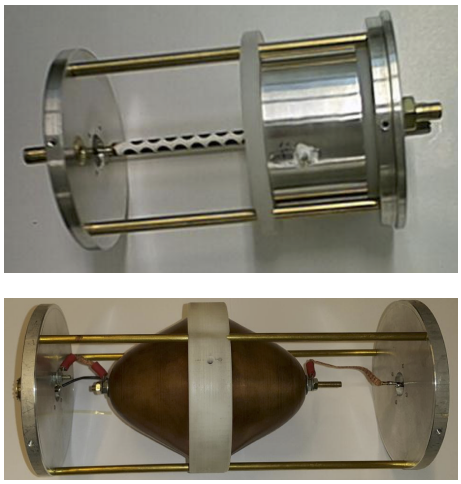


Figure 1.10: Voltage dividers with different shield designs by Slomovitz et al. [Slo+16b], licensed under CC BY 3.0.

- *University College of Southeast Norway (HSN),*
  Norwegian Metrology Service (JV), Norway:
  Karlsen et al. present their efforts on the development of a 1 : 400 voltage divider and a buffer amplifier for ac voltage metrology up to 1 MHz. The frequency response flatness is 30 ppm for the divider, and 200 ppm for the buffer up to 1 MHz. The values seem quite good, but the papers only present simulation results. No measurements on a prototype are shown so far. [Kar+16b], [Kar+16a]

- *National Institute of Metrology (NIM), China,*
  College of Instrumentation and Electrical Engineering, Jilin University, China:
  Shi et al. built different voltage dividers with serial-parallel connection of identical resistors. The divider with the highest input voltage of 300 V is a 257 : 1 voltage divider with 16 kΩ input resistance. Evaluation measurements of the divider show a phase angle error of 4.4 mrad at 100 kHz. (Figure 1.11) [Pan+16], [Shi+18b], [Shi+18a]

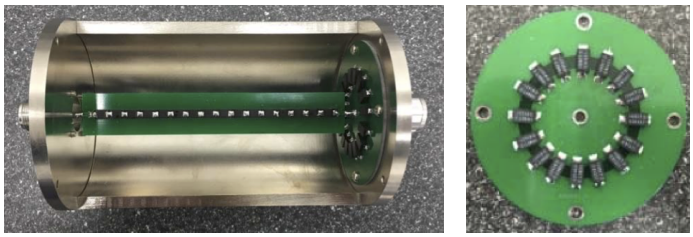


Figure 1.11: Serial (left) and parallel (right) connected identical resistors for voltage dividers at NIM China by Shi et al. [Shi+18a], © 2018 IEEE.

A summary on the listed voltage dividers is given in Table 1.1 (Section 3.4 on page 50). Although all listed dividers cannot be used directly for measurements in power electronics, their design ideas are of great help for the development of precise and wide-bandwidth high voltage probes.

1.2.2 Differential Measurements

1.2.2.1 High Voltage Differential Probes

A high voltage differential probe consists of two well matched input voltage dividers, followed by a differential amplifier. Thus the ground related output signal is the scaled down version of the input differential voltage. A detailed circuit of a precision

differential voltage probe is given by Ting et al. [Tin+86]. The bandwidth of their probe is better than 10 MHz and the precision is better than 0.5 %. However, the maximum input voltage of ±20 V makes the probe unsuitable for measurements of inverter input and output voltages. By contrast, Bossche and Bozalakov [BB13] explain their development of a high voltage differential probe for power electronic applications. Their probe is built for differential input voltages up to ±3 kV and can withstand voltages up to 8 kV. The probe has a bandwidth of 10 MHz and is able to follow slew rates up to 75 V/ns. Despite these promising specifications, the frequency response flatness is only in the range of 3 %.

Since high voltage differential probes are the state of the art probe for measuring floating high voltage signals, nearly every manufacturer of oscilloscopes and electrical measurement equipment offers a few different types. Some commercially available high voltage differential probes have been tested for passband frequency response flatness and linearity. Offset and gain errors have not been taken into account, as these errors can be easily corrected. For the testing, various probes from *Testec* [Sap13], [Sap09a], [Sap09b], [Sap09c] were considered (Figure 1.12). These probes are widely used. They are manufactured by *Sapphire Instruments* and sold by many different vendors. Because all the *Testec* probes are rather low-cost devices, a high-quality probe from *Tektronix* [Tek16] was also evaluated.

Figure 1.12: Examples for commercially available high voltage differential probes. From left to right: *Testec SI-9001* (low-cost probe, 25 MHz bandwidth, ±700 V), *Testec SI-9110* (high-bandwidth probe, 100 MHz bandwidth, ±1400 V differential input voltage) and *Testec SI-51* (high-accuracy and small-size probe, 50 MHz bandwidth, ±700 V differential input voltage, ±1 % accuracy).

The passband frequency response flatness of the evaluated probes is shown by plotting the normalized gain G/G_0 of the probe. The normalized gain is the gain G related

to the gain at dc or low frequency G_0. In contrast to the well-known Bode plot, the vertical axis is not represented in decibels, but in a linear scale, so that a percentage interpretation is easily possible (Figure 1.13). All probes show a flat normalized gain G/G_0 up to a few kilohertz, but already have an error of about 1 % at 50 kHz. Especially the *Testec* low-cost probes end up with a high error in the lower megahertz region.

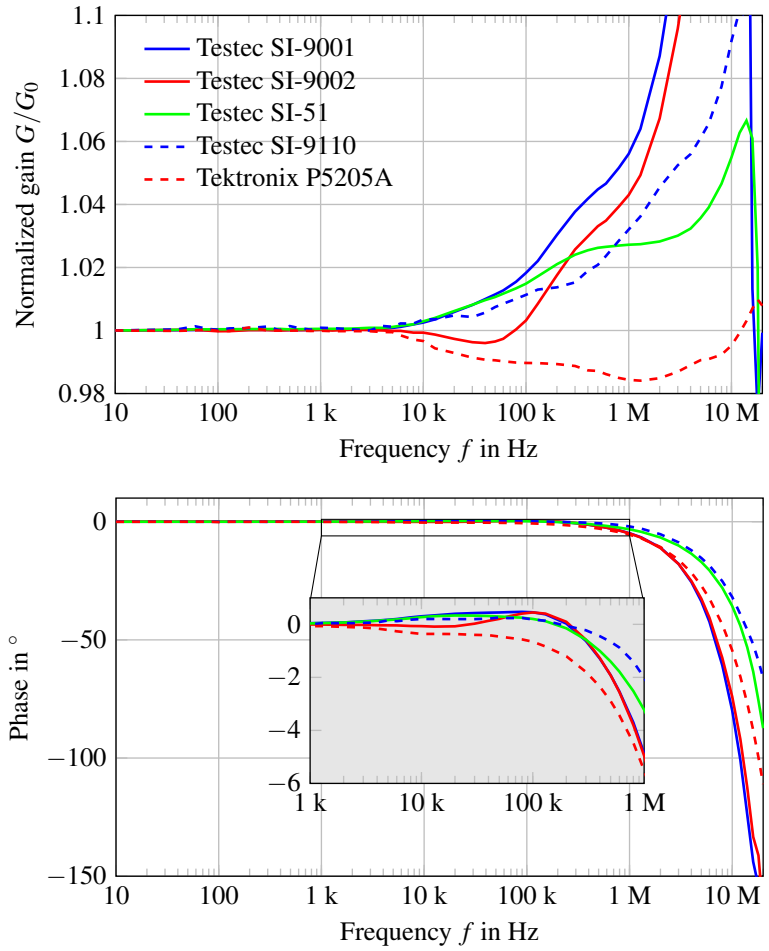


Figure 1.13: Comparison of the passband frequency response flatness and associated phase of commercially available high voltage differential probes. The plot shows the gain G of the probes related to their gain at dc or low frequency G_0. [**GSW17**]

The linearity of a probe is a measure of how much the attenuation of the probe changes with respect to the input voltage (Figure 1.14). The *Testec SI-51* high-accuracy probe shows the worst behavior regarding nonlinearity. The attenuation of the probe changes about 0.5 % over the whole input voltage range. The high-quality

probe *Tekronix P5205A* shows the best frequency response flatness, but also has a gain error of 1 % at 50 kHz and a nonlinearity of 0.3 % at 1 kV.

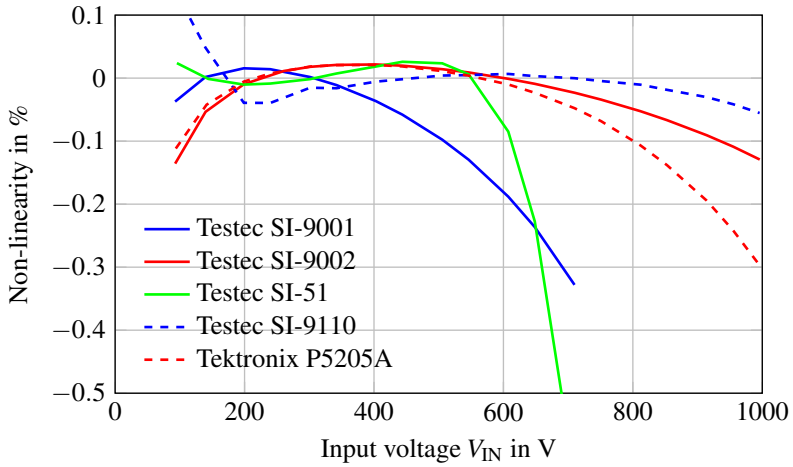


Figure 1.14: Comparison of non-linearity of different commercially available high voltage differential probes. [**GSW17**]

Because high voltage differential probes are simple to use and well known, but still too expensive for non-professionals, the *elektor* magazine published a do-it-yourself article on building a high voltage differential probe [Hes10]. In the article the author explains the development of a very simple and cheap probe for voltages up to 1 kV and a bandwidth of about 1 MHz.

1.2.3 Isolated Measurements

For certain applications the use of a high voltage differential probe is unsuitable. One example is the measurement of the gate-emitter voltage in power electronics. The relatively small gate-emitter voltages are superimposed by high voltage common-mode jumps. Thus, the used voltage probe requires a very high common-mode rejection ratio (CMRR). Conventional differential high voltage probes do not have enough performance for this purpose [Nar94]. A further example is the measurement of the inverter output voltages with the inverter already assembled in an electric vehicle, where the high voltage battery has an insulation monitoring device. Here isolated voltage probes are required, as the grounded measurement with a high voltage differential probe would cause an insulation fault. However, isolated oscilloscopes or battery powered oscilloscopes should not be used for floating measurements in power electronics [BB13]. The isolation barrier of isolated oscilloscopes is not designed

for continuous operation at several hundreds of volts. Battery powered oscilloscopes may introduce a large capacitance to ground, when allowing the oscilloscope to float. Further there may also arise some risk of high voltage hazards to the operating person.

1.2.3.1 Analog Isolated High Voltage Probes

An analog isolated high voltage probe uses a high voltage divider to scale down the input voltage, followed by an isolation amplifier. Isolation amplifiers are components that modulate the low-frequency input signal to a high-frequency signal, transmit it via a transformer based, optical or capacitive isolation barrier and then demodulate the signal again at the output (e.g. [CP81], [Sko82], [Mei90]). Since input and output are purely analog, the device looks like a purely analog device. Due to the modulation, however, a kind of sampling is used and the circuit developer must adhere to the sampling theorem. The disadvantage of isolation amplifiers is that their frequency range is very limited (Figure 1.15).

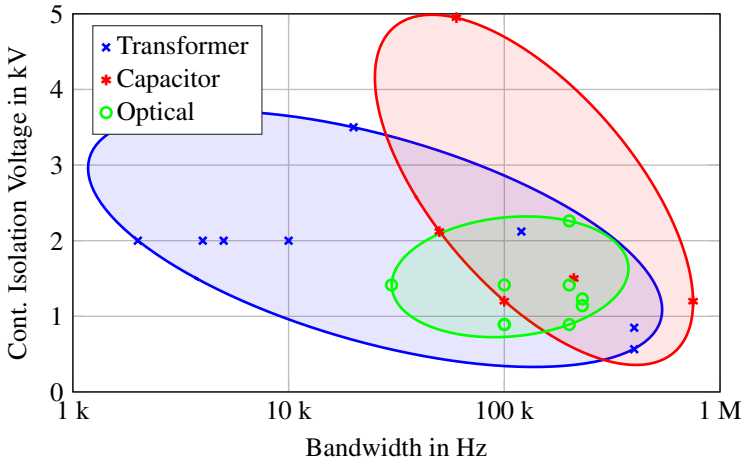


Figure 1.15: Market research on isolation amplifiers. The plot shows the continuous isolation voltage in dependency of the amplifier bandwidth, grouped by their used isolation barrier. (Amplifiers from *Analog Devices*, *Texas Instruments*, *Avago*, *Silicon Labs* and *Toshiba* are considered, May 2016)

For very high isolation voltages, the isolation amplifier can be replaced by an analog fiber optic transmission system [Nar94], [Cro+14]. The drawback of an analog fiber optic transmission systems is the limited linearity and a strong aging effect. Recently, *Tektronix* [Tek18] and *Teledyne Lecroy* [Tel17] introduced probes with

analog fiber optic transmission. Both offer very high isolation voltages in the range of several kilovolts and high CMRR. Because the probes are designed for the use with oscilloscopes, the accuracy, however, is worse than 1 % and the output noise is quite high.

1.2.3.2 Digital Isolated High Voltage Probes

A further way of isolating the probe from the measurement circuit is to include the analog-to-digital conversion in the probe and to isolate the digital data stream. The isolation can be realized by a digital isolation integrated circuit (IC), a digital fiber optic transmission or a wireless interface.

An interesting device was developed by Lobsiger et al. [Lob+11], [Lob+14]. The authors present a wireless single-channel oscilloscope without a screen, where the isolated digital transmission is done via Bluetooth to a computer (Figure 1.16). With the wireless transmission approach, the cabling can be reduced. A reduced cabling may be beneficial, especially when there are more measurement points at the same time, e.g. measuring all three inverter output voltages and the dc input. The wireless oscilloscope is designed for fast, wide-bandwidth short-term measurements, like the measurement of the gate-emitter voltage of power converters. The analog bandwidth of the wireless oscilloscope is 100 MHz. It utilizes an 8 bit analog-to-digital converter (ADC) with 400 MS/s sampling rate. Since the Bluetooth data transfer is too slow for continuous transmission of high-sampling-rate data, only short time slots are measured and stored in a memory before they get transmitted.

Figure 1.16: Wireless Bluetooth oscilloscope by Lobsiger et al. [Lob+14], © 2014 IEEE.

A similar product was launched by *Ikalogic* [IKA18]. The *Ikalogic IkaScope WS200* wireless oscilloscope probe uses Wifi for connecting the probe to a PC or a tablet.

The wireless probe achieves an analog bandwidth of 30 MHz and a sampling rate of 200 MS/s with 8 bit resolution data. The data is written to a 4 kS memory for block data transfer. The differential input voltage of the wireless probe is limited to ±40 V. Due to the small input differential voltage, also this wireless probe may only be used for gate-emitter voltage measurements but not for inverter output voltages.

1.2.4 Summary

Table 1.1 summarizes the state of the art and related work. It shows that voltage dividers are mainly built for high precision measurements in the higher kilohertz region. Therefore, the authors of papers on voltage dividers state a value for the frequency response flatness (or sometimes ac-dc difference) at a certain frequency, but mostly do not give the −3 dB bandwidth. Differential probes, on the other hand, are made for measurements with a large bandwidth. Thus the bandwidth of high voltage differential probes is always given in the regarding paper or datasheet. Since high voltage differential probes are commonly used with standard 8 to 12 bit oscilloscopes, they are not designed for good passband frequency response flatness. Most isolated probes are mainly built for gate-emitter voltage measurements in power electronics. Thus isolated probes therefore only allow relatively small input differential voltages, which are superimposed by high common mode voltages.

Table 1.1: Summary of the state of the art and related work

	Input voltage Diff. [a] (CM [b])	Input impedance [c]	-3 dB Bandwidth	Frequency response flatness	Comments
			Voltage dividers		
[RST02]	1 kV	-	20 kHz	-	
[MK04]	120 V	100 kΩ	1 MHz	1 % @ 100 kHz	Oil filled and hermetically sealed resistors
[HB10] [BH10]	240 V	-	-	100 ppm @ 100 kHz	Limited to power line applications
[Kyr+12]	240 V	60 kΩ || 1 nF	-	4 ppm @ 4 kHz	Limited to power line applications
[PTS13] [Pog+14] [PTS14]	600 V	50 kΩ || 200 pF	-	180 ppm @ 20 kHz	Divider for a three-phase power meter
[HRB13] [Rie+11]	-	-	-	5 ppm @ 100 kHz	Design of a switching sampling power meter up to 1 MHz
[KS15]	5 kV	2 MΩ	-	0.25 % @ 2 kHz	
[Slo+16a] [Slo+16b]	1 kV	256 kΩ	-	23 ppm @ 100 kHz	Sophisticated geometries for the dividers
[Kar+16b] [Kar+16a]	-	-	-	230 ppm @ 1 MHz	Only simulation results
[Pan+16] [Shi+18b] [Shi+18a]	300 V	16 kΩ	-	-	Divider with serial-parallel connection

Continues on next page ...

Table 1.1: Summary of the state of the art and related work

	Input voltage Diff. [a] (CM [b])	Input impedance [c]	-3 dB Bandwidth	Frequency response flatness	Comments
Differential probes					
[Tin+86]	20 V (-)	1 MΩ||6 pF	10 MHz	-	Designed for gate-emitter voltage measurement
[BB13]	3 kV (6 kV)	50 MΩ||2 pF	10 MHz	3 % @ 1 MHz	Capacitors in divider are implemented as PCB capacitors
[Sap09a]	700 V (700 V)	4 MΩ||5.5 pF	25 MHz		
[Sap09b]	1.4 kV (1.4 kV)	4 MΩ||5.5 pF	25 MHz		
[Sap09c]	1.4 kV (1.4 kV)	4 MΩ||7 pF	100 MHz	2 % @ 100 kHz	Different commercially available types
[Sap13]	700 V (1.4 kV)	4 MΩ||7 pF	50 MHz		
[Tek16]	1.3 kV (1.3 kV)	5 MΩ||4 pF	100 MHz		
[Hes10]	1 kV (-)	10 MΩ	1 MHz	-	Simple and cheap circuit for non-professionals
Analog isolated probes					
[Nar94]	- (> 200 V)	-	100 MHz	-	Designed for gate-emitter voltage measurement
[Tel17]	40 V (35 kV)	10 MΩ || 22 pF	60 MHz	-	Battery-powered to isolate supply
[Tek18]	2.5 kV (60 kV)	40 MΩ || 3.5 pF	800 MHz	-	Powered over optical fiber
Digital isolated probes					
[Lob+11] [Lob+14]	- (> 1 MV)	-	100 MHz	-	Needs a passive oscilloscope probe at the input
[IKA18]	40 V (-)	1 MΩ || 14 pF	30 MHz	-	Low voltage device

[a] Maximum working input differential voltage, ± (dc + ac peak)

[b] Maximum working input common-mode voltage range for differential probes, isolation voltage for isolated probes, ± (dc + ac peak)

[c] Impedance of each input against ground for dividers and differential probes, impedance between inputs for isolated probes

1.3 Contribution

1.3.1 Scientific Contribution and Structure of the Thesis

There are many high voltage differential probes and some isolated high voltage probes commercially available or presented in scientific papers. As described in Section 1.2 (State of the Art and Related Work) the performance of the probes, however, do not target high-precision measurements in modern power electronics. The probes are designed to reach a high bandwidth at high input differential voltages but good passband frequency response flatness and high linearity are not taken into consideration, as shown in Subsection 1.2.2 (Differential Measurements) and 1.2.3 (Isolated Measurements).

The main contribution of this thesis is the development and characterization of high voltage probe circuits for high-precision measurements in power electronics. As shown in Figure 1.5 through 1.7 in Section 1.2 (State of the Art and Related Work), a voltage divider is the basic input stage of any high voltage probe concept. Now the question arises whether it is possible to develop a voltage divider with high input impedance, wide bandwidth, high frequency response flatness, low phase lag and high linearity to finally build a probe with better performance than the commonly used probes. In any case, it is essential to understand and quantify the parasitic behavior of the electronic components used and the circuit itself. Every component as well as every circuit trace has parasitic effects that can be modeled by equivalent lumped circuit models out of resistors, capacitors and inductors. Resistors are used to model dc losses, capacitors and inductors are used to model imperfect ac behavior. Parameters of the lumped circuit models of components may not always have a real physical basis, but model their behavior. Only a few parameters of the component model can be found in data sheets and literature. Therefore, most of the model parameters for this work are obtained from measurements and finite element method (FEM) simulations. In order to keep the complexity of the model as low as possible, simple approximations with sufficient accuracy for the model parameters are sought. For this purpose, analytical calculations with simplified geometry are compared to complex FEM simulations. With the help of the final simulation framework, methods can be found to compensate for parasitic effects. These methods contain geometric specifications for achieving defined stray capacitances and further circuits for compensating the frequency-dependent behavior of the components. The effectiveness of the methods can be confirmed by a simulation as shown by the end of Chapter 2 (Frequency Compensated Voltage Divider) and in [**GSW14**].

Since the result of this thesis should be a complete probe circuit and not just a single divider, two identical dividers and a differential amplifier are combined to build a high voltage differential probe. Measurements on a probe prototype confirm the initial design goals of high bandwidth, frequency response flatness, low phase lag and high linearity. Results are shown in the final section of Chapter 3 (High Voltage Differential Probe) and in [**GSW17**].

After all the work on the high voltage differential probe circuit, it might be of interest whether the input impedance of the dividers can be increased to a value so that the probe can be considered isolated but still holds the initial design goals. Further experiments and simulations show that it is not advisable to increase the input impedance to isolation values of more than a few mega ohms. A higher input impedance would increase the noise and lead to a decreasing signal-to-noise ratio (SNR). Since capacitive parasitic effects of high-impedance resistors occur at much lower frequencies than with low-impedance resistors, the flatness of the frequency response and the bandwidth are also degraded. Isolated probes are therefore necessary when galvanic isolation is required. As summarized in Subsection 1.2.3.1 (Analog Isolated High Voltage Probes), commercially available analog isolated probes deliver a very high insulation barrier but are built for the use with low resolution oscilloscopes and not for high-precision measurements. Even digitally isolated probes, as shown in Subsection 1.2.3.2 (Digital Isolated High Voltage Probes), cannot be used for high-precision measurements in power electronics, as the probes use low-resolution converters and only transmit short-term measurement data sections. As a consequence a digitally isolated high voltage probe with continuous high-resolution data transfer is presented in Chapter 4 (Digital Isolated High Voltage Probe) and [**GSW18**]. Since the digitally isolated probe uses a floating divider at the front-end, the isolation impedance to ground is very high and the common-mode rejection ratio (CMRR) is inherently higher than from differential probes.

When developing high-precision measuring circuits, it is of interest how the accuracy is qualified and verified. With voltage probe circuits, the qualification of the dc parameters can be carried out with high-resolution bench multimeters, since the dc performance of these multimeters is very high. For the qualification of ac parameters, especially frequency response flatness, the standard approach of using a network analyzer does not provide the required frequency range and uncertainty. Thus an oscilloscope based alternative setup and procedure is introduced in Chapter 5 (Pass-band Frequency Response Measurement of a Voltage Probe) and [**GN19**]. The key of the presented method is to calibrate the setup at a low common-mode voltage with a low impedance reference attenuator in which parasitic behavior only occurs outside

the interesting frequency range. A final uncertainty analysis proves the suitability of the test setup.

Since each technical chapter of this thesis is based on a specific publication of the author, the publications are attached in the Appendix. For ease of reading, all citations to the author's publications are printed in bold. The following list summarizes the publications and their appendices:

- [**GSW14**] M. Grubmüller, B. Schweighofer, and H. Wegleiter. "Characterization of a resistive voltage divider design for wideband power measurements". In: *Proc. IEEE SENSORS*. 2014. DOI: 10.1109/ICSENS.2014.6985257 (Attached in Appendix A)
- [**GSW17**] M. Grubmüller, B. Schweighofer, and H. Wegleiter. "Development of a differential voltage probe for measurements in automotive electric drives". In: *IEEE Transactions on Industrial Electronics* 64.3 (2017), pp. 2335–2343. DOI: 10.1109/TIE.2016.2626374 (Attached in Appendix B)
- [**GSW18**] M. Grubmüller, B. Schweighofer, and H. Wegleiter. "A digital isolated high voltage probe for measurements in power electronics". In: *Proc. IEEE International Symposium on Industrial Electronics (ISIE)*. 2018. DOI: 10.1109/ISIE.2018.8433652 (Attached in Appendix C)
- [**GN19**] M. Grubmüller and M. Neumayer. "Passband frequency response measurement of a high voltage differential probe up to 10 MHz". In: *Proc. IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*. 2019 (Attached in Appendix D)

1.3.2 Industrial Utilization

A high voltage differential probe based on [**GSW17**] is produced by an industrial partner since 2018. Due to the high demand of the automotive industry for isolated probes, the company evaluates the design of the digital isolated probe presented in [**GSW18**] to incorporate the probe into the companies sales portfolio in the near future.

2

Frequency Compensated Voltage Divider

The common way to scale down a voltage is a pure resistive voltage divider (RVD). RVDs absolutely work for dc and low-frequency measurements. For wide-bandwidth measurements, ranging from dc up to a few megahertz, a frequency compensated voltage divider is necessary. A frequency compensated voltage divider is a mixed architecture of a resistive and a capacitive voltage divider. For the development of compensated voltage dividers an in-depth knowledge about non-ideal behavior of components and parasitic effects due to component placement on a printed circuit board (PCB) is necessary. In this chapter an explanation about the high frequency behavior of resistors and capacitors is given by using lumped element models. Further the influence of the PCB is taken into account. All models described in this chapter work well for frequencies up to several megahertz. For higher frequencies ($> 100\,\mathrm{MHz}$) more complex models are necessary. As a final step, an implementation example of a frequency compensated voltage divider and simulation results are shown.

The basics of this chapter are published in [**GSW14**] (Attached in Appendix A). The publication already contains a basic explanation of parasitic effects in voltage divider

circuits. This chapter complements the topic with the numerical modeling of the parasitic effects.

2.1 Resistor Lumped Element Model

In order to model the high-frequency (i.e. greater than a few kilohertz but below 100 MHz) behavior of a resistor, an $R\,L\,C$ equivalent circuit like in Figure 2.1 is used. The resistor R represents the nominal resistance. A series inductor L_{SER} models the parasitic inductance caused by the internal geometry of the resistor. A parallel capacitor C_{PAR} models the internal parasitic capacitance of the resistor.

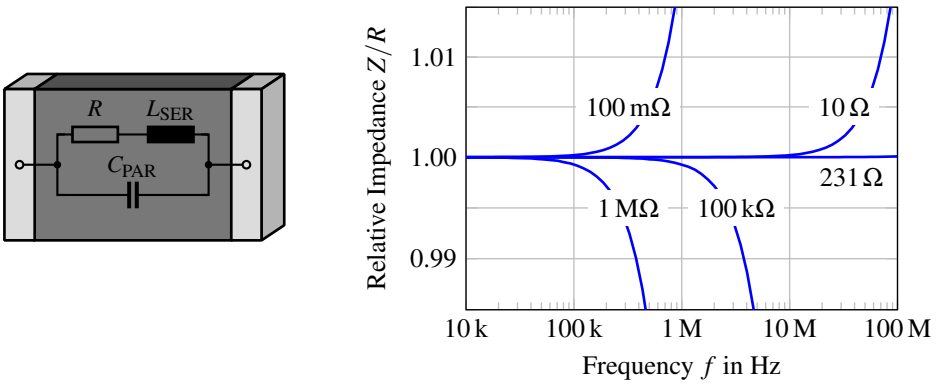


Figure 2.1: Lumped element model of a resistor (left) and relative impedance for different 1206 SMD resistors (right). R represents the nominal resistance, L_{SER} and C_{PAR} are the internal parasitic elements. A Resistors with $R = \sqrt{L_{\mathrm{SER}}/C_{\mathrm{PAR}}} = 231\,\Omega$ is nearly frequency independent up to 100 MHz, because by chance the value of the parasitic impedance is 231 Ω as well. Resistors with higher value show a decreasing impedance at high frequencies (capacitive behavior). Resistors with smaller value show an increasing impedance at high frequencies (inductive behavior).

The complex frequency dependent impedance $\underline{Z}$ of the component results to

$$\underline{Z} = (R + j\,\omega\,L_{\mathrm{SER}}) \,||\, \frac{1}{j\,\omega\,C_{\mathrm{PAR}}} \tag{2.1}$$

where the radian frequency $\omega = 2\,\pi\,f$. For low frequencies the reactance of the internal inductance L_{SER} is nearly zero and the reactance of the internal shunt capacitance C_{PAR} is very high. As a result the impedance Z of the circuit is equal to the nominal

resistor R at dc and low frequency. For increasing frequencies the internal inductance L_{SER} starts increasing the impedance Z of the circuit. On the other hand the internal shunt capacitance C_{PAR} starts decreasing the impedance Z of the circuit. Which one of the two effects will dominate, depends on the nominal value R of the resistor. For high-value resistors the internal shunt capacitance will dominate, for low-value resistors the internal inductance will dominate [TS02, Section 26.1]:

$R < \sqrt{L_{\mathrm{SER}}/C_{\mathrm{PAR}}} \quad \Rightarrow$ inductive behaviour

$R > \sqrt{L_{\mathrm{SER}}/C_{\mathrm{PAR}}} \quad \Rightarrow$ capacitive behaviour

$R = \sqrt{L_{SER}/C_{\mathrm{PAR}}} \quad \Rightarrow$ impedance of the resistor is nearly independent of frequency

Figure 2.1 shows the relative impedance over frequency of different valued SMD resistors with case size 1206. It shows the very flat impedance for a resistor with $R = \sqrt{L_{\mathrm{SER}}/C_{\mathrm{PAR}}}$. In the given frequency range of $f < 100\,\mathrm{MHz}$ the frequency dependent behavior of the resistor is completely described with the lumped circuit model shown in Figure 2.1 and no wave characteristics have to be considered. Thus the flat impedance resistance $R = \sqrt{L_{\mathrm{SER}}/C_{\mathrm{PAR}}}$ must not be mixed up with the $377\,\Omega$ wave impedance of free space. Resistors with greater resistance than $\sqrt{L_{\mathrm{SER}}/C_{\mathrm{PAR}}}$ show capacitive behavior at higher frequencies, resistors with lower resistance show inductive behavior at higher frequencies. Since voltage dividers for high voltages are built with high resistance input resistors, the capacitive behavior will be an issue. Inductive behavior may be a major issue for building shunt resistors for current measurement, where low-resistance resistors are used.

Classic wire-wound components may exhibit $20\,\mu\mathrm{H}$ of internal inductance L_{SER} and $5\,\mathrm{pF}$ of internal capacitance C_{PAR} [Ana83]. Modern small-sized high-frequency SMD components may have an inductance in the pico henry region and a capacitance of a few femto farad [Vis09]. For the development of a voltage divider the internal parallel capacitance C_{PAR} has been measured for different resistor packages. Values for the internal inductance L_{SER} may be approximated by $1\,\mathrm{nH/mm}$ multiplied by the package length of the component [TS02, Section 26.1]. Results are shown in Table 2.1. The table also shows the value for a maximum flat impedance $\sqrt{L_{\mathrm{SER}}/C_{\mathrm{PAR}}}$ for the regarding component packages.

Table 2.1: Values for parasitic elements of a resistor for different SMD packages

Package Imperial code	Length mm	Width mm	C_{PAR} [a] fF	L_{SER} [b] nH	$\sqrt{L_{SER}/C_{PAR}}$ Ω
0402	1.0	0.5	37	1.0	164
0603	1.6	0.85	46	1.6	187
0805	2.0	1.2	58	2.0	186
1206	3.2	1.6	60	3.2	231
MELF MMA	3.6	1.4	85	3.6	206
MELF MMB	5.8	2.2	107	5.8	233

[a] Measured values
[b] Approximated with 1 nH/mm

2.2 Capacitor Lumped Element Model

The frequency dependency of the impedance of a capacitor is modeled by a damped series resonant circuit like shown in Figure 2.2. The capacitor C models the nominal capacitance. A series resistor R_{SER} is used to model the dielectric losses of the component. The series inductor L_{SER} models the parasitic inductance, caused by the internal geometry of the resistor. In literature, the series resistor R_{SER} and the series inductor L_{SER} are often refereed as to equivalent series resistance (ESR) and equivalent series inductance (ESL). For some applications it is further necessary to introduce a parallel leakage resistance R_{PAR}. For the application of an RVD the parallel resistance R_{PAR} may be neglected because a much smaller resistor will be connected in parallel. The complex frequency dependent impedance $\underline{Z}$ of the component results to

$$\underline{Z} = R_{SER} + j\,\omega\,L_{SER} + \frac{1}{j\,\omega\,C}, \tag{2.2}$$

following to the self-resonant frequency at

$$\omega_r = \frac{1}{\sqrt{L_{SER}\,C}}. \tag{2.3}$$

Some manufacturers provide values for the internal inductance L_{SER} and the internal series resistance R_{SER} in the datasheet or provide simulation tools, e.g. *Kemet K-SIM* [Kem18a] and *AVX SpiCAT* [AVX19]. The series inductance L_{SER} is in the region of 0.5 nH to 1 nH for SMD components. The series resistance R_{SER} strongly de-

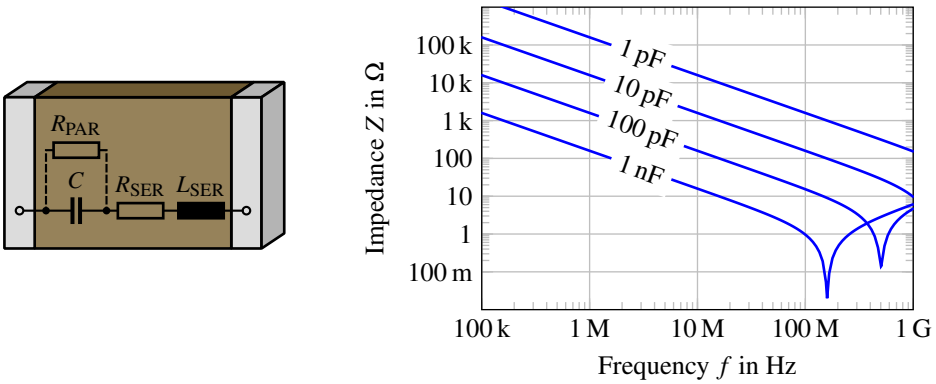
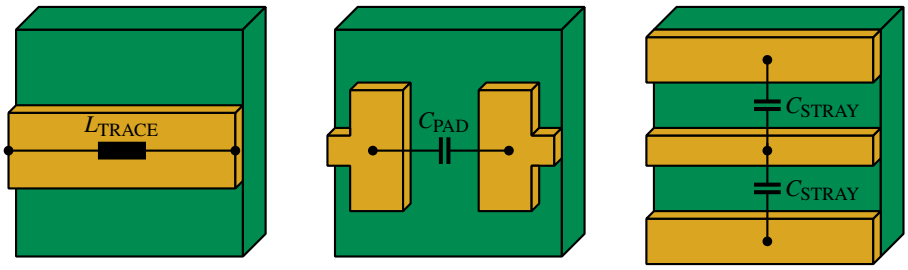


Figure 2.2: Lumped element model of a capacitor (left) and frequency dependent impedance of 0603, C0G dielectric, SMD capacitors with different nominal values (right). The capacitor C represents the nominal capacitance, R_{PAR} , R_{SER} and L_{SER} are the internal parasitic elements.

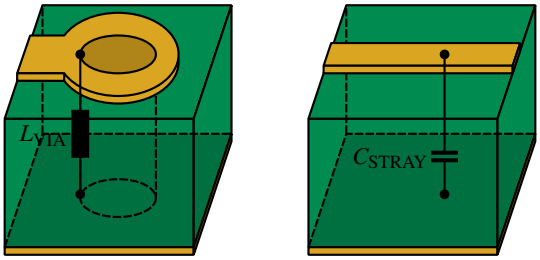
pends on the used dielectric type and the nominal capacitance C. For C0G dielectrics the series resistance R_{SER} varies from several milliohm to a few ohm. Figure 2.2 shows the impedance curve for different valued 0603, C0G dielectric, SMD capacitors. The components have a capacitive behavior up to the self-resonant frequency f_r. For frequencies higher than the self-resonant frequency f_r, the capacitors show inductive behavior.

2.3 PCB High Frequency Model

As with components, inductive and capacitive elements can be used to model the non-ideal behavior of the PCB (Figure 2.3). Traces and vias show inductive behavior, modeled by the trace inductance L_{TRACE} and via inductance L_{VIA}. Between the solder lands of components the pad-to-pad capacitance C_{PAD} acts in parallel to the soldered component. The stray capacitance C_{STRAY} occurs between a trace and any other conducting part of the PCB or a supply layer.



(a) Trace inductance (b) Pad-to-pad capacitance (c) Stray capacitance 1



(d) Via inductance (e) Stray capacitance 2

Figure 2.3: Modeling PCB parasitic effects with passive equivalent components. Inductors L_{TRACE} (a) and L_{VIA} (d) model the trace and via inductance. The pad-to-pad capacitance of solder lands is described by C_{PAD} (b) and is in parallel with the soldered component. A stray capacitance C_{STRAY} occurs between a trace and any other conducting part of the PCB (c) or the ground plane (e).

2.3.1 Trace and Via Inductance

First of all it has to be stated that the inductance of single circuit parts like a trace or via has no meaning. Therefor the concept of partial inductances is used [Rue72]. Thus the inductors shown in Figure 2.3 are partial inductances and the resulting inductance is the sum of all partial inductances forming a closed circuit. The partial trace inductance L_{TRACE} can be calculated by using the formula of the self inductance of a straight rectangular bar with length l, width w and thickness t [RG12, Chapter 8]:

$$L_{TRACE} = 200\,l\left(\ln\frac{2\,l}{w+t}+\frac{1}{2}+0.2235\,\frac{w+t}{l}\right)10^{-9}\,. \tag{2.4}$$

The partial inductance of a via L_{VIA} can be approximated by the self inductance of a straight cylindrical wire with length l and diameter d [RG12, Chapter 8]:

$$L_{VIA} = 200\,l\left(\ln\frac{4\,l}{d}-\frac{3}{4}\right)10^{-9}\,. \tag{2.5}$$

Formulas 2.4 and 2.5 are only rough estimations, some books and application notes may give slightly different formulations, e.g. [Ana05]. Figure 2.4a shows the resulting partial trace inductance L_{TRACE} for a standard 35 μm thick trace. Figure 2.4b shows the partial via inductance L_{VIA} depending on the via diameter for a standard 1.6 mm thick PCB.

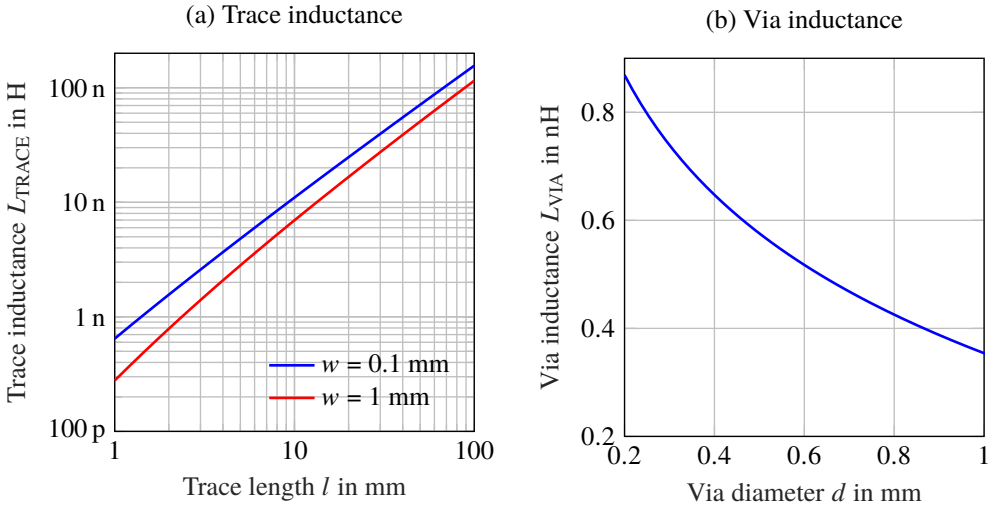
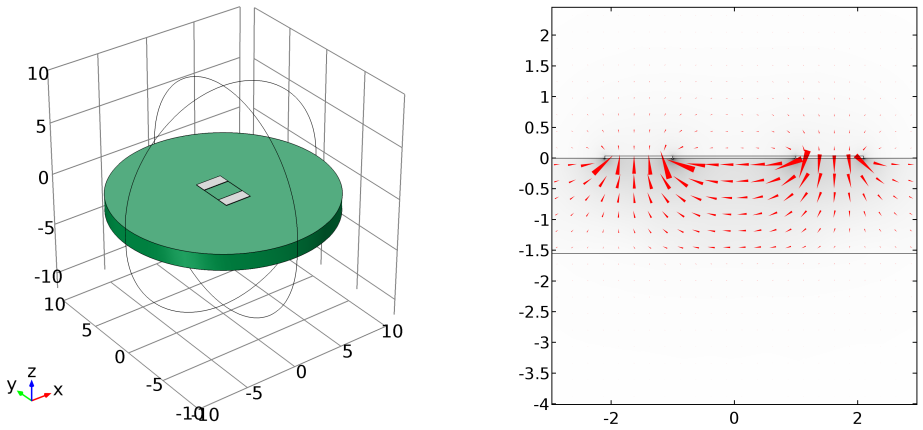


Figure 2.4: Partial trace inductance for a 35 μm thick trace for different trace widths and lengths (b), and partial via inductance for a standard 1.6 mm thick PCB for different via diameters (b).

2.3.2 Pad-to-Pad Capacitance

The pad-to-pad capacitance C_{PAD} is determined by a FEM simulation of the geometry shown in Figure 2.5a. Results are in the range of 62 fF for 0402 footprints up to 118 fF for 1206 footprints. Simulations are done with an *Isola DE104* standard FR4 PCB material with a relative permittivity of $\epsilon_r = 4.37$. Since the electric displacement vectors are mainly going through the PCB, the pad-to-pad capacitance could be lowered by about 20 % by using a *Rogers RO3450B* high frequency PCB material with a relative permittivity of $\epsilon_r = 3.48$, but still not neglected (Figure 2.5b). For the initial simulation, footprint dimension according to the *IPC Standard for Surface Mount Design and Land Pattern* are used [IPC99]. Depending on the electronic design automation (EDA) software used, also the actual footprint dimensions can vary greatly, resulting in a change of the pad-to-pad capacitance C_{PAD} of more than 50 %. Further simulations with different geometries and corresponding measurements

showed, that an approximation of the pad-to-pad capacitance C_{PAD} by using the parallel capacitance C_{PAR} of the resistor model is a good rule of thumb (values for the parallel capacitance C_{PAR} are in Table 2.1 of Section 2.1).



(a) 3d simulation model (b) Electric displacement (zy-plane)

Figure 2.5: Simulation setup to determine the pad-to-pad capacitance of an SMD footprint (a). The resulting electric displacement vectors are concentrated in the PCB (b). Axis dimensions are in millimeter.

2.3.3 Stray Capacitance

Further a reliable value for the stray capacitance C_{STRAY} has to be obtained. The stray capacitance occurs between the components and any other conductors, like other traces, a ground plane or a conductive part of the PCB surrounding. It is very important to reach a constant and predictable value for C_{STRAY} for building a frequency compensated voltage divider. It is a good practice to omit any ground and supply plane below the divider and place a conductive shield connected to ground around the divider (Figure 2.6).

In a first step the stray capacitance C_{STRAY} is calculated with a 2d FEM simulation with the geometry shown in Figure 2.6 (left). In a second step the geometry is simplified to an eccentric rectangular coaxial conductor (Figure 2.6 right). With this

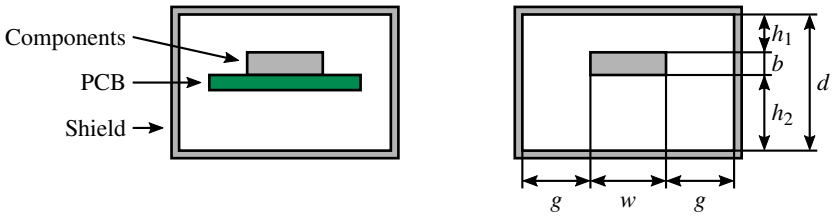


Figure 2.6: Assembly of SMD components on a PCB with surrounding metal shield (left) and simplified geometry for approximation of the stray capacitance (right).

simplification an approximation with a closed form calculation is possible:

$$\begin{aligned} C'_{\mathrm{STRAY}} &= \epsilon \left(2\frac{b}{g} + \frac{w}{h_1} + \frac{w}{h_2}\right) \ldots \\ &\quad + 4\frac{\epsilon}{\pi}\left[\frac{d}{d-b}\ln\left(\frac{2d-b}{b}\right) + \ln\left(\frac{b(2d-b)}{(d-b)^2}\right)\right] \ldots \\ &\quad \cdot \frac{\ln\left(1+\coth\left(\frac{\pi g}{d}\right)\right)}{\ln 2}. \end{aligned} \tag{2.6}$$

Formulation (2.6) is an adapted version of the *capacitance of rectangular lines with thin inner conductors* [Che60] where the conductor thickness $b < d/3$ but still appreciable. For the used geometry of $w = 5\,\mathrm{mm}$, $b = 2\,\mathrm{mm}$ for the inner conductor and $g = 7\,\mathrm{mm}$, $h_1 = 3.8\,\mathrm{mm}$ and $h_2 = 5.8\,\mathrm{mm}$ for the spacings, the 2d FEM simulation results to specific stray capacitance $C'_{\mathrm{STRAY}} = 53\,\mathrm{pF/m}$. The analytic calculation delivers a specific stray capacitance $C'_{\mathrm{STRAY}} = 49\,\mathrm{pF/m}$, which is a good enough to approximate parasitic behavior.

2.4 Practical Example of a Frequency Compensated Voltage Divider

In this subsection the development of a frequency compensated high voltage divider is explained step by step. The divider can be used as a stand-alone circuit, but in this thesis the divider is used as input stage for a high voltage differential probe and for an isolated high voltage probe explained in Chapters 3 and 4. In this chapter the theoretical calculation steps and simulation results are shown. Experimental results are presented in the particular chapters, dealing with the development of the high voltage differential probe and the isolated high voltage probe. For the divider, special

care is taken to reach a flat passband frequency response up to 1 MHz and a good linearity up to the maximum input voltage of ±1500 V. The nominal attenuation G of the the divider is selected to $G = 1/600$, so that the maximum output voltage swing is ±2.5 V. The low output voltage swing of ±2.5 V is chosen because of the availability of high speed and high input impedance amplifiers following the voltage divider. Figure 2.7 shows a schematic of the divider. It consists of an input divider that is left slightly under-compensated and a lag circuit for final frequency response compensation. A description of the individual elements and their calculation is given by the following list.

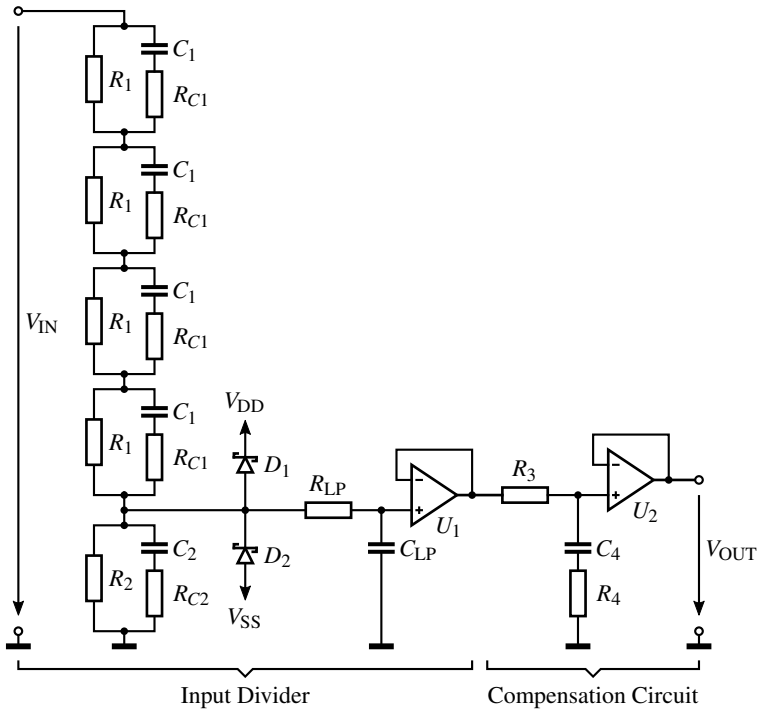


Figure 2.7: Schematic of a frequency compensated voltage divider. It consists of an input divider which is slightly under-compensated and a lag circuit for frequency response compensation.

- Resistive voltage divider with R_1 and R_2
  For dc and low frequency, the circuit acts as a resistive voltage divider built by $N_1 \cdot R_1$ and R_2. $N_1 = 4$ is the number of identical blocks in the high voltage arm of the divider. The division into N_1 partial blocks makes sense as the individual blocks then do not have to withstand the full input voltage. In order to avoid loading the device under test (DUT), the high voltage resistor R_1 is selected with a high value of 2 MΩ, resulting in an input resistance of approximately $N_1 \cdot R_1 = 8\,\text{M}\Omega$. The

output resistor R_2 is then calculated from the attenuation G_{divider} to

$$G_{\text{divider}} = \frac{R_2}{N_1 R_1 + R_2} \Rightarrow R_2 = \frac{N_1 R_1}{\frac{1}{G_{\text{divider}}} - 1} = 13.356\,\text{k}\Omega \approx 13\,\text{k}\Omega + 360\,\Omega\,. \quad (2.7)$$

To avoid any non-linearity caused by self-heating of R_1 due to the high input voltage, resistors with low temperature coefficient are chosen. The *Vishay TNPV120e3* precision thin film flat chip resistor family provide a temperature coefficient of $\pm 25\,\text{ppm/K}$ and a voltage coefficient of $1\,\text{ppm/V}$. Assuming a thermal resistance of $R_{th} = 32\,\text{K/W}$ for the resistor, a worst-case non-linearity of 430 ppm caused by self heating and voltage dependence of the resistors may occur at the maximum input voltage of 1500 V [Vis11] .

- Capacitive voltage divider with C_1 and C_2:
  At high frequencies, the capacitive voltage divider with C_1 and C_2 dominates over the resistive divider R_1 and R_2. The high voltage capacitor $C_1 = 22\,\text{pF}$ is selected to be at least 100 times greater than the parasitic capacitance C_{PAR} of the high voltage resistor R_1. For good stability over voltage and temperature, the capacitor must be a C0G, sometimes also labeled NP0, dielectric type. C0G has negligible change in capacitance with respect to time, voltage and ambient temperature [Kem18b]. In theory the divider is compensated by choosing the output capacitor C_2 to validate

$$G_{\text{divider}} \coloneqq \frac{\frac{C_1}{N_1}}{\frac{C_1}{N_1} + C_2 + C_{\text{LP}}} \Rightarrow C_2 = \frac{C_1}{N_1}\left(\frac{1}{G_{\text{divider}}} - 1\right) - C_{\text{LP}} = 3.280\,\text{nF} \quad (2.8)$$

  In practice, (2.8) is only a rough approximation because it does not consider any parasitic behavior of components and the PCB. For this reason, oscilloscope probes typically have an adjustable capacitor C_2. For the presented voltage divider, a frequency response flatness of about $\pm 0.5\,\%$ could be reached by manual fine tuning the output capacitor C_2 to 2.936 nF (Figure 2.8). To reach a frequency response flatness better than $\pm 0.5\,\%$, an additional frequency response correction with a lag circuit is introduced.

- Lag circuit with R_3, R_4 and C_4:
  To compensate the divider with a lag circuit, the output capacitor C_2 is chosen so that the divider remains under-compensated by approximately 1 dB. This is

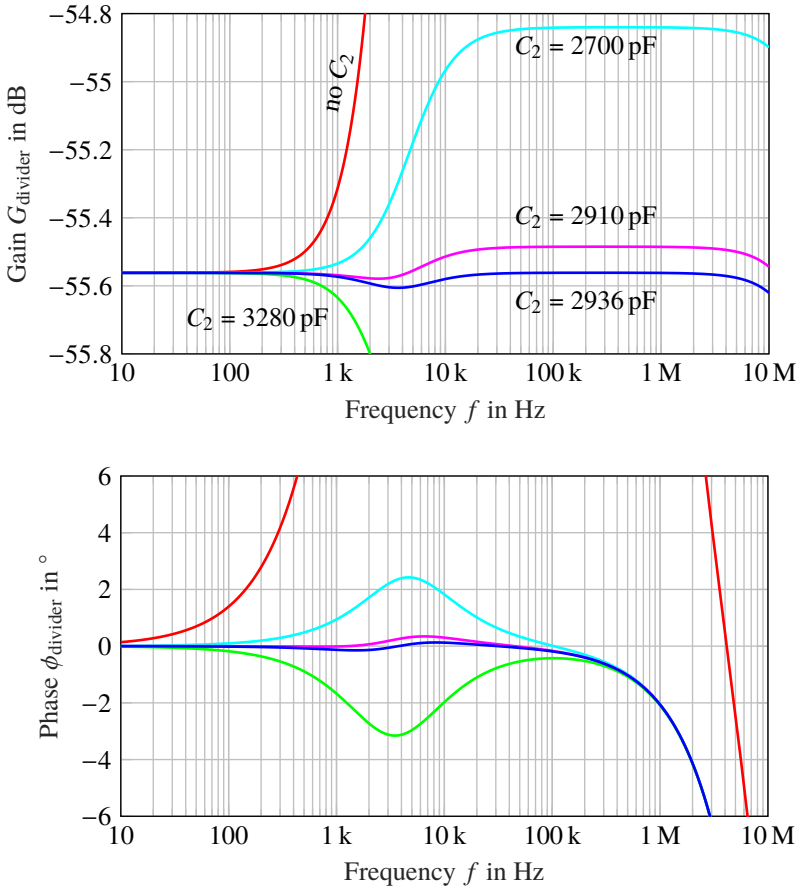


Figure 2.8: Frequency response compensation by adjusting capacitor C_2. The circuit shown in Figure 2.7 is used for the underlying simulation. In addition, the parasitic effects explained in the chapter are taken into account.

reached by choosing

$$C_2 = 0.8\,C_1\,\frac{R_1}{R_2} = 2.635\,\text{nF} \approx 2.7\,\text{nF}, \tag{2.9}$$

which is empirically determined and confirmed by circuit simulation (Figure 2.9a). For compensation, the under-compensated divider is then followed by a lag circuit. The lag circuit has a dc gain of one and attenuates signals at high frequencies due to the resistive divider built with R_3 and R_4 (Figure 2.9b). To compensate the voltage divider, the frequency response $G_{\text{comp.}}$ of the lag circuit

$$G_{\text{comp.}}(f) = \frac{\sqrt{(2\pi f)^2 R_4^2 C_4^2 + 1}}{\sqrt{(2\pi f)^2 (R_3 + R_4)^2 C_4^2 + 1}} \tag{2.10}$$

has to fulfill

$$G_{\text{comp.}}(f) \coloneqq \frac{G_{\text{divider}}(0)}{G_{\text{divider}}(f)}\,. \tag{2.11}$$

This is reached by selecting a fixed value for $R_3 = 1\,\text{k}\Omega$ and further formulating an optimization problem to get values for R_4 and C_4. The nonlinear optimization problem is expressed by finding the minimum of the cost function

$$\min \left\| G_{\text{comp.}}(f, R_4, C_4) - \frac{G_{\text{divider}}(0)}{G_{\text{divider}}(f)} \right\|, \tag{2.12}$$

parameterized by R_4 and C_4. The constraints $R_4 > 0$ and $C_4 > 0$ are chosen to obtain only physically correct solutions. The resulting circuit then has a gain flatness better than $\pm 0.1\,\%$ (Figure 2.9c).

- Damping resistors R_{C1} and R_{C2}:
  The damping resistor R_{C1} is introduced to limit the current, and further the power loss, through the capacitor C_1 in case of fast transient input signals, but not the slope of the input signal. The resistance is chosen to $R_{C1} = 100\,\Omega$. The subsequent resistor R_{C2} is calculated to reach the same time constant for the low and high voltage arm of the divider,

$$\tau_1 \coloneqq \tau_2 \Rightarrow R_{C1}\,C_1 = R_{C2}\,C_2 \Rightarrow R_{C2} = \frac{R_{C1}\,C_1}{C_2} = 0.815\,\Omega \approx 1\,\Omega\,. \tag{2.13}$$

- Clamping Diodes D_1 and D_2:
  The clamping diodes are necessary to limit the input voltage of the voltage

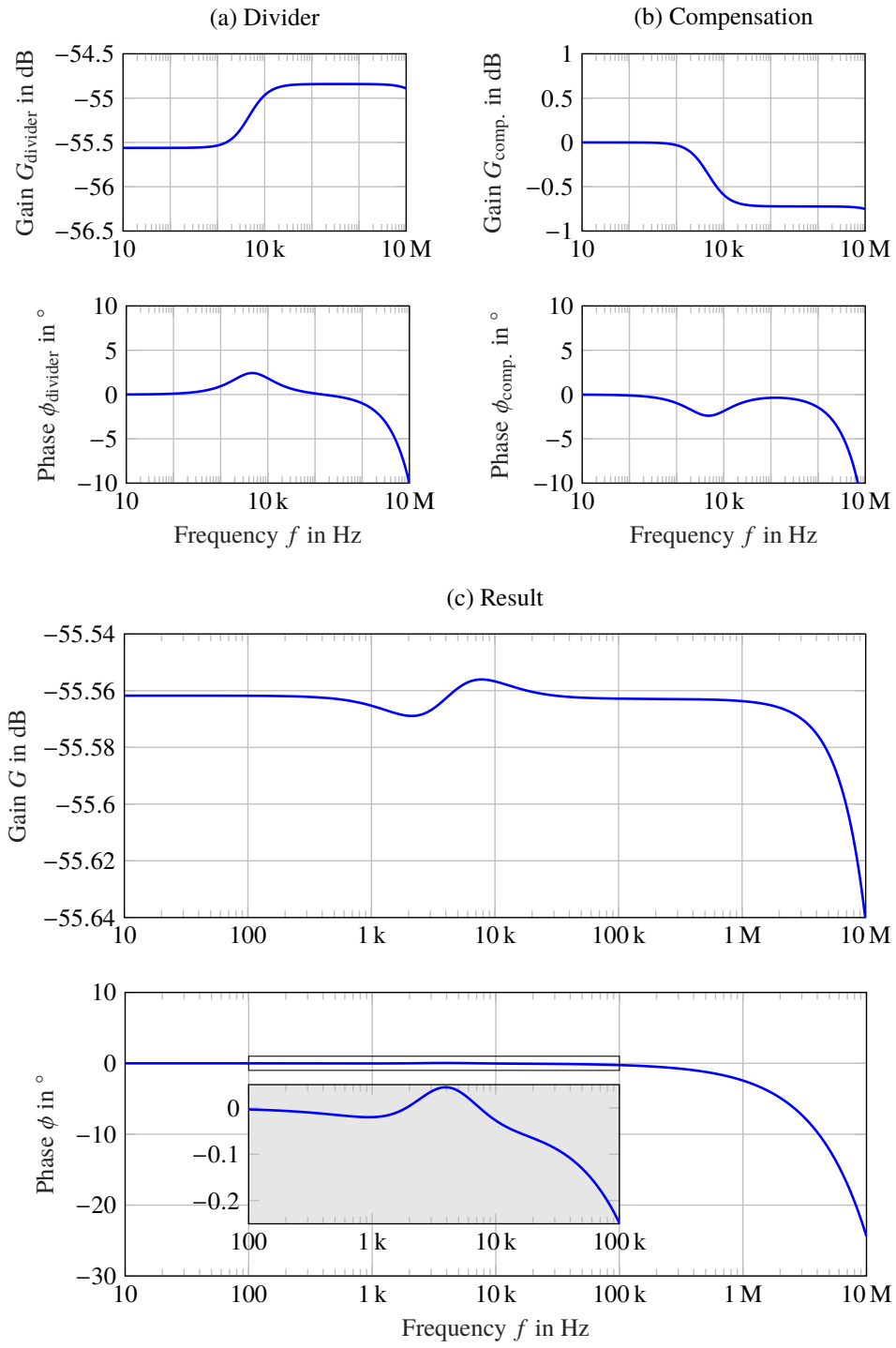


Figure 2.9: Simulated Bode plots of the input divider, the lag circuit and the resulting compensated voltage divider. The input divider (a) is left under-compensated by about 1 dB. A lag circuit (b) with the inverse ac transfer function of the divider follows the divider. As a result the transfer function of the whole circuit (c) has a gain flatness of ±0.1 % up to 1 MHz.

buffer U_1. Low capacitance diodes are selected to prevent any influence on the input divider frequency response characteristics. The *ON Semiconductor BAS40-04* dual series Schottky barrier diode is an ideal candidate for that purpose. Its total capacitance of 5 pF hardly influences the voltage divider.

- Low pass with R_{LP} and C_{LP}:
  A passive first order low-pass filter is introduced to bloc high frequency disturbances. The cutoff frequency is set to 100 MHz by choosing $R_{LP} = 100\,\Omega$ and $C_{LP} = 15\,\text{pF}$.

- Buffer amplifiers U_1 and U_2:
  To avoid loading the input divider and the lag circuit, the buffer amplifiers U_1 and U_2 are necessary. Field-effect transistor (FET) input stage types with low input capacitance and high input resistance are used to avoid feedback due to the input impedance of the amplifiers. The *Analog Devices AD8065* is a 145 MHz FET input operational amplifier (op-amp) with a typical input impedance of $1\,\text{T}\Omega\,||\,4.5\,\text{pF}$.

Finally, it can be stated that the stray capacitance (Figure 2.3 (c) and (e)) is the most critical parasitic effect. It is very sensitive to variations in geometry and material properties. Trace and via inductances can be neglected in the design of high impedance dividers if short traces and cables are used. For mass production of flat frequency response dividers, regardless of environmental conditions, the divider and the surrounding metal shield (Figure 2.6) could be manufactured as a single hermetically sealed unit.

3
High Voltage Differential Probe

Since phase-to-phase voltages are of interest for research and develpment (R&D) of electric drives, a differential voltage measurement is required. Typical voltage levels are in the range of several hundred volts for industrial electric drives and electric passenger cars, but can exceed one kilovolt for heavy duty applications. The switching frequency of inverters is in the range of several tens of kilohertz. Taking all these facts into account, a differential voltage probe with a flat passband frequency response up to a megahertz and an input voltage range of more than one kilovolt is required. High voltage differential probes are the best all-around probes for this [JM18]. This chapter presents the development of a high voltage differential probe. Special attention is paid to a flat frequency response and a high linearity over the entire input voltage range. A detailed experimental characterization of a prototype confirms the achievement of the design goals.

The prototype is a further development of the probe presented in [**GSW17**] (Attached in Appendix B). The probe presented in the publication was built with an input impedance of 4 MΩ and for a maximum input voltage of 1 kV. Various field applications showed that these values were too low. So the advanced prototype presented in this chapter has an input impedance of 8 MΩ and can work with input voltages up to 1.5 kV.

3.1 Concept of the 3+1 Phase High Voltage Differential Probe

A differential high voltage probe consists of two well matched input dividers followed by a differential amplifier. Each input voltage is reduced by one of the voltage dividers between phase and protective earth (PE). The output voltage of the probe is then delivered by a differential amplifier. Since an inverter for electric drives has one dc input and three ac output voltages, four differential probes are required to measure all input and output voltages simultaneously (Figure 3.1). Thus, on the ac side of the inverter, each phase is loaded by two voltage dividers in parallel. As a result, three dividers are redundant and the instrument impedance seen by the inverter is halved on each phase.

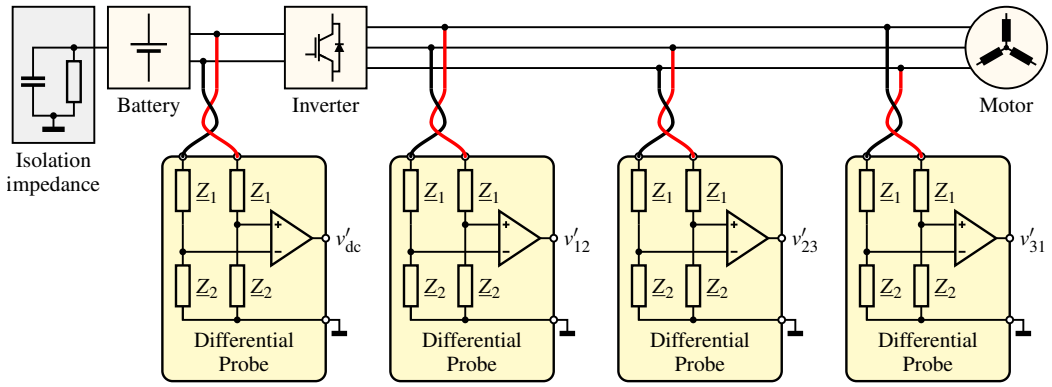


Figure 3.1: Conventional measurement setup for the measurement of input and output voltages of an inverter. To characterize a typical drive train, four differential probes are needed. At each probe, two dividers scale down the input voltages. A differential amplifier then delivers the output signal.

This thesis presents a probe concept especially for measurements in electric drives (Figure 3.2). For the measurement of the ac output voltages only three voltage dividers are used. The load impedance, seen by the inverter, is therefore twice as high as the impedance of the structure with individual differential probes.

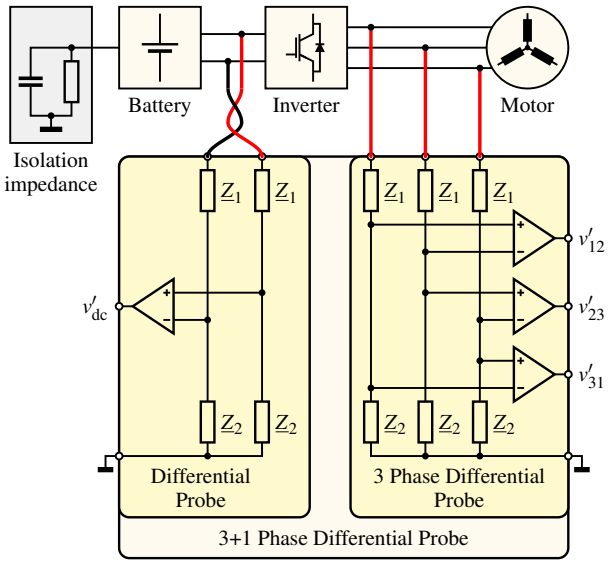


Figure 3.2: Differential probe for measurements in electric drives. On the ac side only three voltage dividers are needed for the voltage measurement.

3.2 Development of a High Voltage Differential Probe for Measurements in Automotive Electric Drives

3.2.1 Input Divider

The main components of the probe are the input dividers and a differential amplifier. The input divider has an attenuation 1/600 to scale down the maximum input working voltage of ±1500 V to ±2.5 V. The circuit is explained in detail in Chapter 2. The used components limit the maximum allowable non-destructive input voltage (input to ground) to 4 kV. To allow a safe operation up to 2 kV, air gaps and creepage distances are chosen according the standards IEC 60664-1 [IEC07], IEC 61010-1 [IEC10] and IPC-2221B [IPC03].

3.2.2 Differential Amplifier

To obtain the difference of the input voltages and amplify the difference, the known differential amplifier circuit shown in Figure 3.3 is used [HH15, Chapter 4.2.4]. In addition to generating the difference between positive and negative probe inputs, the differential amplifier also has a gain of 4 to achieve a probe attenuation of 1/150. The resulting probe output voltage swing of ±10 V is chosen to best utilize industrial digitizers for automotive test beds. An output resistor $R_{\text{out}} = 50\,\Omega$ is added to drive coaxial cables. Regarding simplicity and CMRR an integrated instrumentation amplifier (INA) would be the better choice than the used differential amplifier circuit. Commercially available INAs however have a very limited bandwidth of a few megahertz.

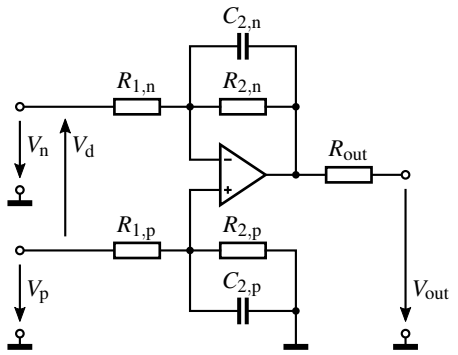


Figure 3.3: Differential amplifier circuit with additional capacitors for adding first order low pass behavior. For the resistors a resistor array is used to reach a high CMRR low gain drift.

The complex transfer function $\underline{G}$ of the circuit is

$$\underline{G} = \frac{R_2}{R_1} \frac{1}{1 + j\,\omega\,R_2\,C_2}, \tag{3.1}$$

where R_1, R_2 and C_2 are the nominal values of $R_{1,\text{n}}$, $R_{2,\text{n}}$, $R_{1,\text{p}}$, $R_{2,\text{p}}$, $C_{2,\text{n}}$ and $C_{2,\text{p}}$; the latter variables are the real components with tolerances. By comparing 3.1 with the standard transfer function of a first order low pass filter, it can be seen that the differential amplifier has a dc gain G_0 of

$$G_0 = \frac{R_2}{R_1} \tag{3.2}$$

and a low pass behavior with a cut-off frequency f_c at

$$f_c = \frac{1}{2\pi R_2 C_2}. \tag{3.3}$$

In order to achieve a high CMRR, a quad resistor array with very low net matching tolerance t_R is used for the resistors R_1 and R_2. The *Vishay MORN* series surface-mount network has a matching tolerance of ±0.05 % and a matching drift of 2 ppm/K. The capacitor C_2 is a standard $t_C = 5\,\%$ tolerance type. The contribution of the resistor mismatch to the CMRR of the amplifier circuit is demonstrated in [PW91]

$$\mathrm{CMRR}_R = \frac{1}{2} \cdot \frac{2R_{2,\mathrm{n}} R_{2,\mathrm{p}} + R_{1,\mathrm{p}} R_{2,\mathrm{n}} + R_{1,\mathrm{n}} R_{2,\mathrm{p}}}{R_{1,\mathrm{n}} R_{2,\mathrm{p}} - R_{1,\mathrm{p}} R_{2,\mathrm{n}}}. \tag{3.4}$$

To also consider the capacitors, $R_{2,\mathrm{n}}$ and $R_{2,\mathrm{p}}$ are extended with their corresponding parallel capacitors $C_{2,\mathrm{n}}$ and $C_{2,\mathrm{p}}$

$$\begin{aligned}\mathrm{CMRR}_{RC}(f) = \Bigg| \frac{1}{2} \cdot \frac{1}{R_{1,\mathrm{n}}(R_{2,\mathrm{p}}||C_{2,\mathrm{p}}) - R_{1,\mathrm{p}}(R_{2,\mathrm{n}}||C_{2,\mathrm{n}})} \cdots \\ \cdot \left(2(R_{2,\mathrm{n}}||C_{2,\mathrm{n}})(R_{2,\mathrm{p}}||C_{2,\mathrm{p}}) \ldots \right. \\ \left. + R_{1,\mathrm{p}}(R_{2,\mathrm{n}}||C_{2,\mathrm{n}}) + R_{1,\mathrm{n}}(R_{2,\mathrm{p}}||C_{2,\mathrm{p}})\right) \Bigg|. \end{aligned} \tag{3.5}$$

For a worst case estimation, the values are then chosen to

$$R_{1,\mathrm{n}} = R_1(1 + t_R/2), \tag{3.6}$$

$$R_{2,\mathrm{n}} = R_2(1 - t_R/2), \tag{3.7}$$

$$C_{2,\mathrm{n}} = C_2(1 - t_C), \tag{3.8}$$

$$R_{1,\mathrm{p}} = R_1(1 - t_R/2), \tag{3.9}$$

$$R_{2,\mathrm{p}} = R_2(1 + t_R/2), \tag{3.10}$$

$$C_{2,\mathrm{p}} = C_2(1 + t_C), \tag{3.11}$$

where t_R is the net matching tolerance of the resistors and t_C is the tolerance of the capacitors. Because of using a resistor array, $t_R/2$ is used to guarantee a deviation of maximum t_R from one resistor to all others. In a final step, the op-amp CMRR is

considered to get the overall CMRR of the whole amplifier circuit [PW91]

$$\frac{1}{\mathrm{CMRR}(f)} \approx \frac{1}{\mathrm{CMRR}_{RC}(f)} + \frac{1}{\mathrm{CMRR}_{\mathrm{op-amp}}(0)} \cdots + \frac{1}{\mathrm{CMRR}_{\mathrm{op-amp}}(0)} \cdot \frac{f}{f_{c,\mathrm{CMRR}}}, \tag{3.12}$$

where $\mathrm{CMRR}_{\mathrm{op-amp}}(0)$ is the low-frequency CMRR of the op-amp and $f_{c,\mathrm{CMRR}}$ is the frequency where the CMRR of the op-amp has decreased by 3 dB. The calculation results to a CMRR of 66 dB up to 100 kHz and decreases to 44 dB at 10 MHz.

3.3 Experimental Characterization of a Prototype

In this chapter the development and characterization of a high voltage differential probe was shown. Compared to commercially available probes, attention was paid to a flat passband frequency response and high linearity. Experiments with a prototype, shown in Figure 3.4, confirmed the achievement of the design goals. The prototype is a four channel device to simultaneously measure a dc battery voltage (inverter input) and a three-phase ac voltage (inverter output). Presented measurement results are from a single channel of the probe but do represent all other channels as well. The high voltage inputs are accessible via safety banana jacks. Input attenuators are surrounded by a metal housing to achieve a defined stray capacitance. Low-voltage output signals are provided by coaxial connectors. The outputs are driven by an amplifier circuit with 50 Ω output resistance to drive coaxial cables. The following subsections explain the performed characterization measurements. The results are summarized int Table 3.1 and Figure 3.5 in Section 3.4 at the end of this chapter.

3.3.1 Input Parameters

The input impedance for each channel is 8 MΩ for dc and low-frequency from phase to ground and 16 MΩ from phase-to-phase respectively. For increasing frequencies the input impedance decreases due to the capacitive part of the input divider. The input capacitance is 5.5 pF from phase to ground and 2.3 pF phase-to-phase (Figure 3.5a). This increases the input current and the power loss at the input attenuator with increasing frequency. To avoid any damages to the components, a derating curve is calculated to limit the temperature rise of the input capacitors to 20 K. As a result the

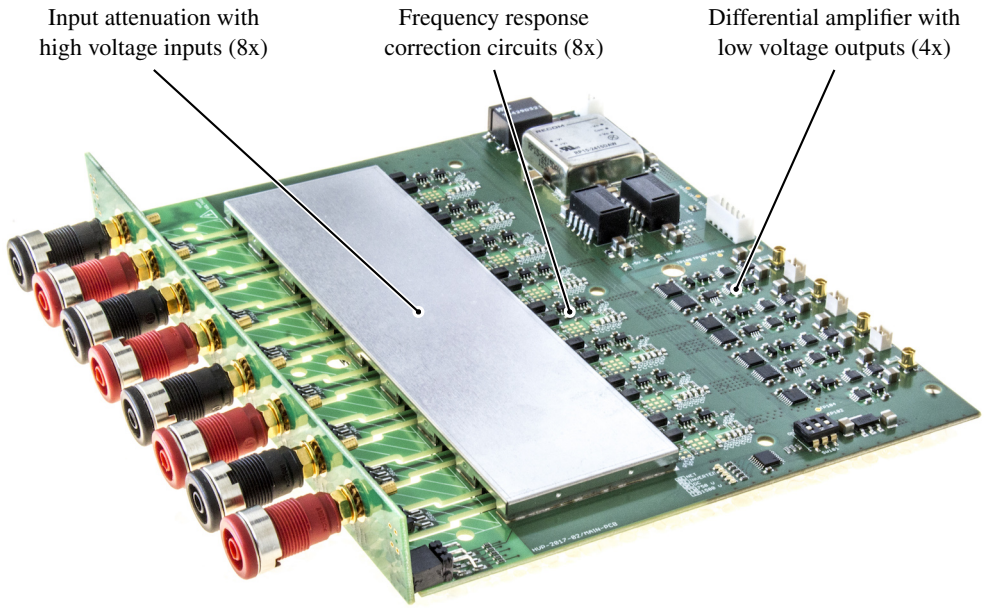


Figure 3.4: Prototype of the high voltage differential probe for measurements in automotive electric drives. The input voltage dividers are hidden under the metal shield.

maximum working voltage of 1.5 kV may be applied up to 1 MHz, a 10 MHz signal must not exceed 150 V (Figure 3.5b).

3.3.2 DC Characterization

The probe is designed to have an attenuation of 1/150. The measurement of the nominal attenuation G_{nom} is done according to the *IEEE Standard for Terminology and Test Methods for Circuit Probes* [IEE14]. Input and output voltage V_{in} and V_{out} of the probe are measured while stepping the input voltage up to the full-scale range (FSR) voltage of 1500 V. The nominal attenuation G_{nom} is then defined by approximating the slope $V_{\text{out}} = f(V_{\text{in}})$ by a linear curve fit over the first half of the input FSR. The change of the attenuation as a function of the input voltage level, the non-linearity $\epsilon_{\text{non-lin}}$, is an important quality feature of the probe. The non-linearity is defined by the maximum deviation of the measured attenuation from the nominal attenuation

$$\Delta G = \max |G(V_{\text{in}}) - G_{\text{nom}}| \,. \tag{3.13}$$

The prototype shows a maximum relative nonlinearity $\Delta G/G_{\text{nom}}$ of ±80 ppm up to the maximum input voltage of 1500 V.

Output offset voltage drift $\Delta V_0/\Delta\vartheta = \pm 310\,\mu\mathrm{V/K}$ and gain drift $\Delta G/(\Delta\vartheta \cdot G_{\mathrm{nom}}) = \pm 50\,\mathrm{ppm/K}$ are calculated according to the GUM [JCG08] for a confidence interval of 99.7 %. Climate chamber tests with temperatures from −10 °C to +50 °C showed an output offset voltage drift of $\Delta V_0/\Delta\vartheta = \pm 33\,\mu\mathrm{V/K}$ and a gain drift of $\Delta G/(\Delta\vartheta \cdot G_{\mathrm{nom}}) = \pm 16\,\mathrm{ppm/K}$ for the prototype.

3.3.3 AC Characterization

Since the high voltage differential probe is designed for wide bandwidth measurements in electric drives, the frequency response, especially the passband frequency response flatness, is an important parameter. Small signal measurements with an input amplitude of $\widehat{v}_{\mathrm{in}} = 1\,\mathrm{V}$ confirmed the −3 dB bandwidth of the probe at about 30 MHz (Figures 3.5d and 3.5e). The phase is about −390 °at the −3 dB bandwidth. The passband frequency response flatness of ±0.1 % holds up to 1 MHz (Figure 3.5f).

Further a high CMRR is important for measurements in electric drives. It describes the ability of the probe to suppress common-mode signals. It is defined by

$$\mathrm{CMRR} = 20\log\left(\frac{G}{G_{\mathrm{CM}}}\right), \tag{3.14}$$

where G is the attenuation for differential input signals and G_{CM} is the attenuation for common-mode signals. The CMRR of the prototype has a constant value of 65 dB up to 50 kHz and drops to 15 dB at 10 MHz (Figure 3.5c).

3.3.4 Transient Characterization

For transient characterization propagation delay and rise-/fall times are measured by applying 500 V pulses to the probe inputs. The propagation delay t_d from 50 % input amplitude to 50 % output amplitude is 30 ns. The output rise-time t_r from 10 % output amplitude to 90 % output amplitude is calculated by correcting the measured rise time t_r' of the probe with the input signal rise time $t_{r,\mathrm{signal}}$,

$$t_r = \sqrt{t_r'^2 - t_{r,\mathrm{signal}}^2}, \tag{3.15}$$

resulting to 14 ns. Both, t_r and t_d, are equal for rising and falling edges.

3.3.5 Noise Characterization

The output noise density $e_{\mathrm{n,out}} = 63\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ is measured with a spectrum analyzer. The RMS noise $E_{\mathrm{n,out}}$ for the $-3\,\mathrm{dB}$ bandwidth of 30 MHz results in $E_{\mathrm{n,out}} = 435\,\mu\mathrm{V}$ at the output of the probe, and the RMS noise $E_{\mathrm{n,in}} = 65\,\mathrm{mV}$ referred to the input of the probe. Further, the SNR referred to full-scale is calculated with

$$\mathrm{SNR} = 20\log\left(\frac{V_{\mathrm{in,max}}}{\sqrt{2}\,E_{\mathrm{n,in}}}\right) \tag{3.16}$$

and results in 84 dBFS (dB full-scale).

3.4 Survey of the Prototype Parameters

Table 3.1: Design parameters and characterization measurement results of the high voltage differential probe prototype

		Conditions	Value	Unit
Input parameters				
Input impedance	Z_{in}	Input to ground	8 || 5.5	MΩ || pF
		Phase-to-phase	16 || 2.3	MΩ || pF
Input voltage range	V_{in}	Input to ground, safe operation	±2000	V
		Input to ground, working	±1500	V
		Phase-to-phase	±1500	V
Output parameters				
Output impedance	R_{out}		50	Ω
Output voltage swing	V_{out}	Into 1 MΩ load	±10	V
DC characteristics				
Non-linearity	$\Delta G/G_{\text{nom}}$		±80	ppm
Output offset drift	$\Delta V_0/\Delta\vartheta$	Calculated, 99.7 % confidence	±310	μV/K
Gain drift	$\Delta G/(\Delta\vartheta \cdot G_{\text{nom}})$	Calculated, 99.7 % confidence	±50	ppm/K
AC characteristics				
Bandwidth	B	−3 dB bandwidth	30	MHz
	$B_{1\,\%}$	1 % flatness	5	MHz
	$B_{0.1\,\%}$	0.1 % flatness	1	MHz
Phase	ϕ	30 MHz	-390	°
		5 MHz	-55	°
		1 MHz	-10	°
Common-mode rejection ratio	CMRR	Low frequency and dc	> 60	dB
		10 kHz	> 60	dB
		1 MHz	40	dB
Transient characteristics				
Rise-time, fall-time	t_r, t_f	10 % to 90 % of output	14	ns
Propagation delay	t_d	50 % input to 50 % output	30	ns

Continued on next page ...

Table 3.1: Design parameters and characterization measurement results of the high voltage differential probe prototype

		Conditions	Value	Unit
Noise characteristics				
Output noise	$e_{\mathrm{n,out}}$		63	$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
	$E_{\mathrm{n,out}}$	$B = 30\,\mathrm{MHz}$	435	$\mu\mathrm{V}$
Input-referred noise	$E_{\mathrm{n,in}}$	$B = 30\,\mathrm{MHz}$	65	mV
Signal-to-noise ratio	SNR		84	dBFS

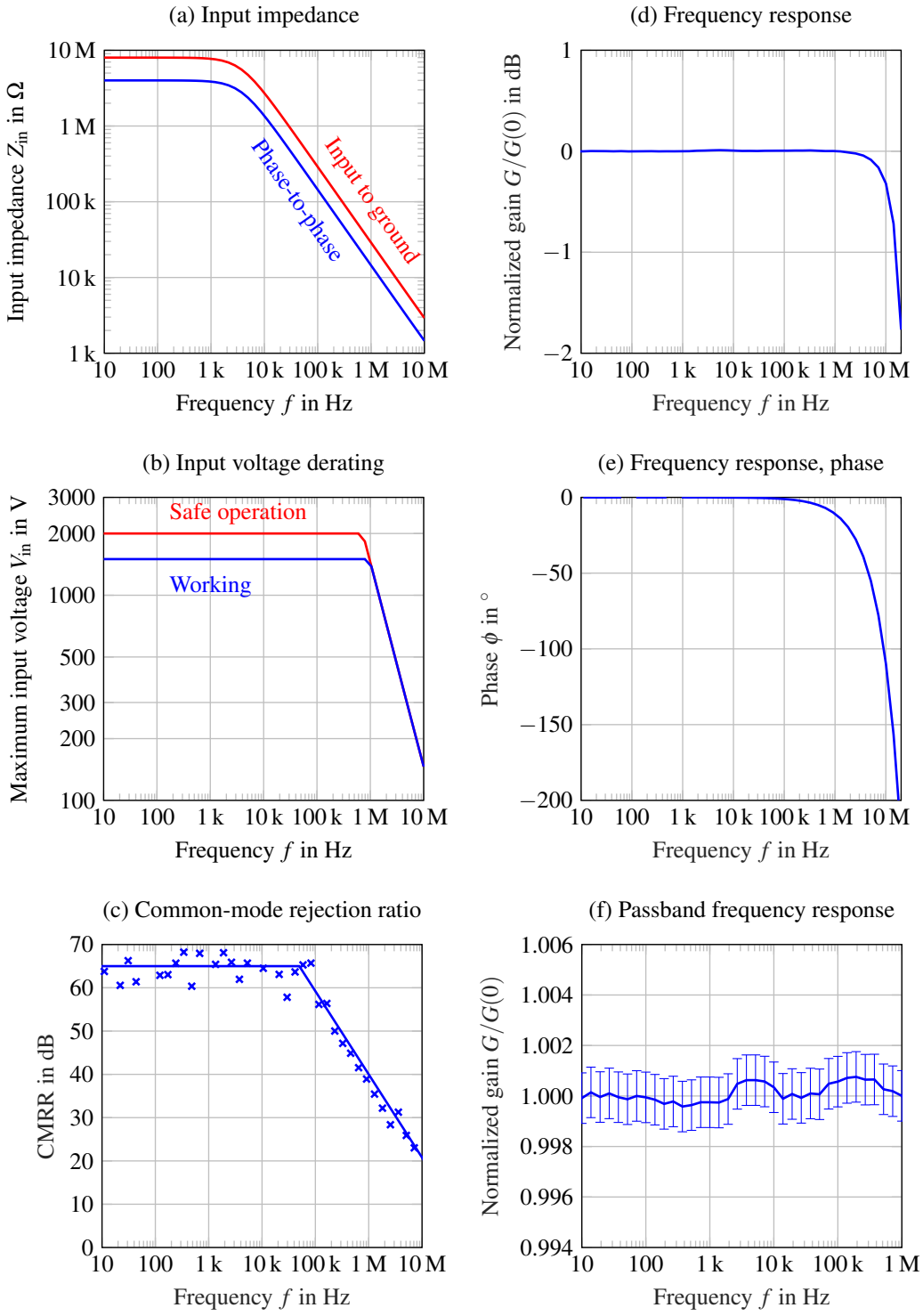


Figure 3.5: Design parameters and characterization measurement results of the high voltage differential probe prototype.

4
Digital Isolated High Voltage Probe

For some applications the use of a high voltage differential probe is not optimal. One example is the measurement of the gate-emitter voltage in power electronics. The relatively small gate control voltages are superimposed by high voltage common mode jumps. For this, the voltage probe requires a very high CMRR, which is normally not achieved with high voltage differential probes. A further example is the measurement of the inverter output voltages, whereby the inverter is already mounted in an electric vehicle. This requires an isolated measurement concept. A grounded measurement with a differential high voltage probe would cause an insulation error. In this chapter the development of a digitally isolated high voltage probe is presented. The probe continuously transmits high-resolution measurement data to a computer.

A prototype of a single-ended isolated voltage probe and first characterization results are already presented in [**GSW18**] (Attached in Appendix C). In this chapter, the individual circuit blocks are explained in more detail. Finally, some limitations of the single-ended isolated probe compared to a differential input stage probe are discussed.

4.1 Development of a Single-Ended Digital Isolated High Voltage Probe

In a digital isolated voltage probe, the digital-to-analog conversion already takes place in the probe. Thus the output signal is a digital data stream (Figure 4.1). At first the high input voltage is scaled down by the input attenuator $A(f)$. Further some analog signal conditioning $H(f)$ is necessary, before the analog-to-digital conversion is done. Output lines and input control signals of the ADC are galvanically isolated by digital isolation components. The control of the ADC and the data transmission from the ADC to a computer is done via a field-programmable gate array (FPGA). To power the galvanic isolated part of the circuit an isolated dc-dc module is used.

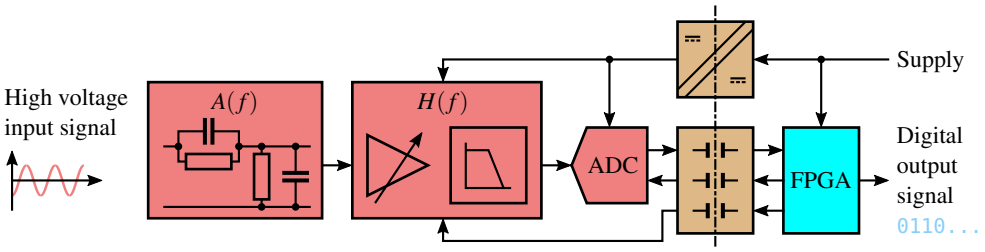


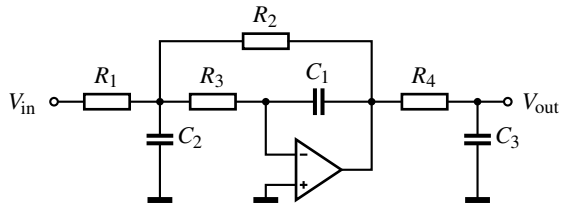
Figure 4.1: Block diagram of a digital isolated high voltage probe. The main components are an input attenuator $A(f)$, some analog signal conditioning $H(f)$, an analog-to-digital converter, and signal and supply isolation components.

4.1.1 Input Attenuator

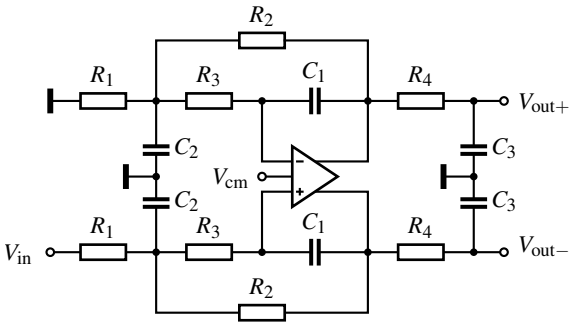
The input stage of the probe is a frequency-compensated voltage divider, based on the divider explained in Chapter 2. The divider attenuation is changed to $A = 1/750$, resulting in an output voltage swing of $\pm 2\,\mathrm{V}$ at the maximum input voltage of $\pm 1500\,\mathrm{V}$. The input impedance of the divider is $4\,\mathrm{M\Omega}||5.5\,\mathrm{pF}$. Since the reference potential of the isolated circuit part is connected to the negative input of the input divider, the reference potential of this circuit part can have a high voltage potential to ground. Thus, the conductive shielding around the divider may also have a high voltage potential and must not be touchable by the user.

4.1.2 Signal Conditioning

After the input divider, a programmable gain amplifier (PGA) is used to expand the dynamic range of the ADC. The PGA has a switchable gain of 1, 2, 5, 10 and 20, enabling additional input voltage ranges of ±750 V, ±300 V, ±150 V and ±75 V. The PGA is then followed by an active 3rd order anti-alias filter (Figure 4.2a). It is designed in multiple-feedback (MFB) topology and calculated to a Bessel filter with a −3 dB corner frequency $f_c = 1\,\text{MHz}$ and a dc gain of $K = 2$. The MFB architecture is used because it is the best architecture to be transformed to a fully differential filter circuit to connect the ADC input (Figure 4.2b) [Tex09].



(a) Single-ended input and output



(b) Single-ended input, fully differential output

Figure 4.2: Active 3rd order filter in MFB topology for anti-alias filtering. The single ended output structure (a) can easily be transformed to a fully differential filter circuit (b) to connect the ADC input.

Different aspects of filter design are covered in different textbooks and application notes. The following calculation steps and approximations are a summary for a 3rd order MFB design. The filter is a cascade of an active second order filter H_1, followed by a passive first order low pass H_2. The final transfer function of the filter can be written to

$$H(s) = H_1(s)\,H_2(s), \tag{4.1}$$

with the single transfer functions [Tex02]

$$H_1(s) = \frac{K}{\frac{1}{(2\pi f_c F_{0,1})^2} s^2 + \frac{1}{2\pi f_c F_{0,1} Q_1} s + 1} \tag{4.2}$$

$$= \frac{-\frac{R_2}{R_1}}{R_2 R_3 C_1 C_2 s^2 + \left(R_3 C_1 + R_2 C_1 \frac{R_2 R_3 C_1}{R_1} \right) s + 1}, \tag{4.3}$$

$$H_2(s) = \frac{1}{\frac{1}{2\pi f_c F_{0,2}} s + 1} = \frac{1}{R_4 C_3 s + 1}. \tag{4.4}$$

Values for the frequency scaling factors $F_{0,1}$, $F_{0,2}$ and the quality factor Q_1 are taken from filter design tables, like Table 4.1.

Table 4.1: Filter design parameters for different 3rd order active filters [Jun04, Chapter 5]

Filter	Q_1	$F_{0,1}$	$F_{0,2}$
Butterworth	1.0000	1.0000	1.0000
Bessel	0.6910	1.4524	1.3270
0.01 dB Chebyshev	1.1389	0.9642	0.8467

Since the mapping of the filter parameters $F_{0,1}$, $F_{0,2}$ and Q_1 to the components R_1 to R_4 and C_1 and C_2 comes up with several degrees of freedom, there are different ways to handle. One way to get very practical results is to select the resistor R_2 to match the feedback requirements of the op-amp and then calculate the other components according to [Jun04, Chapter 5]

$$R_1 = \frac{R_2}{K}, \tag{4.5}$$

$$R_3 = \frac{R_2}{K+1}, \tag{4.6}$$

$$C_1 = \frac{1}{4\pi F_{0,1} f_c R_2 Q_1}, \tag{4.7}$$

$$C_2 = 4 Q_1^2 (K+1) C_1. \tag{4.8}$$

Values for the passive filter at the output are chosen to meet [Jun04, Chapter 5]

$$2\pi F_{0,2} f_c = \frac{1}{R_4 C_3}. \tag{4.9}$$

As a rule of thumb the open loop gain of the op-amp should be [Jun04, Chapter 5], [MC09, Chapter 20]

$$A_{\mathrm{OL}} > (10 \sim 100) K Q_1 \tag{4.10}$$

and the gain-bandwidth product (GBW) should be [MC09, Chapter 20]

$$\mathrm{GBW} = 100 K F_{0,1} f_c \tag{4.11}$$

at minimum for filters with a quality factor $Q < 1$.

4.1.3 Analog-to-Digital Converter

The used ADC is an 18 bit successive approximation (SAR) type with 5 MS/s sampling rate. The *Analog Devices LTC2385-18* is chosen for its ±1.5 LSB integral linearity error and 95.7 dB SNR. It is also pin compatible with the *LTC2387-18* with 15 MS/s sampling rate, the fastest 18 bit ADC available on the market by February 2019. To control and readout the ADC, and transfer the ADC data to a computer, an FPGA is used. The FPGA continuously outputs the ADC data via two 100 Mb/s universal asynchronous receiver-transmitters (UARTs).

4.1.4 Isolation

Before choosing any isolation component for power or signal isolation, one has to understand the terminology for isolation ratings [Tex14]. Datasheets of isolation ICs and dc-dc modules usually advertise a very high isolation voltage at their first page. It is very important to know that this is only a transient isolation voltage, tested for 60 s (qualification testing) or 1 s (production testing), but must not be applied continuously. For that reason some manufacturers also give a value for the maximum isolation working voltage or some kind of conversion between transient isolation voltage and maximum isolation working voltage.

For isolating the voltage supply, a 1 W unregulated dc-dc module with 5 V in- and output voltage is used. The *Recom R05P05S/X2/R8* dc-dc module has a reinforced

isolation of 8 kV (tested for 1 s) and can be used at 4 kV continuos isolation [Rec17]. The added isolation impedance due to the module is 15 GΩ parallel to 10 pF.

For isolating the digital ADC in- and output lines, isolation ICs with capacitive isolation barriers are used. The *Texas Instruments ISO7820x and ISO7830x* are the only parts available on the market, combining a high data rate (100 Mb/s) with a very high maximum isolation working voltage (2000 V) and high common-mode transient immunity (±100 kV/μs). The added isolation impedance due to the isolation ICs is about 300 GΩ parallel to 3 pF.

To guarantee the high isolation barrier not only on component level but also on system level, all creepage distances between the isolated circuit parts are chosen according to [IEC07]. In addition the PCB is removed underneath the digital isolation ICs and the dc-dc module to prevent any deposition of conductive dirt or moisture.

4.2 Experimental Evaluation of a Prototype

All experiments presented in this section are done with the prototype shown in Figure 4.3. The digital output signals are sampled by a logic analyzer (*Saleae Logic Pro 16*) and further streamed to a computer via universal serial bus (USB) 3.0. Characterization results are summarized in Table 4.2 and Figure 4.4.

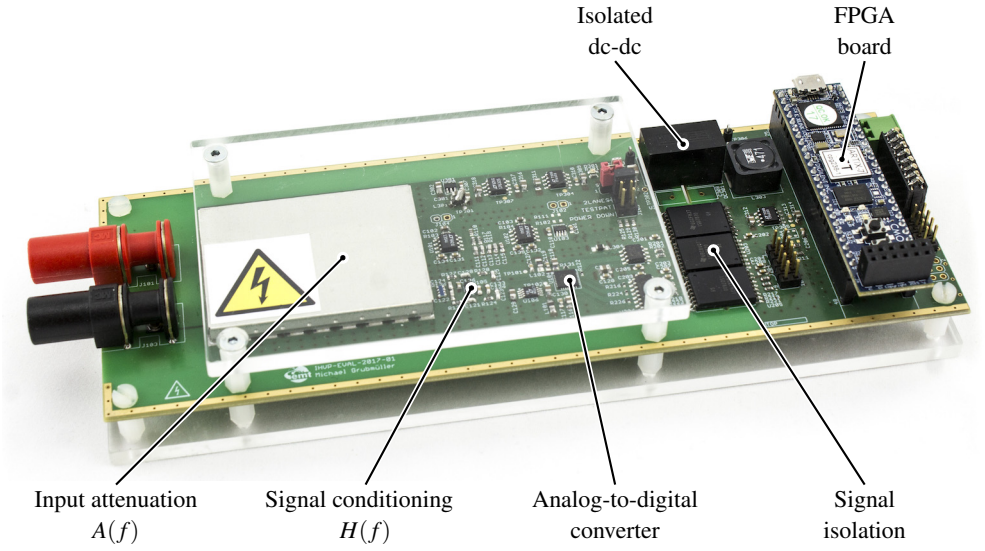


Figure 4.3: Prototype of the digital isolated high voltage probe.

4.2.1 DC Characterization

First, the nominal gain of the probe is defined by a linear least square fit of the gain for input voltages from 0 to 50 % of the FSR according to [IEE14]. Second, the nonlinearity is then expressed by the deviation of the measured gain from 0 to 100 % FSR from the nominal gain. The resulting nonlinearity for negative and positive input voltages ranging up to the FSR of ±1500 V is better than 150 ppm (Figure 4.4a).

4.2.2 AC Characterization

For ac characterization of the probe, the bandwidth, the passband frequency response flatness and the CMRR are measured. Figure 4.4c shows the Bode plot of the frequency response of the prototype compared to the simulated curve of an ideal 3rd order Bessel filter. Figure 4.4d shows the Bode plot in linear scale. It also shows the comparison of the prototype with the simulation of an ideal 3rd order Bessel filter as well as the result of a detailed circuit simulation, including parasitic behavior of the passive components and models of the used op-amps. It can be seen that the prototype has a frequency response flatness better than ±1 % and a phase lag of −15 ° up to 100 kHz. Figure 4.4e shows the resulting CMRR of the prototype. It displays a very high CMRR for low frequencies. For higher frequencies the CMRR decreases but still remains over 60 dB up to 2 MHz. The good CMRR values can only be reached by putting a conductive shield around the divider, the analog circuitry and the ADC.

4.2.3 Transient Characterization

Figure 4.4b shows the step response of the probe. It displays a symmetric behavior for falling and rising edges. Propagation delay t_d is 0.58 μs for both edges, rise and fall times t_r are 0.45 μs.

4.2.4 Noise Characterization

To measure the output noise, negative and positive input of the probe are shorted and $1 \cdot 10^6$ ADC samples d_i are taken. The RMS output noise E_{out} is then calculated by

$$E_{\text{out}} = \sigma(d_i), \tag{4.12}$$

where $\sigma(d_i)$ is the standard deviation of the ADC samples d_i. For better interpretation the input referred noise E_{rti} is calculated by

$$E_{\text{rti}} = E_{\text{out}} \cdot V_{\text{lsb}} \cdot \frac{A}{H}, \tag{4.13}$$

where V_{lsb} is the voltage of the least significant bit of the ADC, A is the attenuation of the input divider and H is the gain of the programmable gain amplifier and the fully differential amplifier. Thus the SNR expressed in dB-full-scale (dBFS) results to

$$\text{SNR} = 20 \cdot \log_{10}\left(\frac{V_{\text{in,range}}/\sqrt{2}}{E_{\text{rti}}}\right), \tag{4.14}$$

where $V_{\text{in,range}}$ is the maximum allowable input voltage of the particular input range (1500 V, 750 V, 300 V, 150 V and 75 V). Results of the measurements are shown in Table 4.2. The limited gain-bandwidth product of the PGA also decreases the bandwidth of the circuit with decreasing input voltage range (Table 4.2).

4.3 Survey of the Prototype Parameters

Table 4.2: Design parameters and characterization measurement results of the digital isolated high voltage prototype

		Conditions	Value	Unit
Input parameters				
Input impedance	Z_{in}	Phase-to-phase	$4 \,\|\|\, 5.5$	$\text{M}\Omega \,\|\|\, \text{pF}$
Input voltage range	V_{in}	Phase-to-phase, safe operation	±2000	V
		Phase-to-phase, working	±1500	V
Isolation impedance	Z_{iso}		$> 1 \,\|\|\, 13$	$\text{G}\Omega \,\|\|\, \text{pF}$
Isolation voltage	V_{isow}	Max. isolation working voltage	1500	V
Output parameters				
Sample rate	f_{s}		5	MS/s
Resolution	N		18	bit
DC characteristics				
Non-linearity	$\Delta G/G_{\text{nom}}$		±150	ppm
AC characteristics				
Bandwidth	B	−3 dB bandwidth, 1500 V range	1	MHz
		750 V range	1	MHz
		300 V range	0.9	MHz
		150 V range	0.8	MHz
		75 V range	0.6	MHz
	$B_{1\,\%}$	1 % flatness, 1500 V range	100	kHz
Phase	ϕ	1 MHz, 1500 V range	−135	°
		100 kHz, 1500 V range	−15	°
Common-mode	CMRR	Low frequency and dc	> 80	dB
rejection ratio		1 MHz	> 60	dB
Transient characteristics				
Rise-time, fall-time	t_r, t_f	10 % to 90 % of output	450	ns
Propagation delay	t_d	50 % input to 50 % output	580	ns

Continued on next page ...

Table 4.2: Design parameters and characterization measurement results of the digital isolated high voltage prototype

		Conditions	Value	Unit
Noise characteristics				
Input-referred noise	E_{rti}	1500 V range	30.5	mV
		750 V range	20.6	mV
		300 V range	15.4	mV
		150 V range	13.3	mV
		75 V range	11.3	mV
Signal-to-noise ratio	SNR	1500 V range	90.8	dBFS
		750 V range	88.2	dBFS
		300 V range	82.8	dBFS
		150 V range	78.0	dBFS
		75 V range	73.4	dBFS

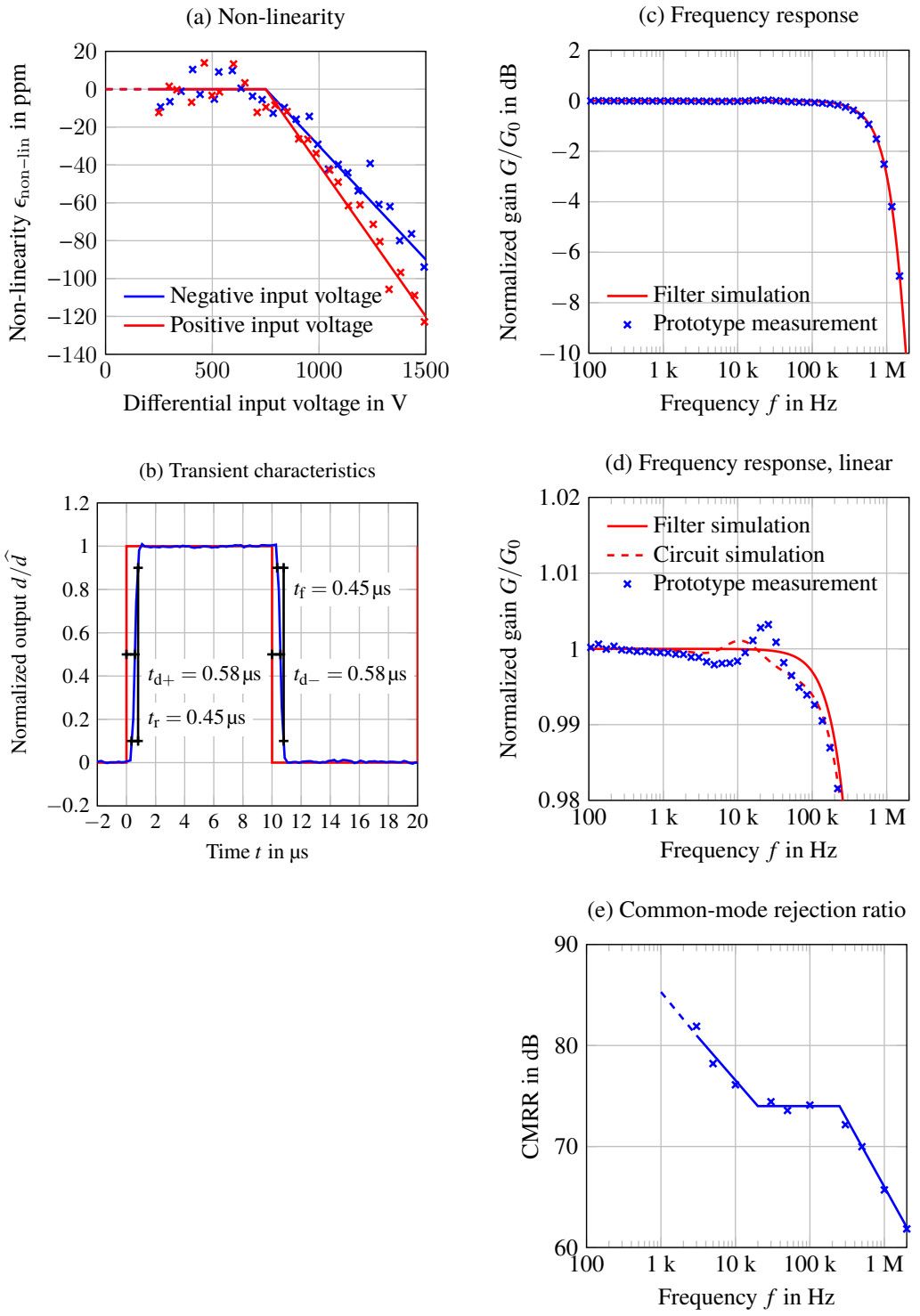


Figure 4.4: Design parameters and characterization measurement results of the digital isolated high voltage prototype [**GSW18**].

4.4 Limitation of the Single-Ended Isolated Voltage Probe

In general, a single-ended isolated voltage probe can act as a differential probe because the front-end floats referred to ground [JM18]. But in addition to the ideal probe circuit shown in Figure 1.7 from Section 1.2, in a real probe circuit a parasitic isolation capacitance C_{ISO} is formed between the floating reference potential and ground. Figure 4.5 shows the simplified circuit of a single-ended digitally isolated high voltage probe containing the parasitic isolation capacitance C_{ISO}, connected to a pure common-mode input signal.

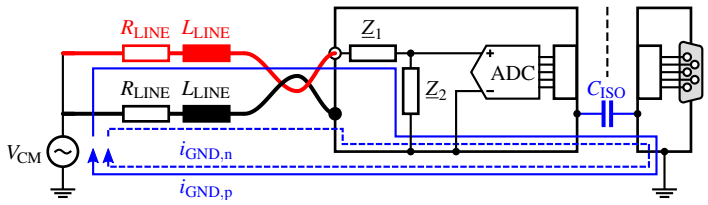


Figure 4.5: Single-ended digitally isolated high voltage probe with pure common-mode excitation V_{CM}. The isolation capacitance C_{ISO} is charged by the currents $i_{\mathrm{GND,p}}$ and $i_{\mathrm{GND,n}}$ during each voltage transition of the the common-mode input voltage V_{CM}. Since both currents pass different impedance paths, a differential input voltage is generated at the probe input terminals.

The parasitic isolation capacitance C_{ISO} has to be charged and discharged through the connection lines during each voltage transition of the the common-mode voltage V_{CM} [NBK18]. Since the current path $i_{\mathrm{GND,p}}$ for the positive input passes a different impedance (line impedance R_{LINE}, L_{LINE} - input impedance $\underline{Z}_1$, $\underline{Z}_2$ of the probe - isolation capacitance C_{ISO}) than the the current path $i_{\mathrm{GND,n}}$ for the negative input (line impedance R_{LINE}, L_{LINE} - isolation capacitance C_{ISO}), the pure common-mode excitation V_{CM} causes an erroneous differential input voltage at the probe input terminals. The erroneous differential input voltage further causes an output voltage at the probe, resulting to a decreasing CMRR. Simulations show, that the decreasing of the CMRR only starts at a few megahertz [NBK18]. The digital isolated high voltage probe explained in this chapter has a $-3\,\mathrm{dB}$ bandwidth of $1\,\mathrm{MHz}$ followed by a third order roll-off. Thus the effect of decreasing CMRR may be neglected and the probe is well suited for the measurement of high voltage inverter output signals. However when developing a probe for measuring floating low-voltage gate-emitter signals at high bandwidth, a differential front-end like explained in Chapter 3 should be used [NBK18]. Figure 4.6 shows a simplified schematic.

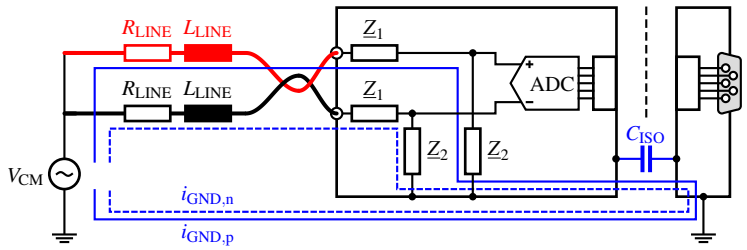


Figure 4.6: Digitally isolated high voltage probe with differential input stage. At the pure common-mode excitation V_{CM}, the isolation capacitance C_{ISO} is charged by the currents $i_{GND,p}$ and $i_{GND,n}$ during each voltage transition of the the common-mode input voltage V_{CM}. Since both currents pass equal impedance paths, no differential input voltage is generated.

By using a differential front-end, both charging currents $i_{GND,n}$ and $i_{GND,p}$ pass an equal impedance (line impedance R_{LINE}, L_{LINE} - input impedance $\underline{Z}_1$, $\underline{Z}_2$ of the probe - isolation capacitance C_{ISO}). Thus a common mode excitation V_{CM} does not cause an input differential voltage, which would lead to an erroneous output of the probe.

5

Passband Frequency Response Measurement of a Voltage Probe

The previous chapters described the development of a voltage divider and two different voltage probes. As for both of the probes a flat passband frequency response was a major design goal, the measurement of the frequency response has to be looked at in detail. This chapter presents a measurement method to evaluate the passband frequency response of a probe from dc up to 10 MHz. It introduces an oscilloscope based setup, including a calibration procedure with a reference attenuator. Amplitude and phase estimation of the oscilloscope data is done with enhanced versions of the *IEEE Standard for Digitizing Waveform Recorders* [IEE08] and *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters* [IEE11] sine-wave fit algorithms. The feasibility of the presented method is verified by an uncertainty evaluation for the complex valued frequency response.

A publication on the extension of the sine-wave fit algorithms and an alternative calculation of the uncertainty is submitted to a scientific conference [**GN19**] (Attached in Appendix D).

5.1 Measurement Method

The most common methods to measure the frequency response of a circuit are the S_{21} parameter (forward voltage gain of scattering parameter matrix) measurement with a network analyzer, or the use of an oscilloscope or voltmeter combined with a waveform generator [IEE14; Cro+17]. Due to the desired frequency range of dc to 10 MHz, the measurement with an oscilloscope is chosen for this work. The challenges with the applied method are, that oscilloscopes only have a limited dc accuracy and frequency dependent internal signal paths. To overcome these difficulties a calibration strategy with a well defined reference attenuator is introduced. Figure 5.1 shows a block diagram of the measurement setup.

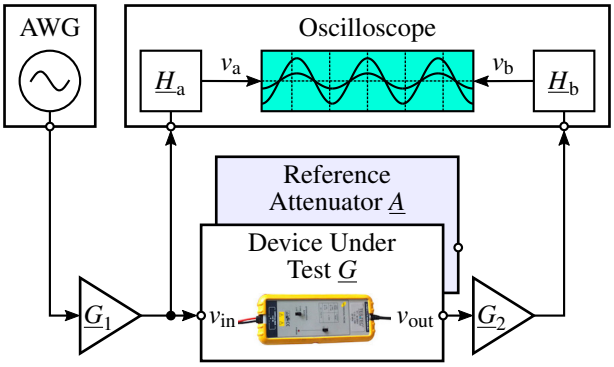


Figure 5.1: Measurement setup to obtain the frequency response of a high voltage differential probe. The measurement is first done with a reference attenuator $\underline{A}$, followed by the measurement of the device under test $\underline{G}$. [**GN19**]

The signal generator produces a sinusoidal voltage with a variable frequency f. The amplifiers $\underline{G}_1$ and $\underline{G}_2$ adjust the voltages to optimally utilize the oscilloscope. The blocks $\underline{H}_a$ and $\underline{H}_b$ model the internal signal paths of the oscilloscope. Thus the oscilloscope screen voltages v_a and v_b are not exact copies of the oscilloscope input voltages v_{in} and $v_{out} \cdot \underline{G}_2$. The resulting measurement can be expressed by

$$\underline{V}_a\big|_G = \underline{V}_{in} \cdot \underline{H}_a, \tag{5.1}$$

$$\underline{V}_b\big|_G = \underline{V}_{in} \cdot \underline{G} \cdot \underline{G}_2 \cdot \underline{H}_b, \tag{5.2}$$

$$\Rightarrow \underline{G}' = \left.\frac{\underline{V}_b}{\underline{V}_a}\right|_G = \frac{\underline{V}_{in} \cdot \underline{G} \cdot \underline{G}_2 \cdot \underline{H}_b}{\underline{V}_{in} \cdot \underline{H}_a} = \frac{\underline{G} \cdot \underline{G}_2 \cdot \underline{H}_b}{\underline{H}_a}, \tag{5.3}$$

where $\underline{G}'$ is the measurement of the frequency response $\underline{G}$, altered by $\underline{H}_a$, $\underline{H}_b$ and $\underline{G}_2$.

The voltage phasors $\underline{V}_x$ are complex values for the corresponding time domain signals v_x, where the index $x = (a, b)$ denotes the oscilloscope channel. All values are a function of the frequency f, for better readability, however, it is not specified in the formulas (e.g. $\underline{G} = \underline{G}(f)$).

Since the internal signal paths $\underline{H}_\mathrm{a}$ and $\underline{H}_\mathrm{b}$ of the oscilloscope as well as the frequency response of the amplifier $\underline{G}_2$ are unknown, the setup must be calibrated by first replacing the probe $\underline{G}$ with a reference attenuator $\underline{A}$. The reference attenuator is a resistive voltage divider, where a flat frequency response is guaranteed by the use of small valued SMD resistors. Thus, the divider can only be used for small signal calibration, but the influence of the parasitic elements can be neglected in the passband in contrast to the high resistance input stage of the high voltage differential probe. The resulting ac characteristic of the reference attenuator $\underline{A}_\mathrm{ac} = \underline{A}(f)/A(f = 0)$ is incorporated from a circuit analysis. The dc ratio $A_\mathrm{dc} = A(f = 0)$ is obtained by a dc ratio measurement with a multimeter. In the following, the frequency response of the reference attenuator is expressed by $\underline{A} = A_\mathrm{dc} \cdot \underline{A}_\mathrm{ac}$ and the calibration measurement is modeled by

$$\underline{V}_\mathrm{a}\big|_A = \underline{V}_\mathrm{in} \cdot \underline{H}_\mathrm{a}, \tag{5.4}$$

$$\underline{V}_\mathrm{b}\big|_A = \underline{V}_\mathrm{in} \cdot \underline{A} \cdot \underline{G}_2 \cdot \underline{H}_\mathrm{b}, \tag{5.5}$$

$$\Rightarrow \underline{A}' = \left.\frac{\underline{V}_\mathrm{b}}{\underline{V}_\mathrm{a}}\right|_A = \frac{\underline{A} \cdot \underline{G}_2 \cdot \underline{H}_\mathrm{b}}{\underline{H}_\mathrm{a}} = \frac{\underline{A}_\mathrm{ac} \cdot A_\mathrm{dc} \cdot \underline{G}_2 \cdot \underline{H}_\mathrm{b}}{\underline{H}_\mathrm{a}}. \tag{5.6}$$

Finally (5.3) and (5.4) are combined and the measurement result can be expressed in two different ways

$$\mathrm{I}: \quad \underline{G} = \left.\frac{\underline{V}_\mathrm{b}}{\underline{V}_\mathrm{a}}\right|_G \cdot \left.\frac{\underline{V}_\mathrm{a}}{\underline{V}_\mathrm{b}}\right|_A \cdot \underline{A}_\mathrm{ac} \cdot A_\mathrm{dc}, \tag{5.7}$$

$$\mathrm{II}: \quad \underline{G} = \frac{\underline{G}' \cdot \underline{A}_\mathrm{ac} \cdot A_\mathrm{dc}}{\underline{A}'}. \tag{5.8}$$

It can be seen that the introduction of a calibration measurement with a reference attenuator effectively compensates the internal signal paths $\underline{H}_\mathrm{a}$ and $\underline{H}_\mathrm{b}$ of the oscilloscope as well as the influence of amplifier $\underline{G}_2$.

Since oscilloscope measurements are time domain measurements, but a frequency transfer function is of interest, a transformation of the data is necessary. Therefore the *IEEE Standards 1057* [IEE08] and *1251* [IEE11] suggest the use of least square

sine-wave fit algorithms. For the algorithms the time domain measurements for input and output are modeled by

$$v_x(t) = V_x \cos(2\pi f t + \phi_x) + V_{x,0} + w(t), \tag{5.9}$$

where $w(t)$ represents an additive white Gaussian measurement noise. The standards deliver a three- (known frequency) and a four-parameter (unknown frequency) algorithm to determine amplitude V_x, phase ϕ_x and an additional offset $V_{x,0}$ of the sinusoidal signal. The three-parameter algorithm can be realized with matrix operations only, resulting in very low computation complexity. The four-parameter algorithm is an iterative algorithm that also estimates the signal frequency f. If the frequency is known with an accuracy limit better than [Hän00]

$$\Delta f < \frac{1}{2\pi}\sqrt{\frac{12}{\mathrm{SNR}\, N_s^3}}, \tag{5.10}$$

the three-parameter algorithm should be used. N_s denotes the number of samples. The SNR for sinusoidal signals is defined by

$$\mathrm{SNR} = \frac{V_x^2}{2\sigma_w^2}, \tag{5.11}$$

where σ_w the is standard deviation of the measurement noise w. With the introduced setup it is not possible to generate signals with a frequency accuracy better than the stated bound Δf. So the four-parameter algorithm has to be used. However, input and output signal are measured simultaneously and the device under test is a linear time-invariant (LTI) system. So it is not necessary to estimate the frequency for input and output separately. For this kind of application, the three- and four-parameter algorithms can be extended to a seven-parameter algorithm [RS08; Hän08]. In the case of a high voltage differential probe, where there is a big ratio between input and output amplitude, a four-parameter algorithm applied to the data with the higher amplitude, followed by a three-parameter algorithm on the low amplitude data delivers results with same quality compared to the seven-parameter estimator [RS08]. Further, the number of samples N_s is chosen large enough that the permanent amplitude error $\epsilon(V_x)$ of [Ale09; Hän10]

$$\epsilon(V_x) = \frac{1}{2\, N_s\, \mathrm{SNR}} \tag{5.12}$$

can be neglected.

For the four-parameter algorithm, also the choice of the initial frequency estimation is critical to the correct frequency estimation [SS03]. The IEEE standards suggest a discrete Fourier transform (DFT)-based calculation or a time measurement between zero crossings. In the proper case, the best initial estimate is the preset arbitrary waveform generator (AWG) output frequency. Thus a very good starting value can be given without any computation. Furthermore, the IEEE standards suggest a fixed number of six iterations for the four-parameter algorithm. This should be appropriate for most applications, but could be a waist of calculation time for applications with very good first estimates. Thus, the stop condition [Bil+04]

$$\frac{\Delta f_i}{f_i} < \frac{\sqrt{2}}{\pi\, 2^{N_b+2}} \tag{5.13}$$

is used, where Δf_i and f_i are the frequency correction term and the frequency estimate of the i-th iteration of the algorithm. N_b is the number of bits of the used oscilloscope.

The oscilloscope used for the measurements is a *Picoscope 5444B* USB oscilloscope with integrated AWG. Oscilloscope measurements are done with $N_b = 15\,\text{bit}$ resolution and $N_s = 4096$ samples. The sampling rate f_s is adjusted so that at least five signal periods are sampled. The multimeter for the dc measurement of the reference attenuator is a *Tektronix/Keithley 2100* $6^1/_2$ - digit desk multimeter.

5.2 Uncertainty of the Proposed Method

Reporting a frequency response is commonly done in polar form by providing a Bode plot with magnitude and phase. The standard tool for calculating the uncertainty of a measurement is the GUM [JCG08]. But if the GUM is applied on polar form measurements, some problems caused by the scales of magnitude and phase may occur [RS02].. The magnitude has a lower bound of zero and the phase has cyclical scale from $-\pi$ to π. A calculation completely in polar form should be admissible, if the measurement input and output hold some constraints. That means that the measurand is far from the origin, meaning

$$G \,/\, u(G) \gg 1 \tag{5.14}$$

and all phase measurements are “unwrapped”, so that there are no phase jumps from $-\pi$ to π. If this cannot be guaranteed uncertainty calculations have to be done in rectangular form and further use of the GUM Supplement 2 (GUM-S2) [JCG11].

[**GN19**] shows a comparison of both methods for the underlying measurement task and validates the use of the polar form calculation.

5.2.1 Uncertainty Calculation with the GUM Uncertainty Framework

Figure 5.2a and Figure 5.2b show measurements of the voltages V_a and V_b of the reference attenuator at a signal frequency $f = 1\,\mathrm{kHz}$ over time. Some recalibration artifacts can be seen in the magnitude data, especially during warm-up. The artifacts occur on both channels simultaneously. A correlation analysis shows that the voltage signals are highly correlated. Thus a correlation term has to be considered to calculate the combined uncertainty, when using expression (5.7) as measurement model. This is not required when using the latter expression (5.8), which only contains the resulting ratio measurements $\underline{G}'$ and $\underline{A}'$. An exemplary ratio measurement $\underline{A}'$ is shown in Figure 5.2c. The data does not contain calibration artifacts any more. After a warm-up time of half an hour the drift of the measured magnitude ends and the measurement data can be considered normally distributed (Figure 5.2d).

Numerical analysis of the measurement data also shows only weak correlation between magnitude and phase. So expression (5.8) can be split into two completely independent measurement problems, one for the magnitude

$$y_1 = G = \frac{G' \cdot A_{\mathrm{ac}} \cdot A_{\mathrm{dc}}}{A'} \tag{5.15}$$

and a second one for the phase

$$y_2 = \phi = \phi(G') + \phi(A_{\mathrm{ac}}) - \phi(A')\,. \tag{5.16}$$

The corresponding input uncertainties are summarized by their covariance matrices

$$\boldsymbol{V_{x,1}} = \mathrm{diag}\left[u^2(G') \quad u^2(A_{\mathrm{ac}}) \quad u^2(A_{\mathrm{dc}}) \quad u^2(A')\right], \tag{5.17}$$

$$\boldsymbol{V_{x,2}} = \mathrm{diag}\left[u^2(\phi(G')) \quad u^2(\phi(A_{\mathrm{ac}})) \quad u^2(\phi(A'))\right]. \tag{5.18}$$

According to the GUM, uncertainties are divided into Type A and Type B uncertainties. Type A uncertainties are evaluated by *statistical analysis of series of observations* (i.e. repeated measurements), and Type B uncertainties are evaluated by *other than the statistical analysis of series of observations* (e.g. datasheet parameters of instruments) [JCG08]. All Type A uncertainties $u(G')$, $u(\phi(G'))$, $u(A')$ and

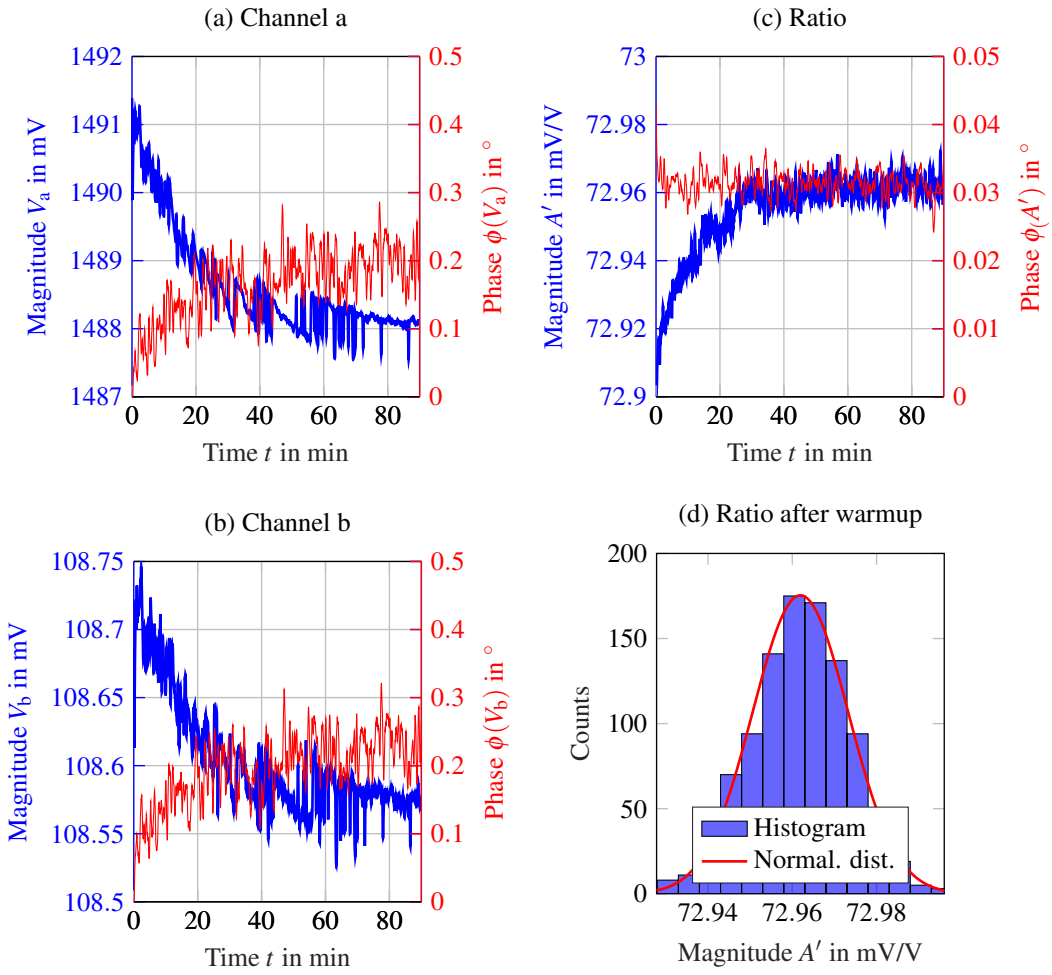


Figure 5.2: Input (a) and output (b) voltage measurement of the reference attenuator at $f = 1\,\text{kHz}$ over time. The magnitude of the voltages show some recalibration artifacts. The resulting ratio (c) does not show the calibration artifacts but still has a remaining warm-up time with drifting magnitude. After the warm-up the ratio is normally distributed (d). [**GN19**]

$u(\phi(A'))$ are defined by their *experimental standard deviation of the mean*. The dc ratio measurement and the ac frequency response flatness uncertainties of the reference attenuator are Type B uncertainties. Values for the dc ratio are taken from the multimeter datasheet. The datasheet values for "accuracy" are treated as worst case values $a(A_{dc})$ with uniform distribution in-between, leading to $u(A_{dc})$=$a(A_{dc})/\sqrt{3}$. The uncertainty evaluation of the frequency response flatness of the reference attenuator is performed with a worst-case circuit analysis. The values are supposed uniform distributed between the worst case simulation output, leading to $u(A_{ac}) = a(A_{ac})/\sqrt{3}$

and $u(\phi(A_{\mathrm{ac}})) = a(\phi(A_{\mathrm{ac}}))/\sqrt{3}$. The output uncertainties are then calculated by the *law of propagation of uncertainties*

$$u(y_1) = u(G) = \sqrt{\boldsymbol{C_1}\,\boldsymbol{V_{x,1}}\,\boldsymbol{C_1}^{\mathrm{T}}}, \tag{5.19}$$

$$u(y_2) = u(\phi) = \sqrt{\boldsymbol{C_2}\,\boldsymbol{V_{x,2}}\,\boldsymbol{C_2}^{\mathrm{T}}}, \tag{5.20}$$

where the vectors

$$\boldsymbol{C_1} = \left[\frac{\partial G}{\partial G'} \quad \frac{\partial G}{\partial A_{\mathrm{ac}}} \quad \frac{\partial G}{\partial A_{\mathrm{dc}}} \quad \frac{\partial G}{\partial A'}\right], \tag{5.21}$$

$$\boldsymbol{C_2} = \left[\frac{\partial \phi}{\partial \phi(G')} \quad \frac{\partial \phi}{\partial \phi(A_{\mathrm{ac}})} \quad \frac{\partial \phi}{\partial \phi(A')}\right], \tag{5.22}$$

contain the sensitivity coefficients. To calculate the coverage factor for an expanded uncertainty [Hal15; Hal16]

$$k_{\mathrm{polar},p} = t_\nu(\sqrt{p}) \tag{5.23}$$

has to be used, where t_ν is the $100\sqrt{p}$-th percentile of the Student t-distribution with ν degrees of freedom. Thus the coverage probability of the two parameter problem is the product of the individual interval coverage probabilities, known from the GUM. The degrees of freedom are calculated with the *Welch-Satterthwaite formula* [JCG08, Annex G.4]

$$\nu = \frac{u^4(y)}{\sum \dfrac{c_i^4(x)\,u_i^4(x)}{\nu_i}}, \tag{5.24}$$

where c_i are the single sensitivity coefficients out of $\boldsymbol{C_1}$ and $\boldsymbol{C_2}$, and ν_i are the degrees of freedom of the measurements. For Type A uncertainties ν is typically defined by the number of measurements decreased by one. For Type B measurements it can be set to infinity.

5.2.2 Resulting Uncertainty

Figure 5.3 shows the frequency response measurements G', A', the reference attenuator flatness A_{ac} and the resulting frequency response G of the probe (top), and the corresponding measurement uncertainties (bottom). Curves of the measurements are normalized to their dc value for better comparison. It can be seen that the measured frequency response G' differs more than 1 % from the frequency response G of the

probe at 100 kHz due to the internal signal paths of the oscilloscope. This approves the importance of the calibration measurement with the reference attenuator.

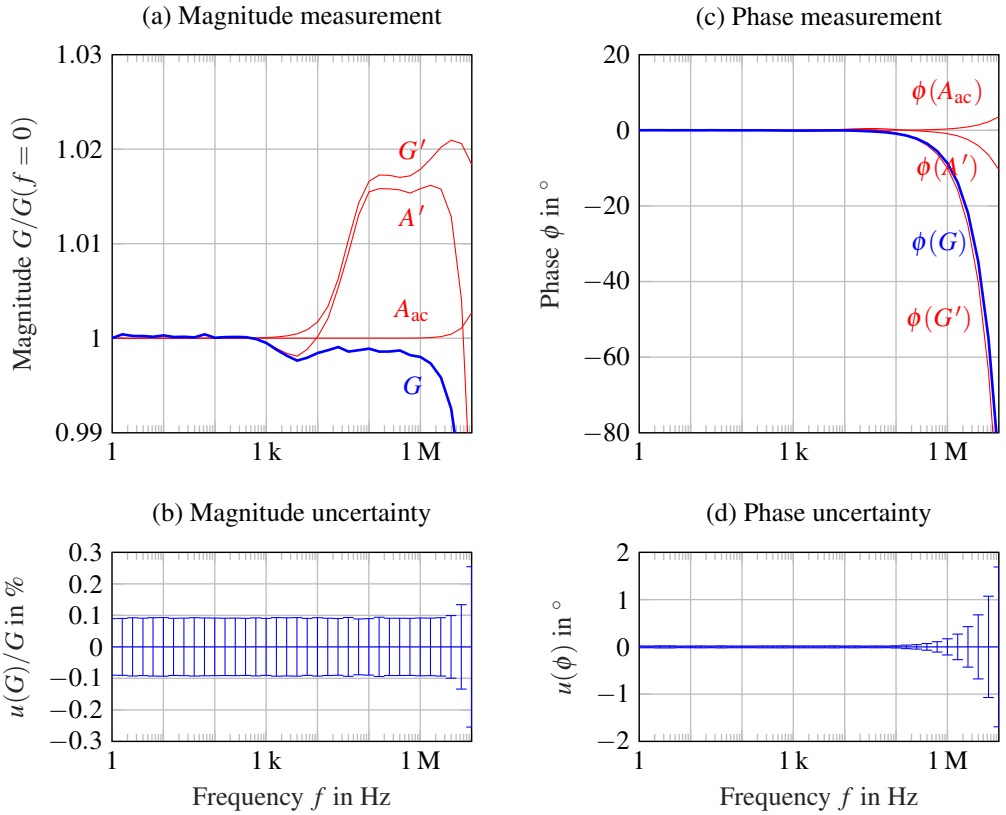


Figure 5.3: Magnitude and phase of frequency response of the measurements of $\underline{G}'$, $\underline{A}'$, $\underline{A}_{ac}$ and the result $\underline{G}$ (top). The uncertainty is calculated for a 95 % confidence interval and $M = 100$ measurements. [**GN19**]

Tab. 5.1 compares the uncertainty for $M = 10$ and $M = 100$ measurements. Further it shows the uncertainty budget by listing the coefficients of contribution h. The coefficient of contribution h quantifies the degree of contribution of an input uncertainty to the combined uncertainty [KKB06]. Coefficients of contribution greater than 30 % are marked in bold red. It can be observed that for frequencies below 1 MHz the Type B uncertainty of the A_{dc} measurement dominates. At higher frequencies the Type B uncertainty of A_{ac} dominates for high number of measurements. For a lower number of measurements the Type A uncertainty of the G' measurement also gets relevant.

As a summary it can be stated that the resulting uncertainty is below 0.1 % for magnitude and smaller than 0.2 ° for phase up to 1 MHz for 100 measurements. The

magnitude uncertainty drops to 0.15 % for the smaller number of 10 measurements. Since the Type B uncertainties of the multimeter for determining the dc ratio of the reference attenuator has a major contribution, the combined uncertainty may be decreased by using a better multimeter.

Table 5.1: Measurement result and uncertainty budget [**GN19**]

			Uncertainty		Uncertainty budget for G				Uncertainty budget for ϕ		
f	G	ϕ	$\frac{u(G)}{G}$	$u(\phi)$	$h(G')$	$h(A_{ac})$	$h(A_{dc})$	$h(A')$	$h(G')$	$h(A_{ac})$	$h(A')$
Hz	mV/V	°	%	°	%	%	%	%	%	%	%
$M = 10$											
1 k	6.667	-0.093	0.12	0.073	**47.9**	0.0	**51.0**	1.1	**99.0**	0.0	1.0
10 k	6.668	-0.055	0.12	0.077	**42.1**	0.0	**57.1**	0.9	**99.1**	0.1	0.8
100 k	6.664	-0.833	0.15	0.060	**62.3**	0.0	**37.3**	0.4	**88.7**	10.7	0.6
1 M	6.668	-8.662	0.14	0.177	**57.2**	0.0	**42.0**	0.8	7.3	**92.7**	0.1
10 M	6.438	-87.949	0.28	1.692	15.0	**75.8**	9.1	0.1	0.2	**99.8**	0.0
$M = 100$											
1 k	6.668	-0.075	0.09	0.020	10.8	0.0	**89.0**	0.1	**99.1**	0.0	0.9
10 k	6.660	-0.048	0.09	0.019	15.0	0.0	**84.8**	0.2	**98.3**	0.8	0.9
100 k	6.664	-0.833	0.09	0.023	9.2	0.0	**90.7**	0.1	**45.8**	**53.7**	0.6
1 M	6.658	-8.711	0.09	0.171	13.5	0.1	**86.3**	0.1	1.3	**98.7**	0.0
10 M	6.439	-87.972	0.26	1.690	2.3	**87.2**	10.5	0.0	0.0	**100.0**	0.0

6

Summary

In modern power electronics, voltage levels may exceed several hundreds of volts. Thus a probe is needed to connect a low voltage measurement instrument, like an oscilloscope or a transient recorder, to a power electronics circuit for measurements. Since power electronics use fast-switching pulse-width modulation (PWM) techniques, the probe not only has to simply scale down the high voltage, but also needs sufficient bandwidth, good frequency response flatness and a low phase lag. State of the art probes and related research is shown at the beginning of this thesis (Chapter 1). For single-ended, ground related measurements the well known passive oscilloscope probe should be used. A variety of well developed passive oscilloscope probes for different input voltages and bandwidths have been available for decades. For measuring input and output voltages of an inverter, however, floating measurements are necessary. This can only be done by differential probes or isolated probes. Various evaluation measurements on commercially available high voltage differential probes showed insufficient performance. The flatness of the frequency response below 100 kHz already shows a deviation of more than 1 %. The linearity of the probes is also worse than 0.1 % at the maximum input voltage. Related research and products of digitally isolated probes achieve very promising common-mode rejection ratio (CMRR) and high isolation barriers greater than 1 MV, but provide only a short term blocked data transmission and low 8 bit resolution. The block data can be used for

fast transient analysis, but long-term power measurements on the power electronics are not possible.

The main output of this thesis is the design and characterization of a high voltage differential probe for high-precision measurements (Chapter 3) and a digital isolated high voltage probe with continuous 18 bit, 5 MS/s measurement data transfer (Chapter 4). Therefor the first step was to design a voltage divider that can be used as an input stage for the high voltage differential probe and the digitally isolated probe. The voltage divider is designed for good passband frequency response flatness and high linearity. For the voltage divider design process, a reliable simulation framework was necessary. The simulation framework was achieved by an in-depth analysis of the frequency dependency of passive components and the printed circuit board (PCB) itself (Chapter 2). Model parameters for the simulation were initially gained from datasheet values, literature and geometry constraints. For the final simulation framework, however, detailed verification measurements and a further adjustment of the parameters were necessary. As a result, the differential probe and the digitally isolated probe, reach very good parameters, but differ in some areas such as bandwidth, CMRR and impedance to ground. Thus each probe is suited for a different measurement task.

For the high voltage differential probe, high bandwidth (30 MHz), good frequency response flatness (0.1 % up to 1 MHz) and good linearity (±80 ppm at the maximum differential input voltage of ±1500 V) could be reached. Since the standard approach of using a network analyzer to evaluate the frequency response does not correspond to the required frequency range and uncertainty, an alternative setup with a high-resolution oscilloscope was introduced. The suitability of this setup was proven by an uncertainty assessment according to the Guide to the Expression of Uncertainty in Measurement (GUM) (Chapter 5). The analog output of the high voltage differential probe makes it well suited for oscilloscope measurements of high-rise-time inverter output signals. The CMRR of the differential probe of better than 60 dB at dc and low frequency is good but still limited by the imperfect matching of the two input dividers, especially for increasing frequencies (40 dB at 1 MHz).

The isolated probe has a high impedance referred to ground (> 1 GΩ parallel to 13 pF) and a higher CMRR (> 80 dB at dc and low frequency) than differential probes. So it is well suited for accurate power measurements of electric drives. It is also the preferred probe when high insulation is critical. The CMRR is still limited and decreases with increasing frequencies (60 dB at the −3 dB bandwidth of 1 MHz). This effect can be explained by the insulation impedances, mainly capacitances, of

the isolation components for data transmission and power supply. Since high-speed fiber optic components and connectors are currently becoming cheaper, fiber optic data transmission could be an interesting alternative for further development. With regard to power isolation, a battery-powered front-end could be considered.

A

Characterization of a Resistive Voltage Divider Design for Wideband Power Measurements

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Characterization of a Resistive Voltage Divider Design for Wideband Power Measurements

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***Abstract*—Due to the continuing trend towards electrification of vehicles, the exact determination of the electrical efficiency is of increasing importance. This requires accurate current and voltage measurements. In this paper we present our research on a resistive voltage divider design for wideband power measurements. The divider covers voltages up to 1 kV and a frequency range from DC to 10 MHz. The parasitic behavior of the resistors and the layout are discussed in detail. Furthermore we present an exemplary implementation of a 100:1 voltage divider, including capacitive compensation and shielding.**

I. Introduction

State of the art electric drives reach a very high efficiency. Thus, high accuracy power measurements are necessary for efficiency optimization. Typical drives consist of an AC motor, driven by a PWM (Pulse Width Modulation) voltage. The broad spectra of the PWM voltage [1] in combination with the motor and cable impedance [2] result in high voltage steps with high frequency oscillations (see Fig. 1).

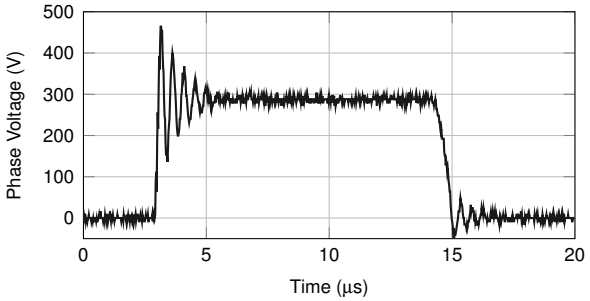

Fig. 1. Single PWM pulse of a typical voltage signal at an electric motor terminal in a vehicle application.

Typically high voltage differential active probes are used for measuring such voltage signals. The major disadvantage of this probes is that their accuracy is only specified for DC and low frequency. None of the manufacturers guaranty any accuracy behavior accounting the frequency. This leads us to work on an own voltage probe which has a predictable behavior over a high bandwidth (several MHz).

The common way to scale down a voltage is a simple resistive divider. This absolutely suits for DC and low frequency applications. For frequencies above a few kHz the parasitic behavior of the resistors and the PCB (Printed Circuit Board) must be considered. The National Measurement Institute Australia [3] and the Swedish National Testing and Research Institute [4] already discussed this issue and presented two voltage dividers in their publications. Their designs are quite sophisticated, but the specifications do not meet the requirements for measuring voltages in the electrified vehicle powertrain, due to their frequency limitations. Our investigation leads to a 100:1 (40 dB attenuation) voltage divider with a very flat frequency response up to 10 MHz. The voltage divider is built with SMD (Surface Mount Device) components and contains capacative compensation and shielding.

II. Design Considerations

When working with high frequencies (starting at a few hundred kHz) parasitic effects have to be considered. In this work we use an equivalent circuit for a resistive voltage divider which accounts the parasitic elements of the resistors and the PCB. The obtained circuit is used for simulations to support the design process of the implemented divider.

A. Resistor Parasitics

Fig. 2 shows the standard lumped circuit model of a resistor.

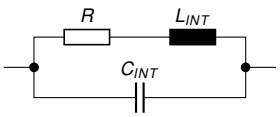

Fig. 2. Lumped circuit model of a resistor. R represents the nominal resistor; L_{INT} the internal inductance; C_{INT} the internal shunt capacitance.

For low frequencies the reactance of the internal inductance is nearly zero and the reactance of the internal shunt capacitance is very high. As a result the impedance of the whole circuit is nearly equal to the nominal resistor. For increasing frequencies the internal inductance starts increasing the impedance of the circuit; the internal shunt capacitance starts decreasing the impedance of the circuit. Which one of the two effects will dominate, depends on the nominal value of the resistor:

- For high-value resistors, the internal shunt capacitance will dominate at high frequencies.
- For low-value resistors, the internal inductance will dominate at high frequencies.

For further work this statement has to be expressed by concrete values. In [5], first published in the 1980s, some very conservative values for leaded resistors are given; [6] gives some more up-to-date values for thin film SMD resistors. Fig. 3 shows the regions where the impedance of a resistor is within ± 100 ppm of its nominal value. One can see that for resistors greater than a few kilo ohm, the internal shunt capacitance will dominate at high frequencies. To reach a high input impedance for the voltage divider, only resistors higher than a few kilo ohm will be used. Due to that limitation, the internal inductance may be neglected for all further investigations.

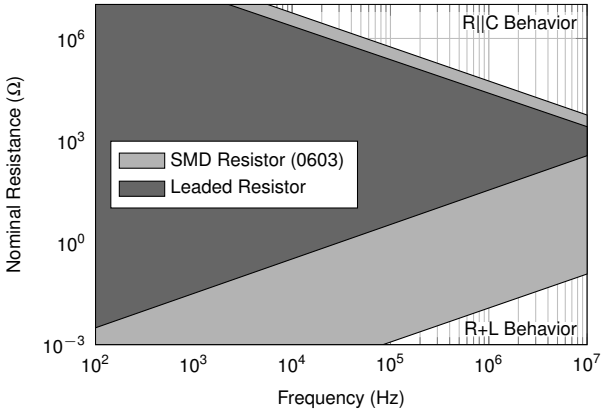

Fig. 3. Regions where the impedance of a resistor is within ± 100 ppm of its nominal resistance value (based on values of [5] and [6]). Outside this regions the parasitic behavior starts dominating.

Table I lists some measured values of the internal shunt capacitance for different resistor packages. The measurement was done with a simple voltage and current measurement at 10 MHz. An additional measurement of the nominal resistance R is done with a multimeter; the final calculation of C_{INT} is shown in (1) and (2).

$$Y = \frac{1}{Z} = \frac{I}{U} \quad \text{and} \quad Y^2 = \left(\frac{1}{R}\right)^2 + (\omega\, C_{\text{INT}})^2 \tag{1}$$

$$\Longrightarrow C_{\text{INT}} = \frac{\sqrt{\left(\frac{I}{U}\right)^2 - \left(\frac{1}{R}\right)^2}}{\omega} \tag{2}$$

B. Layout Parasitics

By assembling the resistors on a PCB, two further parasitic capacitors have to be considered: the stray capacitance C_{GND}, from each solder pad to ground; C_{PAD}, which is between the two solder pads to mount the resistor. It is not possible to calculate values for C_{GND} and C_{PAD} analytically in a simple way. This leads us to the use of FEM (Finite Element Method) simulation.

For PCBs with a ground plane, the stray capacitance C_{GND} may be calculated like a simple plate capacitor. To keep C_{GND} as low as possible, there is no ground plane under and around the voltage divider. Due to that C_{GND} of the voltage divider only depends on the distance from the resistor pads to other

TABLE I
MEASURED INTERNAL SHUNT CAPACITANCE OF DIFFERENT RESISTOR PACKAGE TYPES AND SIZES

Type	Size	C_{INT} (fF)
SMD	0402	37
	0603	46
	0805	58
	1206	60
MELF	0204	85
	0207	107
Leaded	Ø = 3.5 mm, l = 19 mm	85
	Ø = 8 mm, l = 54 mm	70
High Voltage Divider	l = 38 mm	97

conductors which have GND potential. This conductor may also be the user who operates the probe, or the desk on which the probe is placed. Thus the surrounding influences C_{GND} very strong. To get a constant capacitance C_{GND}, a shield around the voltage divider is necessary. We put a thin brass pipe with an diameter of 2 cm around the divider (see Fig. 4). For this geometry we get a capacitance of 150 fF between the resistors solder pad and ground from the FEM simulation.

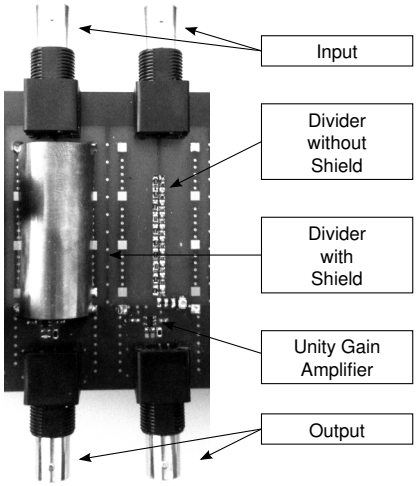

Fig. 4. Picture of the testboard for developing the voltage divider; one with a shield (left), another with removed shield (right).

The pad capacitance C_{PAD} depends on the pad geometry and the gap between them. We found out that $C_{\text{PAD}} = C_{\text{INT}}$ is a good approximation for SMD pads on single-sided PCBs without ground plane near the resistor pads. For leaded resistors C_{PAD} may be neglected, due to the big distance between the two pads.

C. Amplifier

To avoid loading the divider output and for driving a coax cable, a unity gain amplifier is attached at the dividers output. The amplifiers input impedance R_{AMP} and C_{AMP} is parallel to the dividers output. Thus the amplifier input impedance has to be considered. Values are provided in the amplifiers datasheet.

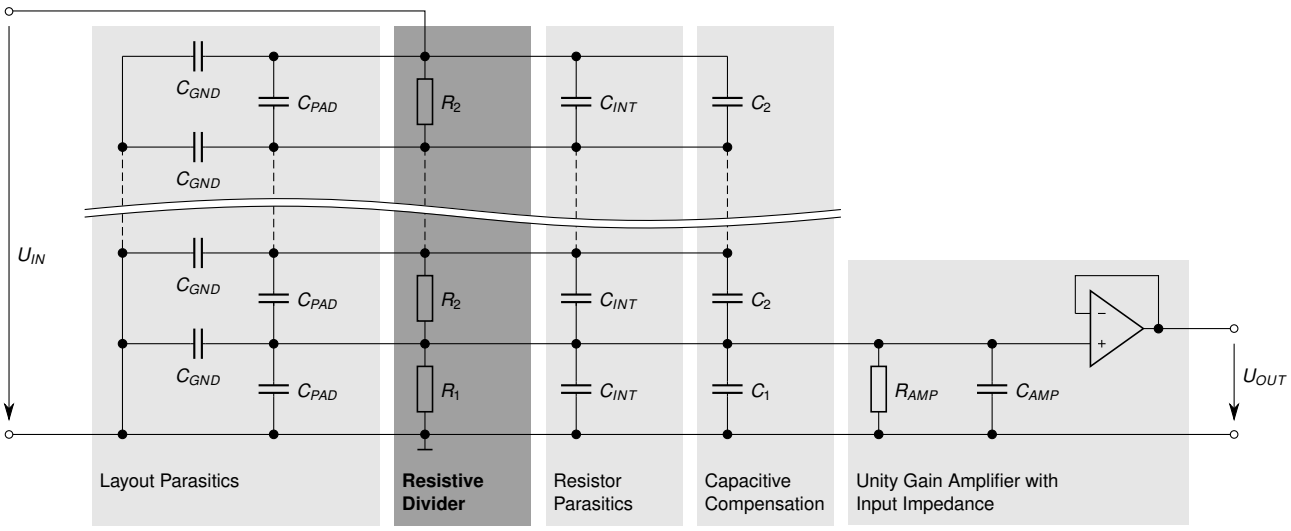

Fig. 5. Circuit diagram of the implemented voltage divider with all considered parasitic elements.

D. Capacitive Compensation

Fig. 5 shows the circuit diagram of the implemented voltage divider with all considered parasitic elements.

To minimize the influence due to variations and instability of the parasitic components C_{INT} and C_{PAD}, even bigger capacitors C_2 (at least 100 times C_{PAD} + C_{INT}) are connected parallel to the resistors R_2. At low frequencies the output voltage is defined by the resistors. At high frequencies the output voltage is defined by the parasitic elements and the capacitors C_2. To reach the same input to output ratio for a wide frequency range, capacitive compensation is necessary. Therefor the capacitor C_1 has to be added. For a first approach (3) has to be achieved.

$$\frac{R_2}{R_1} \approx \frac{C_1 + C_{\text{INT}} + C_{\text{PAD}} + C_{\text{AMP}}}{C_2 + C_{\text{INT}} + C_{\text{PAD}}} \tag{3}$$

In (3) the amplifier input resistance R_{AMP} and the stray capacitance C_{GND} is neglected. Because of the high value of R_{AMP} it is not necessary to take it into account. Nevertheless C_{GND} has to be considered. This can not be done analytically in a simple way; an approach is shown in [7]. We make a nodal analysis of the whole divider to calculate the desired value for C_1. The nodal analysis is iterated for different values of C_1 until the output to input ratio at a specified high frequency is equal to the output to input ratio at DC.

III. Hardware Characterization

All measurements shown in this paper are done with the shielded divider shown in Fig. 4. The main resistive divider consists of a single resistor R_1 in the lower brunch and a chain of 10 resistors R_2 in the upper brunch.

A. Measurement Setup

Fig. 6 shows the test setup to measure the frequency behavior of a voltage divider or probe.

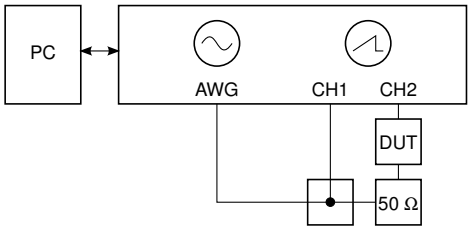

Fig. 6. Measurement setup for attenuation measurement of a DUT (Device Under Test) over frequency.

We use an USB oscilloscope with an integrated AWG (Arbitrary Function Generator). The oscilloscope has a 15 bit resolution and a sampling rate of 125 MS/s. The control of the AWG and the readout of the oscilloscope is done with a PC. The following measurement procedure is repeated for 40 frequencies in the range of 25 Hz to 10 MHz:

1) Output a sinusoidal signal with defined frequency
2) Sample input and output voltage of the voltage divider for an integer number of sine waves
3) Compute the DFT (Discrete Fourier Transformation) of input and output signal
4) Extract the magnitude and phase of the input and output signal at the defined frequency and calculate the attenuation and phase delay

B. Calibration

To guarantee precise measurements a calibration procedure is necessary. Therefore the DUT and the 50 Ω termination resistor (see Fig. 6) are replaced by a high frequency attenuator (see Fig. 7) at first. The attenuator is built with SMD resistors. According to Fig. 3 the resistor values do not change more than 100 ppm within the frequency range of 10 MHz. This makes the attenuator suitable for the calibration measurement.

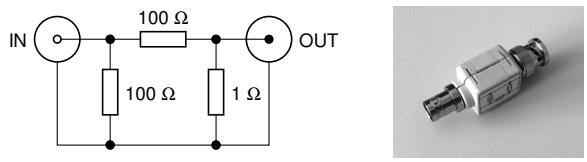

Fig. 7. 40 dB attenuator for calibrating the measurement circuit.

C. Results

We use bode plots to compare different divider assemblies and probes. All dividers and probes are 40 dB attenuators. For a better comparison only the deviation of this attenuation is plotted and the initial error at low frequencies is removed; see (4), where G is the output to input ratio in dB.

$$\text{Deviation}\,(f) = \text{G}\,(f) - \text{G}\,(f = 25\,\text{Hz}) \tag{4}$$

Fig. 8 shows the simulated and measured bode plot of the implemented voltage divider for two different values of C_2.

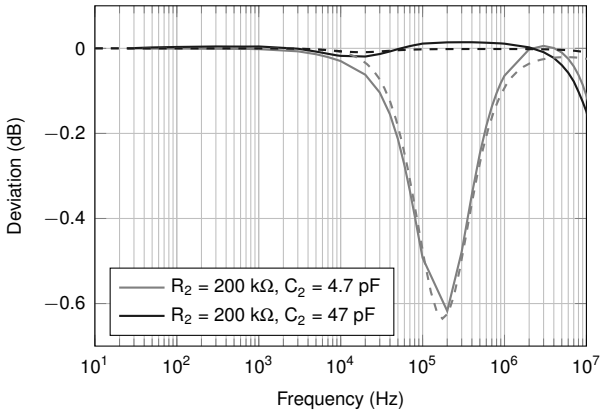

Fig. 8. Comparison of two different assemblies. Full lines are measured data; dashed lines are generated with a circuit simulation.

It is shown that the simulated curve meets the measured one quite well; this confirms that the circuit diagram shown in Fig. 5 suits well for the implemented divider. Additionally one sees that the deviation has a local extremum. The frequency f' where this extremum occurs and the value of the extremum $|\text{Deviation}\,(f')\,|$ are mainly determined by R_2 and C_2, see (5) and (6).

$$f' \approx \frac{1}{2\pi R_2 C_2} \tag{5}$$

$$|\text{Deviation}\,(f')\,| \sim \frac{C_{\text{GND}}}{C_2} \tag{6}$$

To minimize the influence of the extremum we aim to shift it towards high frequencies and minimize its magnitude. This may be achieved by choosing R_2 as low as possible and C_2 as high as possible. Both methods lower the input impedance of the divider; the choice of R_2 for DC and low frequencies, the choice of C_2 for high frequencies. A compromise between attenuation flatness and input impedance has to be made.

Fig. 9 shows the bode plot of the implemented voltage divider in comparison to some commercial high voltage differential active probes.

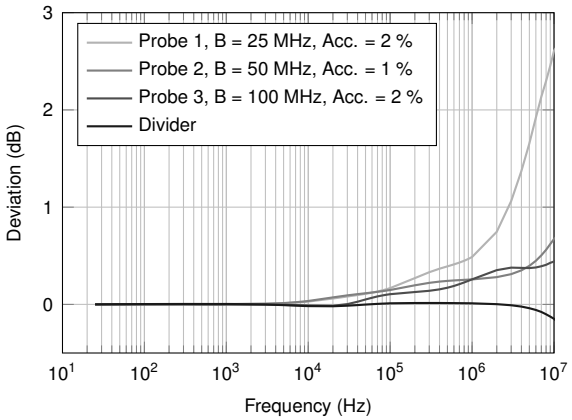

Fig. 9. Comparison of some high voltage differential active probes and the implemented voltage divider. All probes have a nominal attenuation of 40 dB; B is the bandwidth and Acc. the accuracy which is specified in the user manual.

One sees that the deviation of the commercial probes starts getting bigger than their given accuracy at about 10 to 100 kHz. This confirms, that the accuracy which is given by the manufacturers user manual, is only valid for DC and low frequencies. Our investigation leads to a voltage divider with a 0.02 dB flatness (0.23 % accuracy) up to 1 MHz and 0.2 dB flatness (2.3 % accuracy) up to 10 MHz.

IV. Conclusion and Outlook

In this paper we present the characterization of a resistive voltage divider. A simulation framework which considers the parasitic elements of the resistors and the layout is shown. Furthermore a voltage divider with a very flat frequency response up to 10 MHz is implemented.

The next step will be the design of a differential probe with the implemented divider at its input.

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B

Development of a Differential Voltage Probe for Measurements in Automotive Electric Drives

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Development of a Differential Voltage Probe for Measurements in Automotive Electric Drives

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***Abstract*—Accurate efficiency determination is very important in the field of electric drive research and development. Modern inverters generate pulsewidth modulated signals with short rise times and high frequencies. Thus, high-accuracy power measurements under non-sinusoidal conditions have to be performed. This requires high precision voltage and current probes, including frequency response flatness over a wide bandwidth and a high linearity up to a few hundred volts. This paper describes the development and characterization of a high voltage differential probe, suitable for precise measurements in automotive electric drives. The main parts of the probe are two input voltage dividers with a further frequency compensation circuit and a difference amplifier. The complete circuit design and the compensation of parasitic effects is explained in detail. Final experiments show, that the developed probe outperforms commercially available probes. The probe has a very flat frequency response up to 1 MHz, a bandwidth of 20 MHz and a linearity better than 250 ppm up to the maximum differential input voltage of 1 kV.**

***Index Terms*—Voltage measurement, power measurement, instruments - probes, automotive electronics, electric machines - AC machines, electric motors, differential amplifiers.**

I. Introduction

ROAD transportation contributed more than 10 % to the worldwide greenhouse gas emissions in 2010 [1]. To reach a significant reduction of these emissions by 2050, new technologies for vehicles will be a key [2]. Although inverter driven motors have already been used in industrial and commercial applications for many decades, a huge progress has been made in the field of power electronics and electric motors regarding cost reduction and efficiency improvement [3], [4], since the automotive industry focused on electric and hybrid vehicles. Due to the fact that efficiency improvement means an advance in driving range, it is one of the keys for the success of electric vehicles; thus accurate power and efficiency measurements are very important for electric drive research and development.

A typical automotive electric drive consists of a high voltage DC source (battery), an inverter and the motor, see Fig. 1. The inverter converts the DC voltage into a 3-phase AC voltage and vice versa. To minimize the power losses in the inverter, the conversion is done via pulsewidth modulated (PWM) signals with high switching frequency and short rise times, see Fig. 2. Thus, current and voltage contain high frequency harmonics, which makes the accurate power measurement to a challenging task [5]. In many publications, dealing with power measurements of non-sinusoidal signals, the lack of adequate voltage probes is discussed [6], [7].

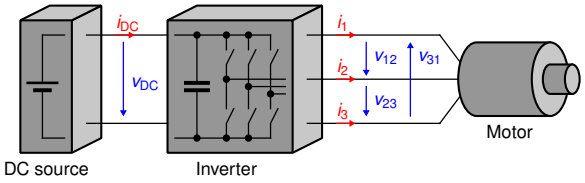

Fig. 1. Components of a typical electric drive. A DC source (battery) provides the power by means of v_{DC} and i_{DC}, the inverter generates a 3-phase system with the phase-to-phase voltages v_{12}, v_{23} and v_{31} to power the motor.

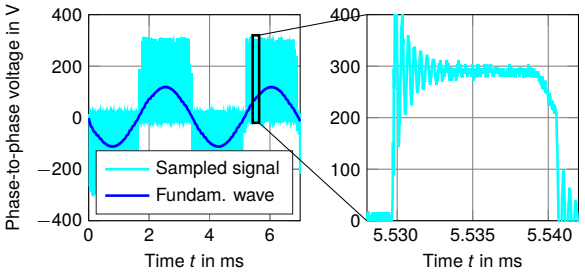

Fig. 2. Measured phase-to-phase voltage of an automotive electric drive. A PWM signal (Sampled signal) is used to approximate a sinusoidal motor voltage (Fundamental wave).

This paper describes the development of a superb voltage probe for highly accurate measurements in automotive electric drives. Section II defines the requirements for a voltage probe for measurements in electric drives. Section III compares some commercially available probes and research projects in this field and points out their insufficient performance. This yields to the development of a novel voltage probe, which is described in Section IV. Further, the experiments in Section V show the superb performance of the developed probe.

II. Requirements

In a typical automotive drive, only the phase-to-phase voltages are accessible, which makes it necessary to use a differential probe. As a rule of thumb, the sampling frequency should be at least ten times higher than the most significant

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harmonic [8]. Thus, a probe for differential amplitudes up to 1 kV and a frequency range from DC to 10 MHz should be sufficient for a modern drive [9]. A more precise formulation is given in [10], where the authors claim a gain accuracy of ±0.1 % up to the switching frequency, ±0.25 % up to four times the switching frequency and ±1 % up to 100 kHz (for a switching frequency of 5 kHz) to achieve a precise power measurement. Considering all these statements, the requirements for voltage measurements in a modern automotive drive (20 to 30 kHz switching frequency) are:

- Differential input voltage range up to 1 kV
- Common mode input range greater than 1 kV
- DC input impedance at least 4 MΩ
- Attenuation of 40 dB (100x probe)
- Attenuation flatness
  - ±0.1 % up to 1 kHz
  - ±0.2 % up to 100 kHz
  - ±1 % up to 1 MHz
  - −3 dB bandwidth of at least 10 MHz

III. State of the Art

A. Commercially available differential high voltage probes

There are many differential high voltage probes on the market. Nearly every manufacturer of oscilloscopes and electrical measurement equipment offers a few different types. It is nearly impossible to select an adequate probe for highly precise measurements in electric drives, because virtually none of the datasheets contain any information about the frequency response flatness and linearity of the probes. Only Keysight [11] and LeCroy [12] provide a frequency response plot to show an overview of the "overall" frequency response and give a graphical proof of the advertised −3 dB bandwidth. Nevertheless, it is not possible to read out a deviation in the (sub-)percent range. Additionally, it may be seen that the manufacturers of the probes allow some peaking in the frequency response to achieve a higher bandwidth.

For an overview, some probes of Testec [13]–[16] are evaluated. These probes are widely used - they are manufactured by Sapphire Instruments and sold by many different vendors (e.g. Testec). Because all these probes are rather low-cost devices, a high-quality probe from Tektronix [17] is also evaluated. The datasheet information of the evaluated probes is summarized in Table I.

For high-accuracy measurements under non-sinusoidal conditions, the gain flatness is a very important information, which is not given in any datasheet. A measurement of the probes' small signal behavior shows, that they have a gain flatness of 1 % up to only 50 kHz, see Fig. 3. Therefore it can be assumed that the given value for "Accuracy" is meant to be the accuracy at DC. A second measurement shows the strong non-linearity of the probes, see Fig. 4. Against expectation, the SI-51 which is classified as a high-accuracy probe, shows the worst behavior; the probe's gain changes about 0.5 % over the whole input voltage range. The high-quality probe of Tekronix shows the best frequency response flatness but also has a gain error of 1 % at 50 kHz and a non-linearity of 0.3 % up to 1 kV.

TABLE I
KEY FACTS OF EVALUATED COMMERCIALLY AVAILABLE PROBES

		Testec SI-9001	Testec SI-9002	Testec SI-51	Testec SI-9110	Tektronix P5205A
Bandwidth	MHz	25	25	50	100	100
Attenuation		10x, 100x	20x, 200x	100x	100x, 1000x	50x, 500x
Accuracy	%	2	2	1	2	- [4]
Rise time	ns	14	14	7	3.5	- [4]
Input impedance [1]	MΩ‖pF	4 ‖ 5.5	4 ‖ 5.5	4 ‖ 7	4 ‖ 7	5 ‖ 4
Input voltage [2]						
- Differential	V	70 , 700	140, 1400	700	140, 1400	130, 1300
- Common-mode	V	700	1400	1400	1400	1300
Output noise	µV	700	700	300	900	- [4]
SNR [3]	dBFS	77	77	84.3	60.8	- [4]
CMRR						
- Low frequency	dB@Hz	86@50	80@50	90@60	80@60	80@DC
- High frequency	dB@Hz	66@20 k	60@20 k	55@1 M	50@1 M	60@100 k
Price	$	350	350	400	500	1500

[1] Input to ground
[2] DC + AC peak
[3] Calculated value, not stated in the datasheet
[4] Not stated in the datasheet

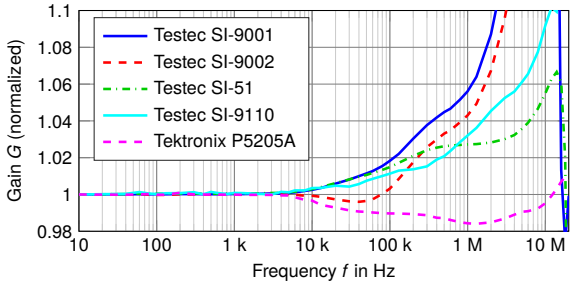

Fig. 3. Frequency response of different commercially available probes. The measurement is done with an input signal of 1 V amplitude.

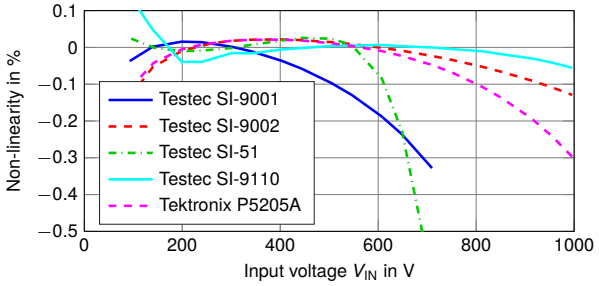

Fig. 4. Non-linearity of commercially available high voltage differential probes. The measurement is done with DC input signals.

B. Research projects

In [18] the authors explain their development of a high voltage differential probe. Their probe is built for differential input voltages up to ±3 kV, has a bandwidth of 10 MHz and is able to follow voltage edges up to 75 V/ns. Despite this promising specifications, they reach a gain flatness of only 2 % to 3 %, which makes it unfeasible for high-accuracy measurements over a wide frequency range.

Further, there are some metrological institutes which also work on voltage dividers, suitable for power measurements; [19] describes a divider which is "built for voltages up to 1 kV and frequencies to 20 kHz"; [20] "focuses on the design of a resistive voltage divider for voltages up to 240 V

(...) with minimal amplitude and phase errors at frequencies up to 100 kHz"; [21], [22] describe the characterization of resistive dividers for a power analyzer which is designed for voltages up to 600 V. All these works cover the design of high-accuracy dividers, but none of them meets the previously given requirements regarding maximum voltage and bandwidth. Also these designs only include single ended voltage dividers which make them unusable for measurements on electric machines where the voltages are not ground related. Although these dividers cannot be used for measurements in automotive electric drives directly, their design-thoughts are a great support towards the development of a new high voltage differential probe.

IV. Development of a differential probe

Fig. 5 shows the schematic of the developed probe. The first stage (A) consists of two identical voltage dividers. The high input voltages on both input terminals are attenuated to a small ground related voltage. To reach a superb frequency response flatness, an additional frequency response correction circuit (B) is used. Finally, a wide bandwidth difference amplifier (C) subtracts the two input voltages to create the ground related difference voltage on the output.

A. Input voltage divider

Each divider consists of $N_1 = 4$ identical blocks containing R_1, C_1 and R_{DAMP} in the high voltage branch, the components R_2 and C_2 on the low voltage side, some diodes D_1 and D_2 for over-voltage protection and an additional low-pass filter with R_{LP} and C_{LP} at the output. The low-pass filter and the damping resistors R_{DAMP} are inserted to block high frequency disturbances greater than 50 MHz. The protection diodes are low capacitance types to avoid any additional capacitive loading of the voltage divider.

For DC and low frequency signals the circuit acts as a resistive voltage divider built with R_1 and R_2. Although the attenuation of the probe should be 40 dB, the divider is designed with an attenuation of 54 dB to match the allowed input voltage levels of the following difference amplifier. For the divider, through-hole metal film resistors $R_1 = 1\,\mathrm{M\Omega}$ with a very low temperature coefficient (TC) of ± 5 ppm/K are used. This results in a maximum linearity error of 81 ppm due to self-heating at the maximum input voltage.

For rising frequencies the capacitive divider built with C_1 and C_2 starts dominating. To avoid any changes of the capacitance due to voltage or temperature, ceramic capacitors with a NP0 dielectric material are used. For a flat transfer function

$$G_{\mathrm{A}}(f) \stackrel{!}{=} G_{\mathrm{A}}(0) = \frac{1}{500} \tag{1}$$

has to be valid. For the circuit shown in Fig. 5 (A), this dependence can be approximated by choosing

$$\frac{R_2}{N_1 R_1 + R_2} \stackrel{!}{=} \frac{C_1/N_1}{C_1/N_1 + C_2 + C_{\mathrm{LP}}}, \tag{2}$$

where the adjustment is done by changing the capacitor C_2. Additionally, the non-ideal behavior of the components has to be considered. Hence, for further simulation the equivalent circuit diagrams for resistors and capacitors shown in Fig. 7 are used. In the resistor equivalent circuit, R represents the nominal resistor. The capacitance C_{PAR} combines all parasitic capacitors, like the internal shunt capacitance and the pad-to-pad capacitance due to the printed circuit board (PCB) mounting. The determination of this value is done by an impedance measurement at high frequencies; for high value resistors like R_1, the series inductance L_{SER} may be neglected [23]. In the capacitor equivalent circuit, C represents the nominal capacitance. The series elements R_{SER} and L_{SER} represent internal (component itself) and external (leads) parasitic behavior; values for internal elements may be found in the datasheet, values for the external elements strongly depend on the PCB design. To avoid additional external parasitic elements, leads and PCB traces are kept short. Both, the resistors and the capacitors, have a further parasitic capacitance C_{STRAY}. This capacitance occurs between the elements and the surrounding, which are other conductors, the housing of the PCB or even the environment of the probe if there is no conductive housing. Thus it is very difficult to predict a value for C_{STRAY}. To reach a constant and predictable capacitance C_{STRAY} a metal shield, which is connected to ground, is assembled around the divider. An exact calculation of C_{STRAY} is still only possible with a detailed electric field simulation like in [24]. A good approximation may be done by simplifying the geometry to a rectangular coaxial conductor, see Fig. 8. The analytic calculation of the specific capacitance is done in [25] and ends up with

$$\begin{aligned} C' = {} & 2\varepsilon \cdot \left(\frac{w}{h} + \frac{b}{g}\right) \\ & + \frac{4\varepsilon}{\pi} \cdot \left[\log\left(\frac{g^2+h^2}{4h^2}\right) + 2\,\frac{h}{g}\arctan\left(\frac{g}{h}\right)\right] \\ & + \frac{4\varepsilon}{\pi} \cdot \left[\log\left(\frac{g^2+h^2}{4g^2}\right) + 2\,\frac{g}{h}\arctan\left(\frac{h}{g}\right)\right], \end{aligned} \tag{3}$$

where b, g, h and w are the physical dimensions and ε is the dielectric permittivity of air. For the assembled geometry, a specific stray capacitance C' of 105 pF/m is calculated.

To avoid any loading of the input divider circuit, a unity gain amplifier is attached at the output. A dual supply, field effect transistor (FET) op-amp with high input resistance, low input capacitance and very low input bias current is used for this purpose.

Fig. 9 shows the results for the AC circuit simulation of the voltage divider. The Bode plots for an uncompensated, an undercompensated, a compensated and an overcompensated divider are shown. It can be seen that there is still a deviation of −0.1 dB (approximately 1 % gain flatness) at 10 kHz in case of compensation. To reach a frequency response with a better gain flatness, an additional frequency response correction is introduced.

B. Frequency response correction

For the frequency response correction, the input divider is left undercompensated by about 2 dB, see G_{A} in Fig. 6. This

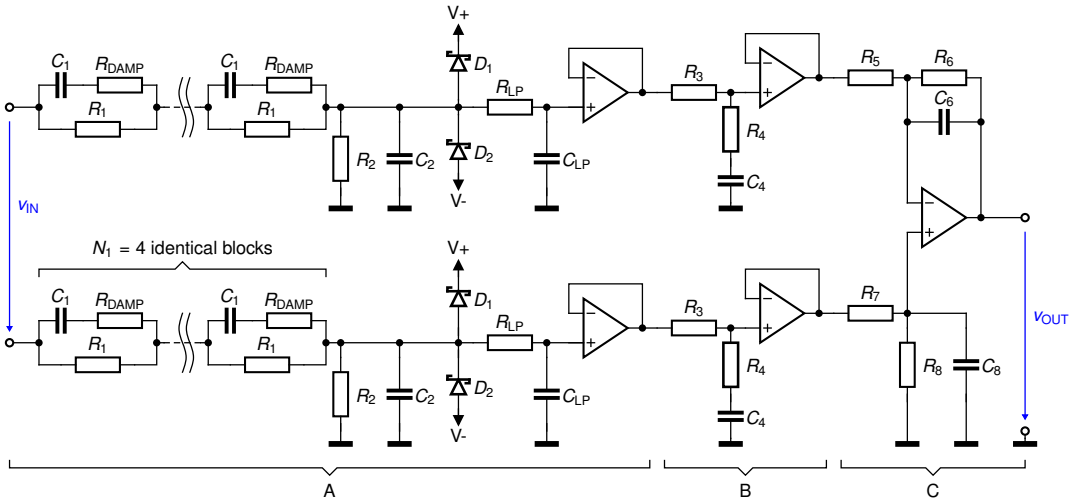

Fig. 5. Schematic of the developed differential probe. It consists of two identical voltage dividers (A), a lag circuit for frequency response correction (B) and a difference amplifier (C).

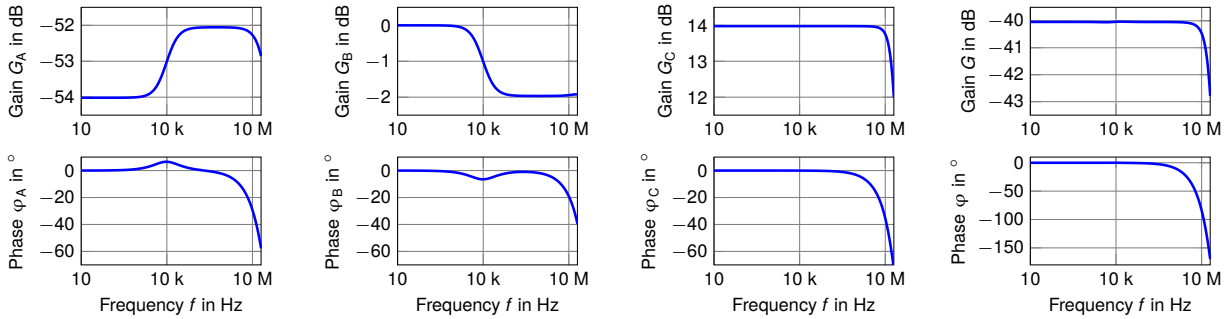

Fig. 6. Simulated Bode plot of the input voltage divider (G_A), the lag circuit for frequency response correction (G_B), the difference amplifier (G_C) and the resulting transfer function of the whole probe ($G = G_A \cdot G_B \cdot G_C$).

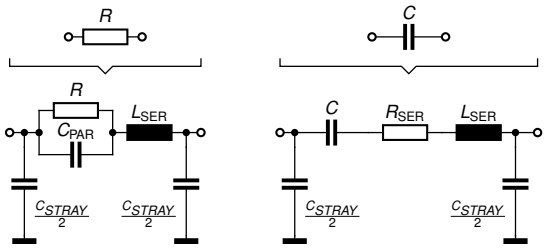

Fig. 7. Equivalent circuit diagrams for real life resistors and capacitors. R and C are the nominal parts, R_{SER}, L_{SER}, C_{PAR} and C_{STRAY} describe the non-ideal behavior.

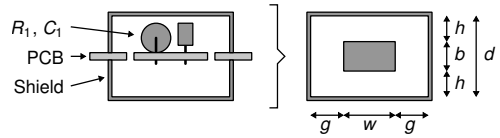

Fig. 8. Assembly of the high voltage branch on the PCB with surrounding copper shield (left) and simplified geometry for approximation of the stray capacitance (right).

is reached by choosing

$$C_2 = 0.7 \cdot C_1 \cdot \frac{R_1}{R_2}, \tag{4}$$

which is empirically determined and confirmed by a circuit simulation. The input divider is then followed by a lag circuit, see (B) in Fig. 5. This circuit has a DC gain of one and attenuates signals at high frequencies due to the resistive divider built with R_3 and R_4, see G_B in Fig. 6. Choosing values for R_3 R_4 and C_4 to reach

$$G_B(f) = \frac{G_A(0)}{G_A(f)}, \tag{5}$$

(see also section V, "B. AC gain" for detailed explanation of the calculation) results in a flat overall gain up to a few MHz, see G in Fig. 6.

C. Difference amplifier

To get the difference of the input voltages at the output, a difference amplifier is used, see (C) in Fig. 5. The amplifier is designed with a gain $G_C = 5$ to reach the overall attenuation of 100 for the probe.

The wide bandwidth, combined with the large output voltage swing of $\pm 10\,\mathrm{V}$ requires a high slew rate at the output. Therefore, an externally compensated op-amp is used, which maximizes the slew rate for the desired closed loop gain.

To reach a high common-mode rejection ratio (CMRR), a quad resistor array with a very low matching tolerance ($t_R =$

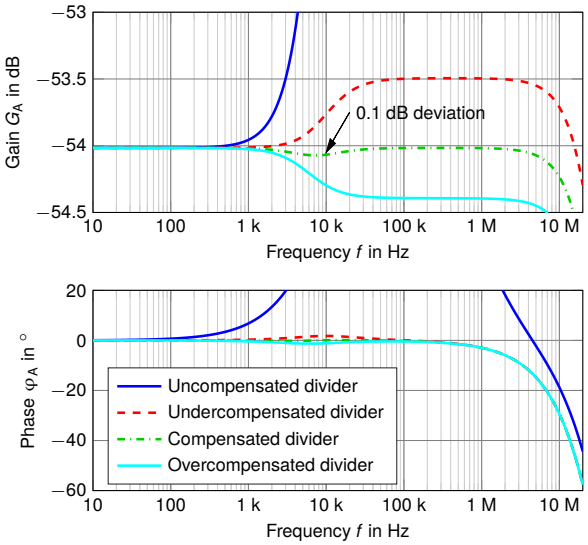

Fig. 9. Bode plot of the input voltage divider. The uncompensated divider (circuit without C_2) can be compensated by adjusting the capacitance C_2. A too small capacitance results in an undercompensated- a too big capacitance in an overcompensated divider. The compensated divider still shows a 0.1 dB deviation at 10 kHz.

0.025 %) is used for the resistors R_5 to R_8; the capacitors are standard $t_C = 5\,\%$ tolerance types. The contribution of the resistor mismatch to the CMRR of the amplifier is calculated with

$$\mathrm{CMRR}_R = \frac{1}{2} \cdot \frac{2\,R_6R_8 + R_6R_7 + R_5R_8}{R_5R_8 - R_6R_7} \tag{6}$$

which is derived in [26]. To consider the capacitors, R_6 is substituted by $\underline{Z_6}$, which is the parallel circuit of R_6 and C_6; R_8 is substituted by $\underline{Z_8}$, which is the parallel circuit of R_8 and C_8. This results in the CMRR

$$\mathrm{CMRR}_{RC} = \left| \frac{1}{2} \cdot \frac{2\,\underline{Z_6}\,\underline{Z_8} + \underline{Z_6}R_7 + R_5\underline{Z_8}}{R_5\underline{Z_8} - \underline{Z_6}R_7} \right| \tag{7}$$

contributed by the resistors and capacitors. For a worst case calculation $R_5 = R_{50}(1+t_R/2)$, $R_6 = R_{60}(1-t_R/2)$, $C_6 = C_{60}(1-t_C)$, $R_7 = R_{70}(1-t_R/2)$, $R_8 = R_{80}(1+t_R/2)$ and $C_8 = C_{80}(1+t_C)$ has to be chosen. R_{50} to R_{80}, C_{60} and C_{80} are the nominal values, t_R is the net matching tolerance of the resistor array and t_C is the tolerance of the capacitors. Because of using a resistor array, $t_R/2$ is used to guarantee a deviation of maximum t_r from one resistor to all others. Further the op-amp CMRR is considered to get the overall CMRR of the whole amplifier circuit [26], which is done with

$$\frac{1}{\mathrm{CMRR}} \approx \frac{1}{\mathrm{CMRR}_{RC}} + \frac{1}{\mathrm{CMRR}_{\mathrm{OPAMP}}(0)} + \frac{1}{\mathrm{CMRR}_{\mathrm{OPAMP}}(0)} \cdot \frac{f}{f_c}, \tag{8}$$

where $\mathrm{CMRR}_{\mathrm{OPAMP}}(0)$ is the low frequency CMRR of the op-amp and f_c is the frequency where the CMRR has decreased by 3 dB. The calculation results in a worst case CMRR for the difference amplifier of 80 dB up to 10 kHz. Further the CMRR decreases to 77 dB at 100 kHz, 64 dB at 1 MHz and 44 dB at 10 MHz.

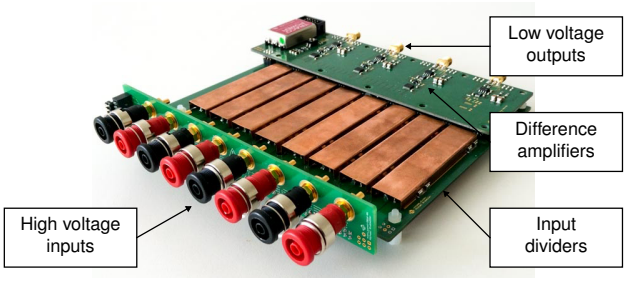

Fig. 10. Ready assembled voltage probe for measurements in automotive electric drives.

V. Experiments

All experiments shown in this section are done with the ready assembled voltage probe which is shown in Fig. 10. The probe already contains 4 differential voltage channels, which makes it suitable to measure all voltage signals of an automotive electric drive (3 phase-to-phase voltages and 1 battery voltage). The cost of material for a single probe is about 600 $ (20 % passive components, 20 % semiconductors, 20 % mechanic components and 40 % PCB).

A. DC gain

A Philips PE-4839 stabilized high voltage source (200 to 2000 V DC output voltage) is used to provide the high input voltage; for voltages below 200 V, a voltage divider is installed between the source and the probe. The input voltage is measured with a Keithley 2100 6 1/2-digit desk voltmeter (100 V and 1000 V DC range); for measuring the output voltage of the probe, a further Keithley 2100 is used (1 V and 10 V DC range). The measurement is iterated in 50 V steps from 100 V up to 50 % of the full-scale range (FSR) (500 V). Afterwards the nominal gain G is defined by approximating the slope of $V_{\mathrm{OUT}}(V_{\mathrm{IN}})$ by using a linear least squares curve fitting.

To calibrate the DC gain, the resistor R_2 of every divider is adjusted. To achieve a good long term stability this is not done via potentiometers. Instead, a resistor with a larger value than nominally required is assembled initially. After a gain measurement, R_2 gets adjusted by placing a further resistor in parallel.

To determine the gain non-linearity, the same setup as for calibrating the DC gain is used. The measurement of input and output voltage is done for voltages from 50 V up to FSR (1000 V), which results in an input voltage dependent gain curve $G(V_{\mathrm{IN}})$. The non-linearity is then defined by the deviation of $G(V_{\mathrm{IN}})$ from the nominal gain G, see Fig. 11. The developed probe has a maximum non-linearity of 250 ppm up to the maximum input voltage.

B. AC gain

A common method for measuring the AC gain is to measure the forward voltage gain S_{21} with a network analyzer [27]. As already mentioned in [28], this method is only applicable down to a few kHz due to the network analyzer's frequency

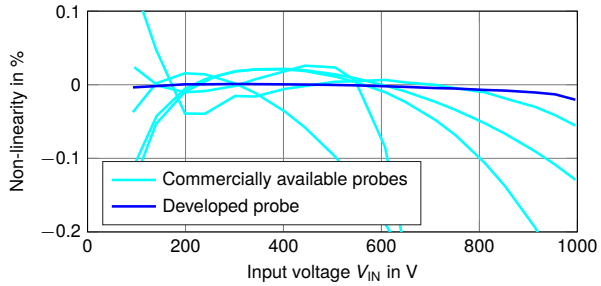

Fig. 11. Non-linearity of the developed probe, compared to the reviewed commercially available probes. The developed probe has a non-linearity of 250 ppm up to the maximum input voltage.

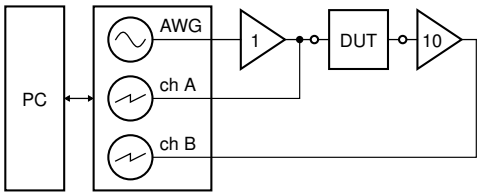

Fig. 12. Experimental setup for measuring the transfer function. The measurement is done with a high resolution USB oscilloscope with an integrated arbitrary waveform generator (AWG).

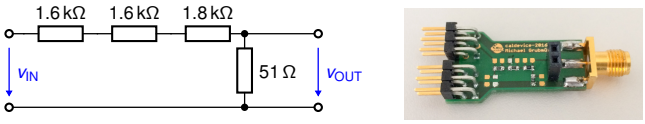

Fig. 13. Calibration device for the transfer function measurement setup. All resistors are surface mount devices in a 0603 package.

range. A further drawback is the insufficient accuracy of network analyzers. Thus, the measurements for this work are done with a Picoscope 5444B USB oscilloscope (200 MHz bandwidth, 125 MS/s sampling rate in 15 bit resolution and 2 channel mode) with an integrated arbitrary waveform generator (AWG). The measurement setup is shown in Fig. 12. To get the transfer function the waveform generator frequency is swept from 10 Hz to 20 MHz and the fast Fourier transformation (FFT) of in- and output voltage at the desired frequency is evaluated. An advantage of using an oscilloscope with an integrated AWG is that both use the same internal clock. Thus it is possible to set the sampling frequency exactly to an integral multiple of the signal frequency, which avoids leakage of the FFT.

Since the gain flatness has to be determined over a wide bandwidth in the sub-percent range, the setup has to be calibrated. For that reason, the device under test (DUT) in Fig. 12 is replaced by the calibration device shown in Fig. 13. To minimize the influence of the parasitic capacitance of the resistors in the calibration device, three resistors in series are used instead of a single 5 kΩ part in the upper branch. A circuit simulation for the calibration device, using the lumped circuit diagram of Fig. 7, verifies that this device has a 60 ppm gain flatness and less than 1° phase shift up to 20 MHz. Thus it is ideal for calibrating the setup in the range up to the desired

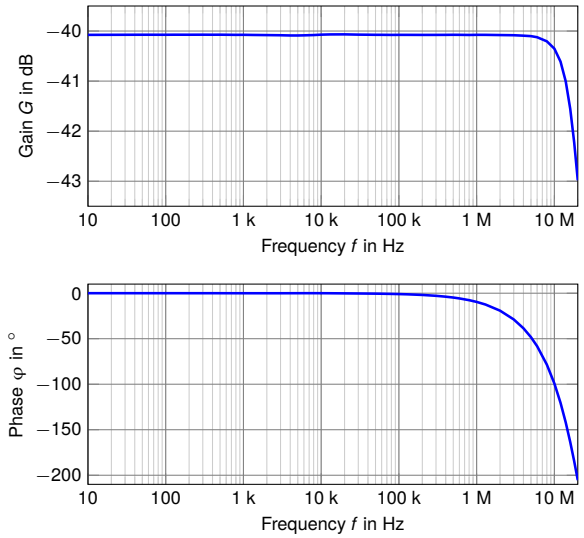

Fig. 14. Bode plot of the calibrated high voltage differential probe, showing the nominal attenuation of 40 dB (100x) and the bandwidth of 20 MHz.

20 MHz.

To calibrate the AC gain of the developed probe, an initial measurement of the undercompensated input divider gain G_A has to be done. In a next step the values for R_4 and C_4 in

$$G_\mathrm{B}(f) = \frac{\sqrt{(2\pi f)^2 R_4^2 C_4^2 + 1}}{\sqrt{(2\pi f)^2 (R_3 + R_4)^2 C_4^2 + 1}}, \tag{9}$$

are calculated, so that

$$G_\mathrm{B}(f) \stackrel{!}{=} \frac{G_\mathrm{A}(0)}{G_\mathrm{A}(f)}, \tag{10}$$

by solving the optimization problem

$$\min \left\| G_\mathrm{B}(f, R_4, C_4) - \frac{G_\mathrm{A}(0)}{G_\mathrm{A}(f)} \right\|, \tag{11}$$

in which G_B is the transfer function of the compensation circuit. Since standard ceramic capacitors have a tolerance of 5 %, the capacitors for C_4 have to be handpicked by measuring their value with a LCR meter. Fig. 14 shows the resulting Bode plot of the calibrated probe. It shows the nominal attenuation of 40 dB and the bandwidth of 20 MHz. Fig.15 shows the normalized magnitude of the Bode plot in a linear scale to point out the very flat frequency response. The probe has a frequency response flatness of ±0.1 % up to 1 kHz and ±0.2 % up to 2 MHz.

C. Rise time

The rise time of the developed probe is measured by applying a 0 to 500 V voltage step at the probe's input. The output voltage is sampled with a Tektronix TDS7154B 1.5 GHz 20 GS/s digital oscilloscope, see Fig. 16. To get the rise time t_R of the input step, the input signal is also measured with the 100 MHz Testec SI9110 probe. The rise time of the input is then calculated with

$$t_\mathrm{R} = \sqrt{t'^2_{\mathrm{R,SI9110}} - t^2_{\mathrm{R,SI9110}}} = 14.1\,\mathrm{ns}, \tag{12}$$

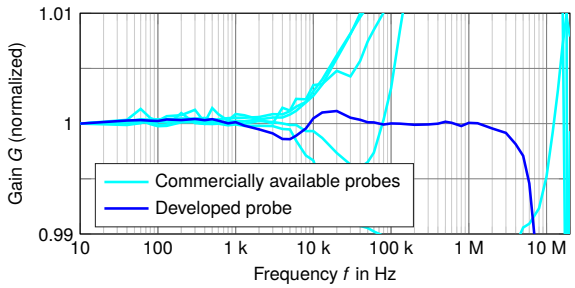

Fig. 15. Normalized gain of the developed differential probe. The probe has a frequency response flatness of ±0.1 % up to 1 kHz and ±0.2 % up to 2 MHz.

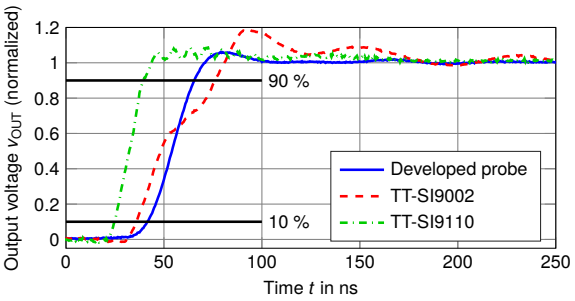

Fig. 16. Step response for a 0 to 500 V input step. For a comparison the normalized output voltages of the developed probe, the Testec SI9002 25 MHz probe and the Testec SI9110 100 MHz probe are shown.

where $t'_{\mathrm{R,SI9110}} = 15.6\,\mathrm{ns}$ is the measured rise time with the Testec device and $t_{\mathrm{R,SI9110}} = 3.5\,\mathrm{ns}$ is the true rise time of the Testec device which is given in the datasheet. In a similar way the rise time $t_{\mathrm{R,PROBE}}$ of the developed probe is calculated by

$$t_{\mathrm{R,PROBE}} = \sqrt{t'^2_{\mathrm{R,PROBE}} - t^2_{\mathrm{R}}} = 19\,\mathrm{ns}, \qquad (13)$$

with a measured rise time $t'_{\mathrm{R,PROBE}} = 23.7\,\mathrm{ns}$.

D. Input voltage derating

For DC and low frequency input signals, the input impedance of the probe is dominated by R_1, which limits the maximum allowable input voltage (input to ground) to 1.5 kV. With increasing frequencies, the input impedance decreases due to capacitor C_1, which is parallel to R_1. The resulting increase of the input current causes increasing power losses at the capacitor's C_1 series resistance and the damping resistor R_{DAMP}. To avoid any damages to C_1 and R_{DAMP} the input current has to be limited, which is done by derating the maximum allowable input voltage over frequency. The derating is calculated to limit the temperature rise of C_1 to 20 K and to limit the power loss of R_{DAMP} to 0.25 W. The resulting derating curve is shown in Fig. 17. It shows that the maximum input voltage of 1.5 kV may be applied up to 700 kHz, 1 kV may be applied at 1 MHz and finally a 20 MHz signal must not exceed 80 V.

E. Signal-to-noise ratio

To calculate the signal-to-noise ratio (SNR) of the probe, the RMS output noise E_{PROBE} has to be measured for a bandwidth of 20 MHz. At first, the output voltage of the probe with short-circuited inputs is sampled with an oscilloscope at a rate of 40 MS/s. Calculating the standard deviation of these samples delivers $E'_{\mathrm{PROBE}} = 593.5\,\mu\mathrm{V}$, the combined noise of the probe and the oscilloscope. At second, the inherent noise of the oscilloscope $E_{\mathrm{SCOPE}} = 115.6\,\mu\mathrm{V}$ is measured by taking samples with a short-circuited oscilloscope input. Finally, the output noise of the developed probe is calculated by

$$E_{\mathrm{PROBE}} = \sqrt{E'^2_{\mathrm{PROBE}} - E^2_{\mathrm{SCOPE}}} = 582.1\,\mu\mathrm{V}, \qquad (14)$$

which leads to

$$\mathrm{SNR} = 20\log\left(\frac{\widehat{v}_{\mathrm{OUT,MAX}}/\sqrt{2}}{E_{\mathrm{PROBE}}}\right) = 81.7\,\mathrm{dBFS}, \qquad (15)$$

where $\widehat{v}_{\mathrm{OUT,MAX}}$ is the full-scale output voltage of 10 V.

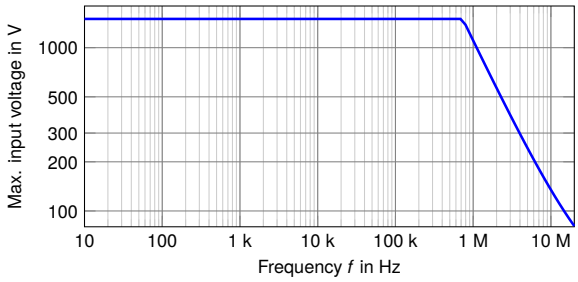

Fig. 17. Derating of the maximum allowable input voltage (DC + AC peak) over frequency.

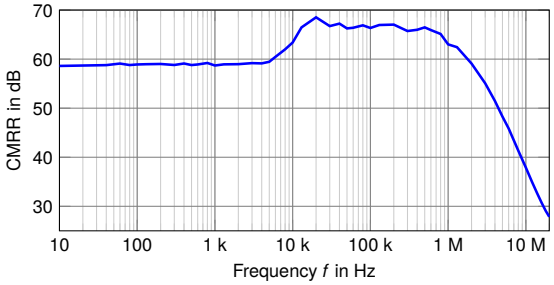

Fig. 18. Common-mode rejection ratio of the developed probe.

F. Common-mode rejection ratio

The measurement of the CMRR is done with the same setup as used for measuring the transfer function, see Fig. 12, with the difference that the input signal is now provided to both input terminals of the developed probe. Fig. 18 shows the resulting CMRR of the probe. It can be seen that the CMRR has a constant value of 59 dB up to 10 kHz, increases by a few dB and stays constant up to 1 MHz before it rolls off to 28 dB at 20 MHz. The change of the CMRR at 10 kHz is caused by the two-step calibration procedure; the CMRR up to 10 kHz is dominated by the DC gain calibration, the CMRR at higher frequencies is dominated by the AC gain calibration.

VI. Summary

Accurate power and efficiency measurements are very important for automotive electric drive research and development.

This requires high-accuracy voltage probes for measuring the inverter voltage signals. This paper demonstrates that commercially available probes do not fulfill the requirements regarding gain flatness and linearity. Further the development of a high voltage differential probe is presented. By showing circuit simulation results and rough calculations, the importance of considering the parasitic effects of the circuit components and the PCB assembly is shown. The experimental results confirm the superb performance of the probe, regarding frequency response flatness, non-linearity, rise time, SNR and CMRR.

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A Digital Isolated High Voltage Probe for Measurements in Power Electronics

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***Abstract*—For the development and optimization of highly efficient power electronic systems, it is essential to precisely measure voltage signals of fast-switching high voltage semiconductors. Due to various reasons off-the shelf high voltage differential probes are not suitable for those measurements. In this paper a digital isolated high voltage probe, especially designed for measurements in power electronics, is presented. The analog to digital conversion of the input signal is already done at the probe, the galvanic isolation is done on the digital lines. In the paper a detailed explanation about the development is given as well as an extensive characterization of a built prototype. The prototype withstands a permanent isolation voltage of 1500 V. It continuously streams 18 bit ADC data at a sampling rate of 5 MS/s. Special care is taken to reach a flat frequency response and a superb linearity up to the maximum differential input voltage of 1500 V.**

***Index Terms*—Automotive electronics, power electronics, instruments–probes, power measurement, voltage measurement**

I. Introduction

Power electronics are playing a dominant role in the 21st century, because they are the key to high efficient power converter systems [1]. One example for such a system is the electric drivetrain of an electric vehicle (EV), hybrid electric vehicle (HEV) or fuel cell electric vehicle (FCEV). Here an inverter is used to transform a dc voltage, delivered by a battery or a fuel cell, into a variable-frequency 3-phase ac voltage to power a motor (Fig. 1). A further example is a photovoltaic system; here an inverter is used to transform the dc voltage, delivered by the photovoltaic cells, into a constant-frequency 3-phase voltage system (Fig. 2). For the development and optimization of such systems, it is essential to precisely measure in- and output voltages of the inverter. Since power electronics use fast-switching semiconductor devices to approximate sinusoidal output voltages, the voltage signals not only contain the fundamental wave but also some high frequency harmonics. Especially for power and efficiency measurements of inverters it is very important to also measure those harmonics with an adequate accuracy [2], [3].

A. High Voltage Differential Probe

The state of the art probe for measuring floating high voltage signals is the high voltage differential probe (Fig. 3). Nearly every manufacturer of oscilloscopes and electrical measurement equipment offers a few different types. It consists of two well matched input voltage dividers and a differential amplifier. The ground related output signal is the scaled down input differential voltage. High voltage differential probes, especially developed and characterized for measurements on power electronics, are shown in [4], [5].

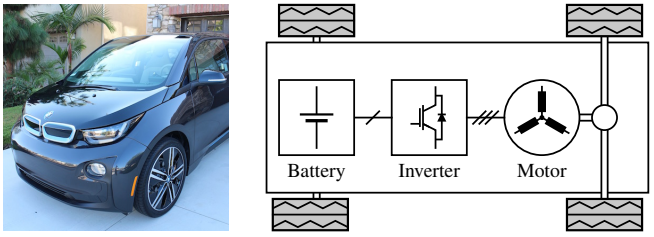


Fig. 1. Automotive electric drivetrain: A battery provides the energy; further an inverter generates a variable-frequency 3-phase voltage to power the motor.

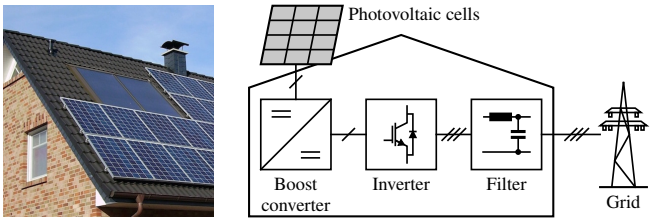


Fig. 2. Photovoltaic system: First the small dc voltage of the photovoltaic cells is increased by a boost converter; afterwords the inverter builds a constant-frequency 3-phase ac voltage to connect to the grid.

B. Isolated High Voltage Probe

For some applications the use of a high voltage differential probe is not possible. One example is the measurement of the gate-emitter voltage in power electronics. The relatively small gate control voltages are superimposed by high voltage common mode jumps. Thus, the voltage probe requires a very high common-mode rejection ratio (CMRR). A further example is the measurement of the inverter output voltages where the inverter is already assembled in an EV. For that purpose an isolated measurement concept is necessary, because the earth connected measurement with a differential

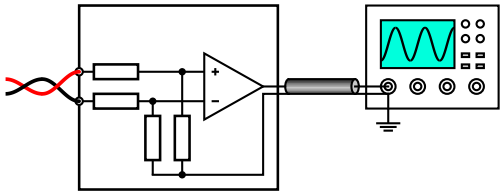
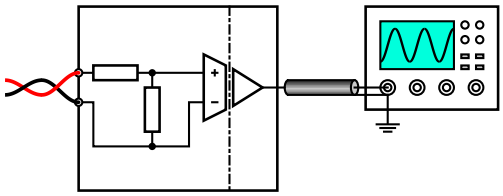
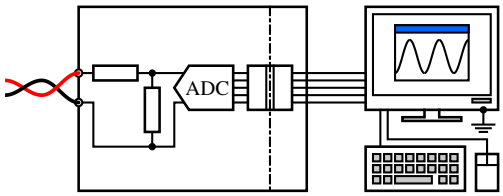


Fig. 3. High voltage differential probe: Two well matched input dividers scale down both input voltages; further a differential amplifier outputs the scaled down input differential voltage.



(a) Analog isolated high voltage probe



(b) Digital isolated high voltage probe

Fig. 4. Isolated high voltage probe; the signal isolation of such a probe may either be done at the analog signal or at the digital interface.

high voltage probe could cause an isolation error. Isolated oscilloscopes or battery powered oscilloscopes should not be used for floating measurements in power electronics [4]. The isolation in isolated oscilloscopes is not designed for continuous operation at several hundreds of volts; battery powered oscilloscopes, may introduce a large capacitance to earth. Thus, it is recommended to use isolated high voltage probes. The signal isolation of an isolated probe may either be done at the analog signal or at the digital interface.

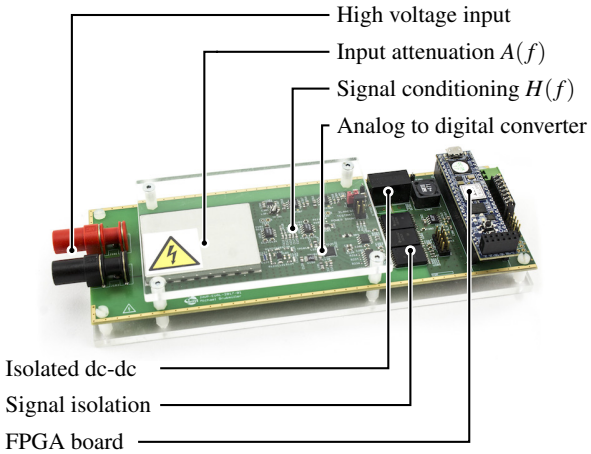
1) Analog Isolated High Voltage Probe: An analog isolated high voltage probe uses a high voltage divider to scale down the input voltage and an isolation amplifier to isolate the output from the input. The isolation amplifier could also be replaced by a fiber optic transmission system [6], [7]. The advantage of an analog fiber optic transmission is, that there is no limitation regarding the isolation voltage; drawbacks are the poor linearity and a strong aging effect.

2) Digital Isolated High Voltage Probe: In a digital isolated high voltage probe the analog to digital conversion is already done in the probe. The isolation is done by isolating the digital data lines. This may be realized by a digital isolation integrated circuit (IC), a digital fiber optic transmission or even wireless. In [8], [9], a Bluetooth probe is shown; with this approach the cabling can be reduced, especially when there are more measurement points at the same time, e.g. measuring all 3 inverter output voltages and the dc input. A drawback of this probe is, that the Bluetooth data transfer is too slow for continuous transmission of high-sampling-rate and high-resolution data. Thus only short time slots are measured and stored in a memory before they get transmitted.

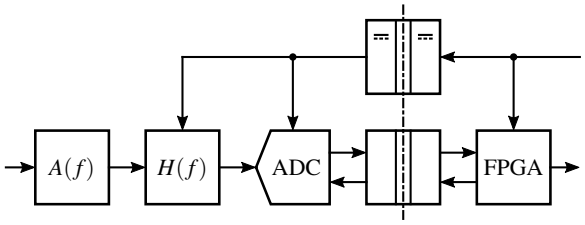
In this paper the authors present their work on a digital isolated high voltage probe with a continuous isolation voltage of 1500 V. The probe continuously streams the 18 bit ADC data at a sampling rate of 5 MS/s. Special care is taken to reach a flat frequency response and a superb linearity over the complete input voltage range of ±1500 V.

II. Development of a Digital Isolated High Voltage Probe

The basic concept of a digital isolated high voltage probe is shown in Fig. 4b; a more detailed block diagram and a foto of the built prototype is given in Fig. 5. At first the high



(a) Prototype



(b) Block diagram

Fig. 5. Prototype and block diagram of the developed digital isolated high voltage probe.

input voltage gets attenuated by $A(f)$. Further some analog signal conditioning $H(f)$ is necessary, before the analog-to-digital conversion is done. Output lines and input control signals of the ADC are galvanically isolated with digital isolation components. The control of the the ADC and the data transmission from the ADC to a computer is implemented in an FPGA. To power the galvanic isolated part of the circuit an isolated dc-dc module is used. In the following sections, the particular stages are explained more in-depth.

A. Input Attenuation

The input stage of the probe is a frequency-compensated resistive-capacitive voltage divider [10]–[12]. The divider has an input impedance of 4 MΩ parallel with 5.5 pF. To reach high linearity, resistors with very low temperature and voltage coefficient (25 ppm/K, 1 ppm/V) and capacitors with C0G dielectric are chosen. The dividers' attenuation $A = 1/750$ leads to an output voltage of ±2 V at the maximum input voltage of ±1500 V. In order to reach a defined stray capacitance, necessary for a well defined frequency response, a shield is put around the divider. A detailed circuit and an in-depth simulation framework including the parasitic behavior of the passive components and a stray capacitance approximation has already been presented by the authors [5], [13].

B. Signal Conditioning

Some analog signal conditioning circuitry is applied to interface the input attenuator to the ADC. First, a programmable gain amplifier (PGA) is used to expand the dynamic range of the ADC. The PGA has a switchable gain of 1, 2, 5, 10 and 20, enabling additional input voltage ranges of 750 V, 300 V, 150 V and 75 V. Second, a fully differential amplifier generates the differential input signal, necessary for the ADC. The fully differential amplifier is also used as an anti-alias filter, implemented with a multiple feedback (MFB) topology. The filter is a 3rd order Bessel type with a −3 dB cutoff frequency at 1 MHz and a dc gain of 2.

C. Analog-to-Digital Conversion

The used ADC is the LTC2385-18 from Linear Technology, an 18 bit successive approximation register (SAR) type with 5 MS/s sampling rate. The component is chosen for its excellent linearity (maximum ±1.5 LSB integral linearity error) and the very good signal-to-noise ratio (SNR) of 95.7 dB.

D. Isolation

Before choosing any isolation component for power or signal isolation, one has to understand the terminology for isolation ratings. Definitions are given in different standards; a good summery is given in [14]. Datasheets of isolation ICs and dc-dc modules usually advertise a very high isolation voltage at their first page. It is very important to know that this is only a transient isolation voltage, tested for 60 s (qualification testing) or 1 s (production testing), but must not be applied continuously. For that reason some manufacturers also give a value for the maximum isolation working voltage or some kind of conversion between transient isolation voltage and maximum isolation working voltage.

1) Supply isolation: For isolating the power supply a Recom R05P05S/X2/R8 is used. It is a 1 W unregulated dc-dc converter with 5 V in- and output voltage. It has a reinforced isolation of 8 kV (tested for 1 s) and may be used for a continuous isolation voltage of 4 kV [15]. The added isolation impedance due to the converter is 15 GΩ parallel with 10 pF.

2) Signal Isolation: For isolating the digital ADC in- and output lines, isolation ICs of the ISO7820x and ISO7830x series of Texas Instruments are used. These parts are the only parts available, combining a high data rate (100 Mb/s) with a very high maximum isolation working voltage (2000 V) and high common-mode transient immunity (±100 kV/μs). The added isolation impedance due to the isolation ICs is about 300 GΩ parallel with 3 pF.

To guarantee the high isolation not only on component level but also on system level, all creepage distances between the isolated circuit parts are chosen according to [16]. In addition the printed circuit board (PCB) is milled underneath the digital isolation ICs and the dc-dc module to prevent any deposition of conductive dirt or moisture.

E. Control and Data Transmission

To control and readout the ADC, and transfer the ADC data to a computer, a field programmable gate array (FPGA) is used. The FPGA continuously outputs the ADC data via two 100 Mb/s UARTs. The UART signals are sampled by a logic analyzer and further streamed to a computer over USB.

III. Experimental Characterization

In the following sections, the performance of the built prototype of the digital isolated high voltage probe is analyzed. Measurement procedures and results are presented.

A. Noise and SNR

To measure the output noise, positive and negative input of the probe are shorted and $1 \cdot 10^6$ ADC samples d_i are taken. The RMS output noise E_{out} is then calculated by

$$E_{\text{out}} = \sigma(d_i)\,, \tag{1}$$

where $\sigma(d_i)$ is the standard deviation of the ADC samples d_i. For better interpretation the input referred noise E_{rti} is calculated by

$$E_{\text{rti}} = E_{\text{out}} \cdot V_{\text{lsb}} \cdot \frac{A}{H}\,, \tag{2}$$

where V_{lsb} is the voltage of the least significant bit of the ADC, A is the attenuation of the input divider and H is the gain of the programmable gain amplifier and the fully differential amplifier. Thus the SNR expressed in dB-full-scale (dBFS) results to

$$\text{SNR} = 20 \cdot \log_{10}\left(\frac{\widehat{v}_{\text{in,max}}/\sqrt{2}}{E_{\text{rti}}}\right), \tag{3}$$

where $\widehat{v}_{\text{in,max}}$ is the maximum allowable input voltage of the particular input range. Results of the measurements are shown in Tab. I.

B. Frequency Response

For the measurement of fast-switching signals, the probe's frequency response is a very important parameter. Since the

TABLE I
NOISE, SNR AND BANDWIDTH OF THE PROTOTYPE

Input Range $\widehat{v}_{\mathrm{in,max}}$ (V)	**Noise** E_{rti} (mV)	**Signal-to-noise** SNR (dBFS)	**Bandwidth** $f_{-3\,\mathrm{dB}}$ (MHz)
1500	30.5	90.8	1
750	20.6	88.2	1
300	15.4	82.8	0.9
150	13.3	78.0	0.8
75	11.3	73.4	0.6

absolute value can easily be calibrated, the relative frequency response G/G_0 is more significant.

$$G/G_0 = \frac{G(f)}{G(f=10\,\mathrm{Hz})} \tag{4}$$

$$= \frac{\widehat{d}(f)/\widehat{v}_{\mathrm{in}}(f)}{\widehat{d}(f=10\,\mathrm{Hz})/\widehat{v}_{\mathrm{in}}(f=10\,\mathrm{Hz})} \tag{5}$$

The measurement is done with a 0.1 % full-scale range (FSR) small signal input amplitude of $\widehat{v}_{\mathrm{in}} = 1.5\,\mathrm{V}$. Fig. 6 shows the Bode plot of the prototype's frequency response compared to the simulated curve of an ideal 3rd order Bessel filter. Fig. 7 shows the Bode plot in linear scale. It also shows the comparison of the prototype with a simulation of an ideal 3rd order Bessel filter as well the result of a detailed circuit simulation, including parasitic behavior of the passive components and models of the used op-amps. It can be seen that the prototype has a frequency response flatness better than ±1 % up to 100 kHz.

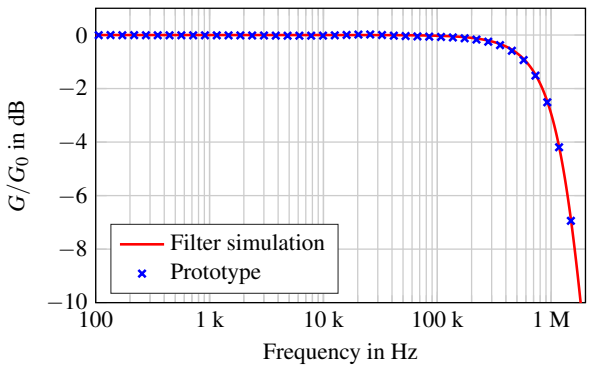


Fig. 6. Relative frequency response of the prototype. The simulated curve shows the frequency response of an ideal 3rd order Bessel filter.

C. Common-Mode Rejection Ratio

For measurements on power electronics a probe with a high CMRR is necessary. The CMRR evaluation of the developed probe is done by first applying a sinusoidal voltage with an amplitude of $\widehat{v}_{\mathrm{in,d}}$ at the probes' inputs and measuring the output amplitude $\widehat{d}_{\mathrm{d}}$. In a second step the inputs are shorted and a sinusoidal voltage with the amplitude $\widehat{v}_{\mathrm{in,cm}}$ is applied

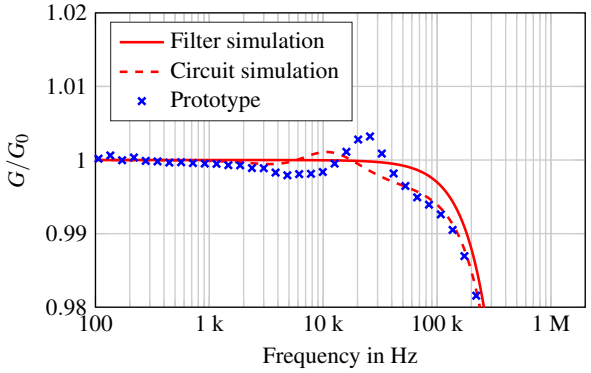


Fig. 7. Relative frequency response of the prototype in linear scale. The simulated curves show the frequency response of an ideal 3rd order Bessel filter and a circuit simulation of the whole analog input circuit.

as a common-mode signal, resulting in an output amplitude of $\widehat{d}_{\mathrm{cm}}$. Further the CMRR can be calculated by

$$\mathrm{CMRR} = 20 \cdot \log\left(\frac{G_{\mathrm{d}}}{G_{\mathrm{cm}}}\right) = 20 \cdot \log\left(\frac{\widehat{d}_{\mathrm{d}}/\widehat{v}_{\mathrm{in,d}}}{\widehat{d}_{\mathrm{cm}}/\widehat{v}_{\mathrm{in,cm}}}\right). \tag{6}$$

As the amplitude of the input differential signal is equal to the amplitude of the input common mode signal, $\widehat{v}_{\mathrm{in,d}} = \widehat{v}_{\mathrm{in,cm}}$, the calculation can be simplified to

$$\mathrm{CMRR} = 20 \cdot \log\left(\frac{\widehat{d}_{\mathrm{d}}}{\widehat{d}_{\mathrm{cm}}}\right)\Bigg|_{\widehat{v}_{\mathrm{in,d}}=\widehat{v}_{\mathrm{in,cm}}}. \tag{7}$$

Fig. 8 shows the resulting CMRR of the prototype. It displays a very high CMRR for low frequencies; for higher frequencies the CMRR decreases but still remains over 60 dB up to 2 MHz. The good CMRR values can only be reached by putting a shield around the divider, the analog circuitry and the ADC.

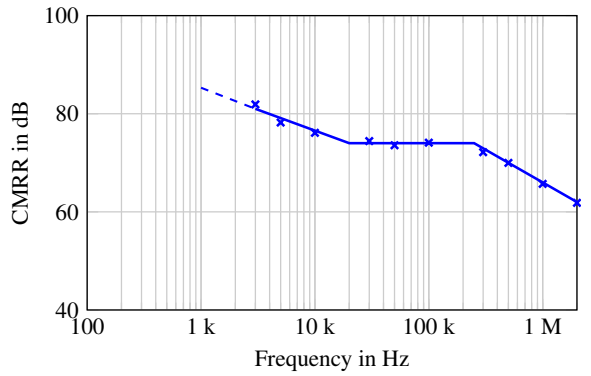


Fig. 8. Measured common-mode rejection ratio of the prototype.

D. Rise/Fall Time and Propagation Delay

To measure rise/fall time and propagation delay of the probe, a square wave with 10 V amplitude is applied at the probe's input. Rise and fall time of the input signal is 2 ns. Fig. 9 shows the resulting output signal. It displays a

TABLE II
COMPARISON OF DIFFERENT HIGH VOLTAGE PROBES FOR MEASUREMENTS IN POWER ELECTRONICS

		Tektronix P5202A [18] Differential probe	**Grubmüller et al. [5]** Differential probe	**Lobsiger et al. [9]** Isolated probe	**Presented probe** Isolated probe
Input voltage					
- Differential	V	±1300	±1000	- [a]	±1500
- Common mode	V	±1300	±1500	> 1 M	±1500
Input impedance					
- Differential	MΩ || pF	10 || 2	8 || 2.8	- [a]	4 || 5.5
- To ground	MΩ || pF	5 || 4	4 || 5.5	-	-
Isolation					
- Technique		-	-	Bluetooth	Isolation IC
- Impedance	GΩ || pF	-	-	>>	> 1 || 13
Bandwidth	MHz	50	20	100	1
CMRR					
- DC	dB	> 80	60	-	> 80
- Medium frequency	dB @ Hz	> 60 @ 100 k	66 @ 100 k	> 80 @ 200 k [b]	74 @ 100 k
- High frequency	dB @ Hz	> 30 @ 3.2 M	62 @ 1 M	-	66 @ 1 M
Analog-to-digital					
- Sample rate	MS/s	-	-	400	5
- Memory length	Samples	-	-	200 k	- [c]
- Resolution	bit	-	-	8	18

[a] The probe does not have a high voltage input - it has to be combined with a passive oscilloscope probe.
[b] Result in combination with a 10:1 passive oscilloscope probe.
[c] No memory on the device - continous streaming to a computer.

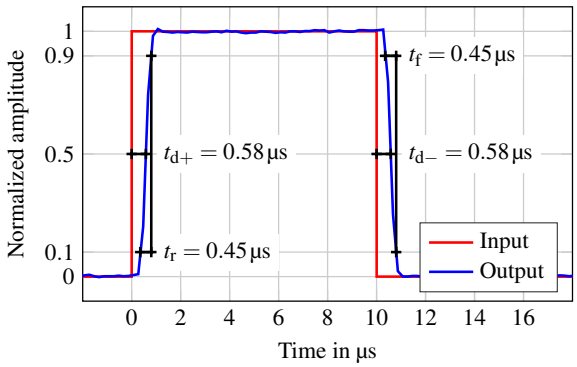


Fig. 9. Timing values of the prototype. The measurement is done with a 10 V amplitude square wave at the probes' input.

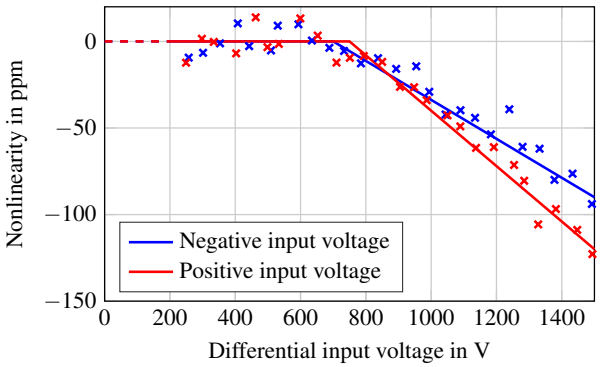


Fig. 10. Nonlinearity of the prototype for high voltage dc input voltages up to the full-scale range of ±1500 V.

symmetric behavior for falling and rising edges; propagation delay is 0.58 µs for both edges, rise and fall time is 0.45 µs.

E. Nonlinearity

The measurement of the nonlinearity is done by applying a high voltage dc differential signal at the probes' input. The signal is provided by a high voltage dc source. It delivers a symmetrical high voltage around earth potential; the voltage is measured with two Keithley 2100 6 1/2 digit desk multimeters. Further the nonlinearity is calculated according to [17]. First the nominal gain of the probe is defined by a linear least square fit of the gain for input voltages from 0 to 50 % of the full-scale range. Second, the nonlinearity is then expressed by the deviation of the measured gain from the nominal gain of the previous step. Fig. 10 shows the resulting nonlinearity for negative and positive input voltages ranging up to the full-scale of ±1500 V. The resulting nonlinearity is better than 150 ppm.

F. Comparison

Table II shows a comparison of a high-end differential high voltage probe from Tektronix [18], a differential high voltage probe previously presented by the authors [5], a Bluetooth isolated probe [9] and the presented probe. It can be seen that isolated probes have a better CMRR than differential probes. By comparing the Bluetooth probe with the presented probe, it is clear that both probes are designed for different use cases. The Bluetooth probe was designed for fast, very

wide bandwidth short term measurements, like the measurement of the gate-emitter voltage of power converters. The presented probe is built for high precision continuos high voltage measurements, like necessary for power and efficiency measurements of automotive and solar inverters.

IV. Summary

In this paper the authors present a digital isolated high voltage probe for measurements on power electronics. The experimental evaluation of a prototype shows, that the probe is suitable for measurements of fast-switching high voltage signals. Low noise, flat frequency response and very good linearity confirms that the probe can be used for high accuracy measurements.

Acknowledgment

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Passband frequency response measurement of a high voltage differential probe up to 10 MHz

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Passband frequency response measurement of a high voltage differential probe up to 10 MHz

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***Abstract*—High voltage differential probes are widely used for measurements in power electronics. For accurate measurements in power electronics, the use of probes with flat passband frequency response is indispensable. In this article we present a measurement method to evaluate the passband frequency response of a probe up to 10 MHz. We introduce an oscilloscope based setup, including a calibration procedure with a reference attenuator. Amplitude and phase estimation of the oscilloscope data is done with enhanced versions of the IEEE 1057 and 1251 sine-wave fit algorithms. The feasibility of the presented method is verified by a detailed uncertainty evaluation for the complex valued passband frequency response. The uncertainty assessment is done with two different methods, provided by the Guide to the Expression of Uncertainty in Measurement (GUM) and the associated Supplement 2.**

***Index Terms*—Voltage probe, frequency response, sine-wave fit, uncertainty, GUM, Standard 1057 and 1251**

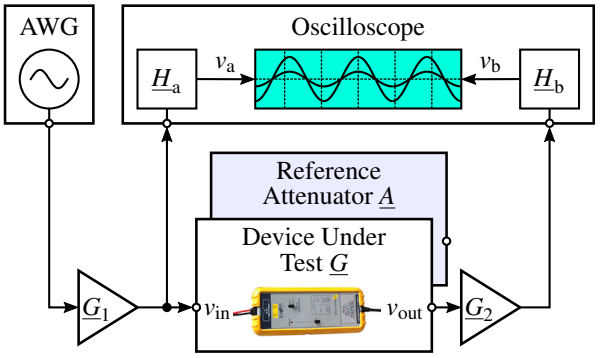

Figure 1. Measurement setup to obtain the frequency response of a high voltage differential probe. The measurement is first done with a reference attenuator, followed by the measurement of the device under test.

I. Introduction

High voltage differential probes are essential devices for voltage measurements in power electronics. Since power electronics use fast-switching pulse-width modulation (PWM) techniques, the voltage signals contain a low frequency fundamental wave as well as a high frequency PWM carrier and intermodulation components. To precisely measure all signal components a probe with flat passband frequency response is necessary; in the case of power electronics the frequency band ranges from dc up to several megahertz.

In this paper we address the measurement of the passband frequency response of a high voltage differential probe for the desired frequency range. The most common methods to measure the frequency response of a circuit are the S_{21} parameter measurement with a network analyzer, or the use of an oscilloscope or voltmeter combined with a waveform generator [1], [2]. Due to the desired frequency range, the measurement with an oscilloscope is chosen (Fig. 1). The challenges with the applied method are, that oscilloscopes only have a limited dc accuracy and frequency dependent internal signal paths. To overcome these difficulties we introduce a calibration strategy with a well defined reference attenuator. The dc gain of the reference attenuator is measured with a precision desk multimeter; the ac frequency response is flat in the passband due to its design, which is verified by a detailed circuit analysis. As a result the presented measurement method combines the high dc accuracy of the multimeter with the wide bandwidth of the oscilloscope.

Since oscilloscope measurements are time domain measurements, but we are interested in a frequency transfer function, a transformation of the data is necessary. Therefore we use the least square sine-wave fit suggested by the IEEE Standards 1057 [3] and 1251 [4]. The standards deliver a three- (known frequency) and four-parameter (unknown frequency) algorithm to determine amplitude V, phase ϕ and an additional offset V_0 of a sinusoidal signal. The three-parameter algorithm can be realized with matrix operations only, resulting in very low computation complexity. The four-parameter algorithm is an iterative algorithm that also estimates the unknown signal frequency f. The standards explain both algorithms very well, but some points remain untreated: When to use the three- or the four-parameter algorithm; how to determine the number of samples necessary for good estimation results; how to choose a good starting value for the frequency estimation in the four-parameter algorithm; how to define a stop condition or number of iterations for the four-parameter algorithm. These issues are addressed in a number of further papers [5], [6], [7], [8], [9], [10] - in Section II appropriate extensions to the algorithms for the underlying measurement problem are summarized.

The feasibility of the measurement method is verified by a detailed uncertainty evaluation. The standard tool for this, is the Guide to the Expression of Uncertainty in Measurement (GUM) [11]. The GUM itself, however, does not deal with complex valued measureands, but the associated Supplement 2 [12] gives an example how to treat complex values in rectangular form as a bivariate measurement model. In Section III we explain the uncertainty evaluation with the tool provided by the GUM Supplement 2 and an alternative way by separating the measurement problem into magnitude and phase and simply apply the procedures explained in the GUM. A comparison of the results and the final feasibility of the measurement method is given in Section IV.

II. Measurement method

Fig. 1 shows a block diagram of the measurement setup. The signal generator produces a sinusoidal voltage with a variable frequency f. Amplifiers $\underline{G}_1$ and $\underline{G}_2$ adjust the voltages to optimally utilize the oscilloscope. The blocks $\underline{H}_\mathrm{a}$ and $\underline{H}_\mathrm{b}$ model the internal signal paths of the oscilloscope. Thus the oscilloscope screen voltages v_a and v_b are not exact copies of the oscilloscope input voltages v_in and $v_\mathrm{out} \cdot \underline{G}_2$. The resulting measurement can be expressed by

$$\underline{V}_\mathrm{a}\big|_G = \underline{V}_\mathrm{in} \cdot \underline{H}_\mathrm{a}, \tag{1}$$

$$\underline{V}_\mathrm{b}\big|_G = \underline{V}_\mathrm{in} \cdot \underline{G} \cdot \underline{G}_2 \cdot \underline{H}_\mathrm{b}, \tag{2}$$

$$\underline{G}' = \left.\frac{\underline{V}_\mathrm{b}}{\underline{V}_\mathrm{a}}\right|_G = \frac{\underline{V}_\mathrm{in} \cdot \underline{G} \cdot \underline{G}_2 \cdot \underline{H}_\mathrm{b}}{\underline{V}_\mathrm{in} \cdot \underline{H}_\mathrm{a}} = \frac{\underline{G} \cdot \underline{G}_2 \cdot \underline{H}_\mathrm{b}}{\underline{H}_\mathrm{a}}, \tag{3}$$

where $\underline{G}'$ is the measurement of the frequency response $\underline{G}$, altered by $\underline{H}_\mathrm{a}$, $\underline{H}_\mathrm{b}$ and $\underline{G}_2$. The voltage phasors $\underline{V}_x$ are complex values for the corresponding time domain signals v_x, where the index $x = (a, b)$ denotes the oscilloscope channel. All values are a function of the frequency f; for better readability it is not specified in the formulas (e.g. $\underline{G} = \underline{G}(f)$).

Since the internal signal paths $\underline{H}_\mathrm{a}$ and $\underline{H}_\mathrm{b}$ of the oscilloscope as well as the frequency response of the amplifier $\underline{G}_2$ are unknown, the setup must be calibrated by first replacing the probe $\underline{G}$ with a reference attenuator $\underline{A}$. The reference attenuator is a resistive voltage divider, where a flat frequency response is guaranteed by the use of small valued surface-mount device (SMD) resistors. Thus, the divider can only be used for small signal calibration, but the influence of the parasitic elements can be neglected in the passband in contrast to the high resistance input stage of the high voltage differential probe. The resulting ac characteristic of the reference attenuator $\underline{A}_\mathrm{ac} = \underline{A}(f)/A(f = 0)$ is incorporated from a circuit analysis; the dc ratio $A_\mathrm{dc} = A(f = 0)$ is obtained by a dc ratio measurement with a multimeter. In the following, the frequency response of the reference attenuator is expressed by $\underline{A} = A_\mathrm{dc} \cdot \underline{A}_\mathrm{ac}$ and the calibration measurement is modeled by

$$\underline{A}' = \left.\frac{\underline{V}_\mathrm{b}}{\underline{V}_\mathrm{a}}\right|_A = \frac{\underline{A} \cdot \underline{G}_2 \cdot \underline{H}_\mathrm{b}}{\underline{H}_\mathrm{a}} = \frac{\underline{A}_\mathrm{ac} \cdot A_\mathrm{dc} \cdot \underline{G}_2 \cdot \underline{H}_\mathrm{b}}{\underline{H}_\mathrm{a}}. \tag{4}$$

Finally (3) and (4) are combined and the measurement result can be expressed in two ways

$$\mathrm{I}: \quad \underline{G} = \left.\frac{\underline{V}_\mathrm{b}}{\underline{V}_\mathrm{a}}\right|_G \cdot \left.\frac{\underline{V}_\mathrm{a}}{\underline{V}_\mathrm{b}}\right|_A \cdot \underline{A}_\mathrm{ac} \cdot A_\mathrm{dc}, \tag{5}$$

$$\mathrm{II}: \quad \underline{G} = \frac{\underline{G}' \cdot \underline{A}_\mathrm{ac} \cdot A_\mathrm{dc}}{\underline{A}'}. \tag{6}$$

It can be seen that the introduction of a calibration measurement by means of a reference attenuator effectively compensates the internal signal paths $\underline{H}_\mathrm{a}$ and $\underline{H}_\mathrm{b}$ of the oscilloscope as well as the influence of amplifier $\underline{G}_2$.

The time domain measurements for input and output are modeled by

$$v_x(t) = V_x \cos(2\pi f t + \phi_x) + V_{x,0} + w(t) \tag{7}$$

containing an additive white Gaussian measurement noise $w(t)$. The parameters for the magnitude V_x, phase ϕ_x and offset voltage $V_{x,0}$ are estimated by a least square algorithm [3], [4].

The least square fit can be done either for three or four parameters. If the frequency is known with an accuracy limit better than [5]

$$\Delta f < \frac{1}{2\pi}\sqrt{\frac{12}{\mathrm{SNR}\, N_s^3}}, \tag{8}$$

the three-parameter algorithm should be used. N_s denotes the number of samples; the signal-to-noise ratio (SNR) for sinusoidal signals is defined by $V_x^2/2\sigma_w^2$, where σ_w the is standard deviation of the measurement noise w. With our setup it is not possible to generate signals with a frequency accuracy smaller than the stated bound Δf, so the four-parameter algorithm has to be used. However, we are always measuring input and output signal simultaneously and the device under test is linear and time invariant (LTI). Thus it is not necessary to estimate the frequency for input and output separately. For this kind of application, the three- and four-parameter algorithms are extended to a seven-parameter algorithm [8], [13]. In the case of a high voltage differential probe, where there is a big ratio between input and output amplitude, a four-parameter algorithm applied to the data with the higher amplitude, followed by a three-parameter algorithm on the low amplitude data delivers results with same quality compared to the seven-parameter estimator [8].

Since the estimator is biased for the amplitude V_x, a permanent amplitude error of [9], [10]

$$\epsilon(V_x) = \frac{1}{2\, N_s\, \mathrm{SNR}} \tag{9}$$

is present. Thus, we suggest to choose the number of samples N_s large enough so that the bias can be neglected.

For the four-parameter algorithm, the choice of the initial frequency estimation is critical to the correct frequency estimation [6]. The IEEE standards suggest a DFT-based calculation or a time measurement between zero crossings. In our case, the best initial estimate is the desired output

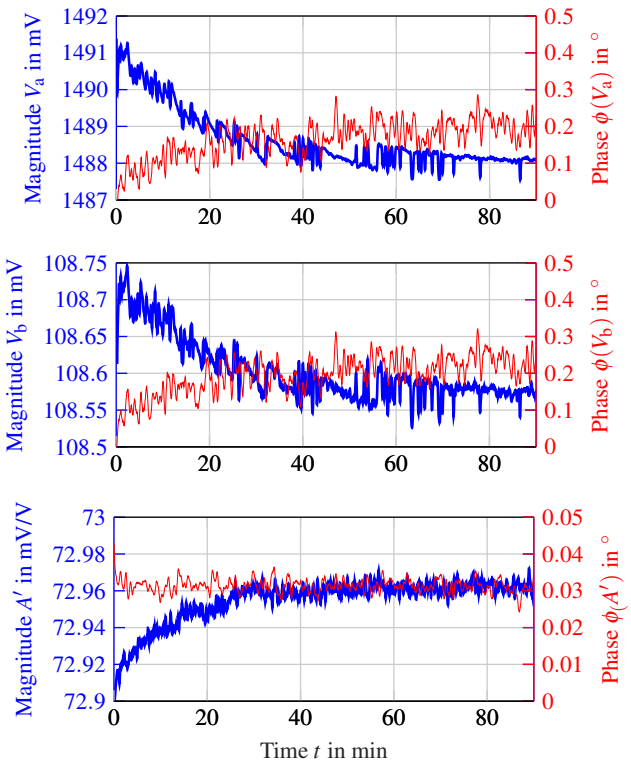

Figure 2. Input (top) and output (center) voltage measurement of the reference attenuator at $f = 1\,\mathrm{kHz}$ over time. The magnitude of the voltages show some recalibration artifacts. The resulting ratio (bottom) does not show the calibration artifacts but still has a remaining warm-up time with drifting magnitude.

frequency. Thus a very good starting value can be given without any computation.

Furthermore, the IEEE standards suggest a fixed number of six iterations for the four-parameter algorithm. This should be appropriate for most applications, but could be a waist of calculation time for applications with very good first estimates. Thus, we used the stop condition [7]

$$\frac{\Delta f_i}{f_i} < \frac{\sqrt{2}}{\pi\, 2^{N_b+2}}, \tag{10}$$

where Δf_i and f_i are the frequency correction term and the frequency estimate of the i-th iteration of the algorithm; N_b is the number of bits of the used oscilloscope.

III. Uncertainty Evaluation

Fig. 2 shows measurements of input and output voltages V_a and V_b of the reference attenuator at a signal frequency $f = 1\,\mathrm{kHz}$ over time. Some recalibration artifacts can be seen in the magnitude data, especially during warm-up. The artifacts occur on both channels simultaneously; a correlation analysis showed that the voltage signals are highly correlated. Thus a correlation therm has to be considered to calculate the combined uncertainty, when using expression (5). This is not required when using the latter expression (6), which only contains the resulting ratio measurements $\underline{G}'$ and $\underline{A}'$. An exemplary ratio measurement $\underline{A}'$ is shown in the bottom plot of Fig. 2; the data does not contain any calibration artifacts any more. After a warm-up time of half an hour the drift of the measured magnitude ends and the measurement data can be considered normally distributed.

Reporting a frequency response is commonly done in polar form, by means of magnitude and phase. However, if the *GUM uncertainty framework* (*GUF*) is applied on polar form measurement inputs, some problems caused by the scales of magnitude and phase may occur. The magnitude has a lower bound of zero; the phase has cyclical scale from $-\pi$ to π. Thus it is commonly recommended to do all uncertainty calculations in rectangular form, where the real and imaginary axis contain the whole set of real numbers [14]. After splitting the model into a real part and an imaginary part the *GUM uncertainty framework - Supplement 2* (*GUF S2*) can be applied. However, a calculation completely in polar form should be admissible, if the measurement input and output hold some constraints. As a consequence we will first show the uncertainty evaluation by applying the *GUF* to polar form data and then compare it to the commonly valid way of applying the *GUF S2* on the rectangular form data.

A. Uncertainty with GUF for polar form

Numerical analysis of the measurement data showed only weak correlation between magnitude and phase. So we propose to split (6) into two completely independent measurement problems - one for the magnitude and a second for the phase

$$y_1 = G = \frac{G' \cdot A_{\mathrm{ac}} \cdot A_{\mathrm{dc}}}{A'}, \tag{11}$$

$$y_2 = \phi = \phi(G') + \phi(A_{\mathrm{ac}}) - \phi(A'). \tag{12}$$

In order to apply the *GUF* to the polar form data, we must also ensure that the measurand is far from the origin, by means of

$$G \,/\, u(G) \gg 1 \tag{13}$$

and that all phase measurements are “unwrapped”, so that there are not phase jumps from $-\pi$ to π. The corresponding input uncertainties are then summarized by their covariance matrices

$$\boldsymbol{V}_{\boldsymbol{x},\mathbf{1}} = \mathrm{diag}\left[u^2(G') \quad u^2(A_{\mathrm{ac}}) \quad u^2(A_{\mathrm{dc}}) \quad u^2(A')\right], \tag{14}$$

$$\boldsymbol{V}_{\boldsymbol{x},\mathbf{2}} = \mathrm{diag}\left[u^2(\phi(G')) \quad u^2(\phi(A_{\mathrm{ac}})) \quad u^2(\phi(A'))\right]. \tag{15}$$

All Type A uncertainties $u(G')$, $u(\phi(G'))$, $u(A')$ and $u(\phi(A'))$ are defined by their experimental standard deviation of the mean. The dc ratio measurement and the ac frequency response flatness uncertainties of the reference attenuator are Type B uncertainties. Values for the dc ratio are taken from the multimeter datasheet; the datasheet values for “accuracy” are treated as worst case values $a(A_{\mathrm{dc}})$ with uniform distribution in-between, leading to $u(A_{\mathrm{dc}})$=$a(A_{\mathrm{dc}})/\sqrt{3}$. The uncertainty evaluation of the frequency response flatness of the reference attenuator is performed with a worst-case circuit analysis; the values are supposed uniform distributed between the worst

case simulation output, leading to $u(A_{\mathrm{ac}}) = a(A_{\mathrm{ac}})/\sqrt{3}$ and $u(\phi(A_{\mathrm{ac}})) = a(\phi(A_{\mathrm{ac}}))/\sqrt{3}$. The output uncertainties are then calculated by the law of propagation of uncertainties

$$u(G) = \sqrt{\boldsymbol{C_1}\,\boldsymbol{V_{x,1}}\,\boldsymbol{C_1}^{\mathrm{T}}} \quad \text{and} \quad u(\phi) = \sqrt{\boldsymbol{C_2}\,\boldsymbol{V_{x,2}}\,\boldsymbol{C_2}^{\mathrm{T}}}, \tag{16}$$

where the vectors

$$\boldsymbol{C_1} = \begin{bmatrix} \dfrac{\partial G}{\partial G'} & \dfrac{\partial G}{\partial A_{\mathrm{ac}}} & \dfrac{\partial G}{\partial A_{\mathrm{dc}}} & \dfrac{\partial G}{\partial A'} \end{bmatrix}, \tag{17}$$

$$\boldsymbol{C_2} = \begin{bmatrix} \dfrac{\partial \phi}{\partial \phi(G')} & \dfrac{\partial \phi}{\partial \phi(A_{\mathrm{ac}})} & \dfrac{\partial \phi}{\partial \phi(A')} \end{bmatrix}, \tag{18}$$

contain the sensitivity coefficients. Even though the calculation of of magnitude and phase uncertainty are done completely independent, one should use [15], [16]

$$k_{\mathrm{polar},p} = t_\nu(\sqrt{p}) \tag{19}$$

to calculate the coverage factor for an expanded uncertainty, where t_ν is the $100\sqrt{p}$-th percentile of the Student t-distribution with ν degrees of freedom, instead of the relation for the univariate case from the *GUF*. Thus the coverage probability of the two parameter problem is the product of the individual interval coverage probabilities. The degrees of freedom are calculated with the Welch-Satterthwaite formula [11, Annex G.4].

B. Uncertainty with GUF S2 for rectangular form

For the uncertainty calculation in rectangular form, the measurement model of (6) is rewritten to the bivariate form [17], [18]

$$\boldsymbol{y} = \boldsymbol{f}(\boldsymbol{x}), \tag{20}$$

where $\boldsymbol{x}$ and $\boldsymbol{y}$ are the input and result vectors

$$\boldsymbol{x} = [G_R \;\; G_I]^{\mathrm{T}} \tag{21}$$

$$\boldsymbol{y} = \left[G'_R \;\; G'_I \;\; A_{\mathrm{ac},R} \;\; A_{\mathrm{ac},I} \;\; A_{\mathrm{dc},R} \;\; A_{\mathrm{dc},I} \;\; A'_R \;\; A'_I\right]^{\mathrm{T}}. \tag{22}$$

Both contain the real parts of the corresponding input and output values (marked with index R), and the imaginary parts (marked with index I). The measurement function $\boldsymbol{f}$ is the split-up version of model (6) into a real and an imaginary part

$$\boldsymbol{f} = \begin{cases} f_R: & \Re(\underline{G}) \\ f_I: & \Im(\underline{G}) \end{cases}. \tag{23}$$

Subsequently, the law of propagation of uncertainties is performed with basic vector operations

$$\boldsymbol{V_y} = \boldsymbol{J}\,\boldsymbol{V_x}\,\boldsymbol{J}^{\mathrm{T}}, \tag{24}$$

where $\boldsymbol{V_y}$ is the 2×2 output covariance matrix, containing the the variance of real and imaginary part, and the associated covariances. The input covariance matrix $\boldsymbol{V_x}$ is a 8×8 diagonal matrix

$$\boldsymbol{V_x} = \mathrm{diag}\left[\boldsymbol{V}(G') \quad \boldsymbol{V}(A_{\mathrm{ac}}) \quad \boldsymbol{V}(A_{\mathrm{dc}}) \quad \boldsymbol{V}(A')\right] \tag{25}$$

with the 2×2 covariance matrices $\boldsymbol{V}(x)$ of the inputs in the main diagonal. The Type A uncertainties $\boldsymbol{V}(G')$ and $\boldsymbol{V}(A')$ are defined by their variances and covariances associated with the mean

$$\boldsymbol{V}(x)|_{\mathrm{Type\,A}} = \begin{bmatrix} u_R^2 & v_{R,I} \\ v_{R,I} & u_I^2 \end{bmatrix} = \begin{bmatrix} \sigma_R^2 & \sigma_{R,I} \\ \sigma_{R,I} & \sigma_I^2 \end{bmatrix} \frac{1}{M}, \tag{26}$$

where M is the number of measurements. The dc ratio measurement uncertainty $\boldsymbol{V}(A_{\mathrm{dc}})$ and the ac frequency response flatness uncertainty $\boldsymbol{V}(A_{\mathrm{ac}})$ of the reference attenuator are Type B evaluations. Both are supposed uniform distributed between their worst case values. Thus the covariance matrices for both Type B evaluations have the form

$$\boldsymbol{V}(x)|_{\mathrm{Type\,B}} = \begin{bmatrix} u_R^2 & v_{R,I} \\ v_{R,I} & u_I^2 \end{bmatrix} = \begin{bmatrix} a_R^2 & 0 \\ 0 & a_I^2 \end{bmatrix} \frac{1}{3}, \tag{27}$$

where a_R and a_I are the half-width boundaries of the uniform distributed inputs. Covariance entries are assumed to be zero for Type B evaluations. The matrix $\boldsymbol{J}$ is a 2×8 Jacobian of the form

$$\boldsymbol{J} = \begin{bmatrix} \dfrac{\partial f_R}{\partial G'_R} & \dfrac{\partial f_R}{\partial G'_I} & \dfrac{\partial f_R}{\partial A'_{\mathrm{ac},R}} & \cdots & \dfrac{\partial f_R}{\partial A'_I} \\ \dfrac{\partial f_I}{\partial G'_R} & \dfrac{\partial f_I}{\partial G'_I} & \dfrac{\partial f_I}{\partial A'_{\mathrm{ac},R}} & \cdots & \dfrac{\partial f_I}{\partial A'_R} \end{bmatrix}, \tag{28}$$

whose first line contains the derivatives of the real part of $\boldsymbol{f}$ to the real and imaginary part of $\boldsymbol{x}$ and the second line contains the derivatives of the imaginary part of $\boldsymbol{f}$ to the real and imaginary part of $\boldsymbol{x}$.

In the univariate measurement problem, the output uncertainty is reported as an interval around the mean on each side. For the complex valued, bivariate case, one may think of a two-dimensional region around the mean in the complex plane. Based on the assumption the data origins from a bivariate normal distribution, an ellipse best represents the two-dimensional region of uncertainty [14]. The coverage factor $k_{\mathrm{ell},p}$ for reporting an expanded uncertainty is calculated with

$$k_{\mathrm{ell},p} = \sqrt{\frac{2\nu}{\nu-1} F_{2,\nu-1}(p)}, \tag{29}$$

where $F_{2,\nu-1}(p)$ is the $100p$-th percentile of the F-distribution with two degrees of freedom in the numerator and $\nu-1$ degrees of freedom in the denominator. The degrees of freedom ν for the denominator are calculated by the method of *total variance*, explained in [19, Appendix 1].

For reporting the frequency response, values for magnitude and phase are of interest. Thus the result - including the uncertainty - is transformed to polar coordinates by using [12, Annex C]

$$G = \sqrt{G_R^2 + G_I^2} \quad \text{and} \quad \phi = \tan^{-1}(G_I/G_R), \tag{30}$$

$$u(G) = \sqrt{u_R^2\cos^2\phi + u_I^2\cos^2\phi + 2\,v_{R,I}\sin\phi\cos\phi}, \tag{31}$$

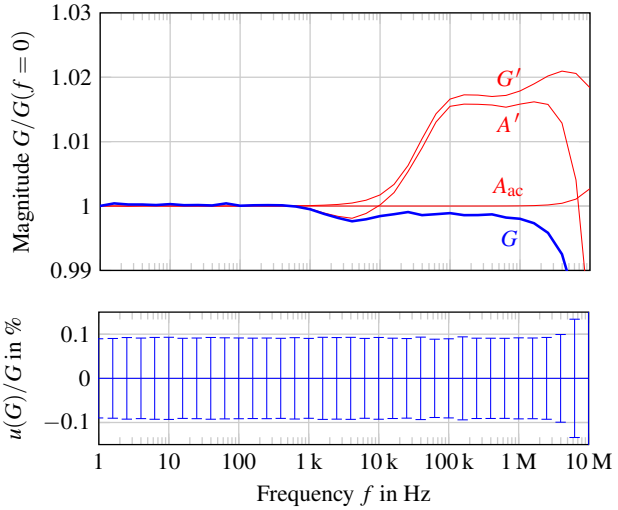

Figure 3. Normalized frequency response of the measurements of G', A', A_{ac} and the result G (top). The relative magnitude uncertainty is calculated for a 95 % confidence interval and $M = 100$ measurements (bottom).

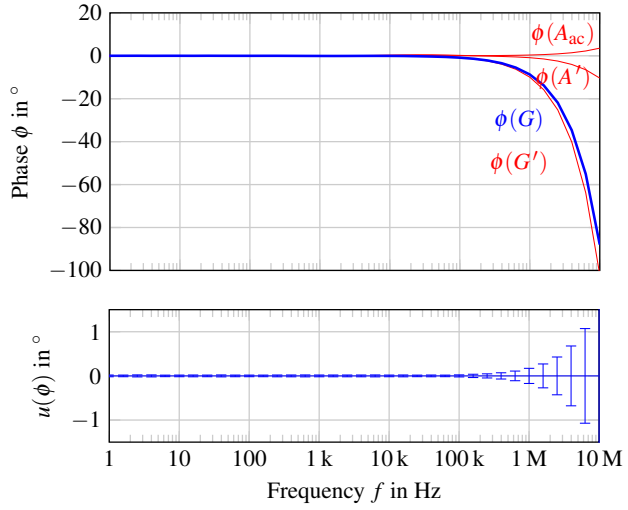

Figure 4. Measurement result for the phase measurement of the probe (top) with corresponding uncertainty for a 95 % confidence interval and $M = 100$ measurements (bottom).

$$u(\phi) = \sqrt{u_R^2 \sin^2\phi + u_I^2 \cos^2\phi - 2\,v_{R,I} \sin\phi\cos\phi}\,/\,G\,. \qquad (32)$$

To report an annular expanded uncertainty interval, magnitude and phase uncertainties are multiplied by the coverage factor $k_{\mathrm{polar},p}$ (19). The resulting annular section is only valid for measurands far from the origin (13), otherwise alternative shapes for uncertainty regions have to be considered [15].

IV. Measurement Result

The oscilloscope used for the measurements is a *Picoscope 5444B* USB oscilloscope with integrated arbitrary waveform generator (AWG). Oscilloscope measurements are done with $N_b = 15$ bit resolution and $N_s = 4096$ samples; the sampling rate f_s is adjusted so that at least five signal periods are sampled. The multimeter for the dc measurement of the reference attenuator is a *Tektronix/Keithley 2100* $6^1/_2$ - digit desk multimeter. The device under test is a high voltage differential probe with an attenuation of 1/150 [20].

Fig. 3 shows the frequency response measurements G', A', the reference attenuator flatness A_{ac} and the resulting frequency response G of the probe and the corresponding measurement uncertainty; curves of the measurements are normalized to their dc value for better comparison. Due to the different internal signal paths $\underline{H}_{\mathrm{a}}$ and $\underline{H}_{\mathrm{b}}$, the resulting measured frequency response G' can no longer be explained with a conventional pole/zero transfer function. It can be seen that the measured frequency response G' differs more than 1 % from the frequency response G of the probe at 100 kHz due to the internal signal paths of the oscilloscope. This approves the importance of the calibration measurement with the reference attenuator. Fig. 4 shows the resulting phase measurement. The uncertainty values in the figures are calculated with the *GUF S2* and $M = 100$ measurements. Tab. I gives a comparison between the uncertainty calculation methods *GUF* and *GUF S2* at different frequencies and for a different

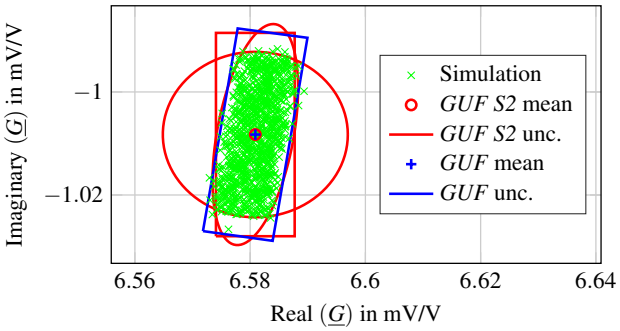

Figure 5. Simulation of the measurement process at a signal frequency of $f = 1$ MHz (green crosses), uncertainty region for the *GUF* method (blue) and different regions of uncertainty for the *GUF S2* method (red) for 95 % level of confidence.

number of measurements. It confirms that the results for both methods are very similar for the presented measurement problem. This can be confirmed by looking at the uncertainty regions in the complex pane. Fig. 5 shows a simulation of the measurement process, the annular uncertainty region defined by the *GUF* and different regions of uncertainty (ellipse, circle and rectangle according to [21]) for the *GUF S2* method. The best fitting region is the ellipse. However the annular region obtained with the *GUF* method perform quite similar in that case of measurement problem; due to the small uncertainty in phase the annular region might look like a rotated rectangle to the reader. Tab. I further shows the uncertainty budget by listing the coefficients of contribution [22]; coefficients of contribution greater than 30 % are marked in bold red. It can be observed that for frequencies below 1 MHz the Type B uncertainty of the A_{dc} measurement dominates the combined uncertainty; at higher frequencies the Type B uncertainty of A_{ac} dominates for high number of measurements. For a

Table I
MEASUREMENT RESULT AND UNCERTAINTY BUDGET

			GUF		*GUF S2*		Uncertainty budget for G				Uncertainty budget for ϕ		
f	G	ϕ	$\frac{u(G)}{G}$	$u(\phi)$	$\frac{u(G)}{G}$	$u(\phi)$	$h(G')$	$h(A_{\mathrm{ac}})$	$h(A_{\mathrm{dc}})$	$h(A')$	$h(G')$	$h(A_{\mathrm{ac}})$	$h(A')$
Hz	mV/V	°	%	°	%	°	%	%	%	%	%	%	%
						$M = 10$							
1 k	6.667	-0.093	0.12	0.073	0.14	0.073	**47.9**	0.0	**51.0**	1.1	**99.0**	0.0	1.0
10 k	6.668	-0.055	0.12	0.077	0.13	0.075	**42.1**	0.0	**57.1**	0.9	**99.1**	0.1	0.8
100 k	6.664	-0.833	0.15	0.060	0.14	0.052	**62.3**	0.0	**37.3**	0.4	**88.7**	10.7	0.6
1 M	6.668	-8.662	0.14	0.177	0.13	0.177	**57.2**	0.0	**42.0**	0.8	7.3	**92.7**	0.1
10 M	6.438	-87.949	0.28	1.692	0.24	1.697	15.0	**75.8**	9.1	0.1	0.2	**99.8**	0.0
						$M = 100$							
1 k	6.668	-0.075	0.09	0.020	0.09	0.020	10.8	0.0	**89.0**	0.1	**99.1**	0.0	0.9
10 k	6.660	-0.048	0.09	0.019	0.09	0.019	15.0	0.0	**84.8**	0.2	**98.3**	0.8	0.9
100 k	6.664	-0.833	0.09	0.023	0.09	0.023	9.2	0.0	**90.7**	0.1	**45.8**	**53.7**	0.6
1 M	6.658	-8.711	0.09	0.171	0.09	0.171	13.5	0.1	**86.3**	0.1	1.3	**98.7**	0.0
10 M	6.439	-87.972	0.26	1.690	0.22	1.696	2.3	**87.2**	10.5	0.0	0.0	**100.0**	0.0

lower number of measurements the Type A uncertainty of the G' measurement also gets relevant.

V. CONCLUSION

In this work we presented a passband frequency response measurement method of a high voltage differential probe. We showed the importance of a calibration measurement to compensate the limited dc accuracy and the internal signal paths of the oscilloscope. The resulting uncertainty is below 0.1 % for magnitude and smaller than 0.2 ° for phase up to 1 MHz for 100 measurements; the magnitude uncertainty drops to 0.15 % for the smaller number of 10 measurements. Since the Type B uncertainties of the multimeter for determining the dc ratio of the reference attenuator has a major contribution, the combined uncertainty may be significantly decreased by using a better multimeter. Further we compared two different methods for calculating the uncertainty. The results showed that the simple application of the *GUF* is valid for the underlying measurement problem.

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