Christoph Bauer, BSc

Studies on the Resistive Switching in Hybrid Organic/Inorganic Memory Elements

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Supervisor:

Ao.Univ.-Prof. Dipl.-Ing. Dr.techn. Emil List-Kratochvil

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Abstract

Memory and storage devices are key elements of today's information technology and play an essential role in emerging trends as well as technological developments associated with Industry 4.0, Big Data, Internet of Things, Cloud Computing and Smart Environments. Besides entrenched systems, upcoming new memory technologies are prepared to compete with today's leading memory technologies for a multi-billion dollar market. Organic memory systems are proven to be ready for mass production by roll-to-roll printing processes turning them into competitive players especially in low-price segments like packaging of perishable products, one-time-use medical products and disposable consumer goods. Besides the main advantage of cost effective high volume production by printing processes on virtually any substrate, organic memory elements also exhibit a long endurance comparable with storage systems.

However, the underlying physical mechanisms, which are responsible for unipolar and reversible resistance switching of such two-terminal hybrid organic/inorganic memory devices are still a matter of debate. Especially with regards to potential memory application and device performance optimization, a detailed understanding of the switching mechanism is of significant importance.

In order to address this issue, different types of I/V measurements are performed and combined to an overall picture to gain a deeper insight into the resistance switching processes. For this purpose, the device endurance, which is also a crucial parameter for reliable memory function, is investigated by a large number of switching operations performed by voltage pulses. In this context, it is shown that due to repeated switching the initially symmetric device characteristic evolves an asymmetric behavior which is indeed an inherent property of the investigated unipolar memory devices. Moreover, strong indications are presented that temperature triggered diffusion plays a significant role which is indicated by an accelerated evolution of the measured I/V characteristics.

Kurzfassung

Speichermedien bilden ein Kernelement der Informationstechnologie und spielen in Anwendungen, die unter Begriffen wie Industrie 4.0, Big Data, Internet of Things, Cloud Computing und Smart Environments zusammengefasst werden, eine wesentliche Rolle. Neben etablierten Systemen treten auch neue Speichertechnologien in den Wettbewerb um einen Multi-Milliarden Dollar Speichermedienmarkt ein. Organische Systeme stehen hierbei bereits an der Schwelle zur günstigen Massenproduktion mittels Roll-to-Roll Druckprozessen, durch die ein kompetitiver Mitbewerb im Niedrigpreissegment für Verpackungen verderblicher Ware, one-time-use medizinischen Produkten und Gebrauchsartikel möglich ist. Wesentliche Vorteile organischer Speichermedien sind neben einer kosteneffektiven Massenproduktion mittels Druckprozessen auf nahezu beliebigen Trägermaterialien auch eine mit Archivsystemen vergleichbare Datenbeständigkeit.

Die verantwortlichen physikalischen Mechanismen für unipolare und reversible Widerstandsänderungen von hybriden organischen/anorganischen Speicherelementen mit zwei Kontakten sind nach wie vor Gegenstand intensiver Diskussion. Insbesondere im Hinblick auf potentielle Speicheranwendungen und Leistungsoptimierung ist ein detailliertes Verständnis der zugrundeliegenden Speichermechanismen von signifikanter Bedeutung.

Hierfür werden unterschiedliche Strom- und Spannungsmessungen durchgeführt und die erhaltenen Resultate zu einem einheitlichen Bild vereint, um einen tieferen Einblick in die zugrundeliegenden Prozesse zu erlangen. Zu diesem Zweck, wird eine große Anzahl an Schreibvorgängen mittels Strompulsen durchgeführt und somit die Beständigkeit der hergestellten Speicherelemente untersucht. Dies ist insbesonders für potentielle Speicheranwendungen von signifikanter Bedeutung. Zusätzlich wird der Einfluss einer Vielzahl von Schreibvorgängen mittels Spannungssweeps auf die Kennlinie herausgearbeitet. In diesem Zusammenhang wird gezeigt, dass durch wiederholtes Schalten des Zustandes sich eine ursprünglich symmetrische Kennlinie asymmetrisch entwickeln und diese Asymmetrie in der Tat eine inhärente Eigenschaft der untersuchten unipolaren Speicherelemente ist. Außerdem werden starke Anzeichen dafür präsentiert, dass temperaturinduzierte Diffusion eine signifikante Rolle spielt und somit die Entwicklung und Form der gemessenen Kennlinien beeinflusst.

Abbreviations

BE Bottom Electrode

BL Bit Line

CD Compact Disc

CG Control Gate

CHE Channel Hot Electron

CMOS Complementary Metal Oxide Semiconductor

CPU Central Processing Unit

DRAM Dynamic Random Access Memory

DVD Digital Versatile Disc

FeRAM Ferroelectric Random Access Memory

FET Field Effect Transistor

FG Floating Gate

FL Free Layer

FN Fowler-Nordheim

HCl Hydrochloride Acid

HDD Hard Disk Drive

HRS High Resistive State

LCAO Linear Combination of Atomic Orbitals

LRS Low Resistive State

IML Intermediate Layer

IMS Intermediate States

MLC Multi Level Cell

MO Molecule Orbital

MRAM Magnetoresistive Random Access Memory

MTJ Magnetic Tunneling Junction

NDR Negative Differential Resistance

NP Nanoparticle

PANI Polyaniline

PCM Phase Change Material

PCRAM Phase Change Random Access Memory

PEO Polyethylene Oxide

PL Pinned Layer

PVC Polyvinylchlorid

SMU Source Measurement Unit

SRAM Static Random Access Memory

SSD Solid State Drive

STT Spin Transfer Torque

STT-MRAM Spin-Transfer Torque Magnetoresistive Random Access Memory

TE Top Electrode

USB Universal Serial Bus

VDU Vapor Deposition Unit

WL Word Line

Contents

1 Introduction and Scope of the Thesis

On November 17^{th}, 2014 IBM research announced on Twitter "By 2020, we will have generated 40 ZB (1 ZB = 10^{21} byte) of data. That's the number of stars in the universe." [1] All the data must be stored, their integrity must be secured and they must be kept available for further processing. Therefore, memory systems are an essential part of today's information technology, which is increasingly associated with upcoming keywords such as Industry 4.0 [2], Big Data [3], Internet of Things, Cloud Computing and Smart Environments [4]. Besides manufacturing and operating costs, technical and physical parameters such as retention time, endurance and the time required to fetch a random bit are just as important. Unfortunately, the holy grail of memory technology has not been invented so far despite of considerable efforts made by numerous academic and economic research facilities. As a result, a memory architecture has been used, which combines the advantages of available technologies in such a way that an optimal performance can be achieved at minimum costs. Today's leading technologies are the static and dynamic random access memory (SRAM and DRAM), the flash memory and the hard disk drive (HDD). A detailed explanation as well as a comparison of characteristic parameters is given in the first part of Chapter 2.

"Tape is dead, Disk is tape, flash is disk, RAM locality is king", was proclaimed by Jim Gray in Redmond in December 2006 [5] and it is just a matter of time when today's leading memory technologies are going to be replaced by upcoming memory technologies such as phase change random access memory (PCRAM), spin-transfer torque magnetoresistive random access memory (STT-MRAM), ferroelectric random access memory (FeRAM) and the Memristor (see second part of Chapter 2). Especially, the Memristor has the potential to revolutionize memory technology and was originally conceived by Leon Chua in 1971.[6] Stanley Williams et al. were the first to experimentally demonstrate the Memristor in 2008 and also elaborated that memristive behavior is a property of nanoscaled devices and plays an increasingly important role with proceeding down-

scaling.[7] Furthermore, organic memory systems based on ferroelectric compounds and fabricated by roll-to-roll printing process are ready for cheap mass production as well as for the Internet of things.[8]

With regards to potential memory applications, a detailed understanding of the underlying physical mechanisms responsible for reversible resistance switching of organic memory devices is of significant importance, whereby the focus of this work is on two terminal and unipolar hybrid/organic inorganic memory elements which are capable for reversible resistance switching. Their device structures and device characteristics are introduced in Chapter 3. The fabricated prototypes exhibited a sandwich structure corresponding to a capacitor where the two electrodes are separated by one (single layer device) or more layers (multilayer device) of organic compounds which could also exhibit incorporated aluminum oxide shell nanoparticles. Nevertheless, independent of the switching mechanism, the devices must comply with the fundamental charge transport properties of organic devices which are also discussed in Chapter 3.

The resulting unipolar device characteristics exhibit three essential features. First, the continuous range of non-volatile resistance states is limited by two boundary states denoted as high resistance state (HRS) and low resistance state (LRS). Second, state transitions from HRS into LRS are triggered similarly to PCRAM at a certain threshold voltage and, last but not least, the unipolar device characteristic exhibits a negative differential resistance range (NDR) in which programming operations are performed. The term unipolar indicates that the switching ability of the memory device depends only on the bias voltage amplitude and is independent of the bias voltage polarity. Possible explanations for such behavior are based on filamentary conduction and are also discussed in Chapter 3.

Chapter 4 deals with the fabrication and characterization of the investigated memory device structures within an argon atmosphere glove box cluster. Different approaches for resistance switching by current/voltage measurements are presented and are combined in order to get a better understanding of the switching behavior. Additionally, the preconditioning as well as device initialization is explained.

In Chapter 5, obtained experimental results are discussed in detail in order to examine the underlying physical mechanism responsible for reversible resistance switching. For this purpose, measured current/voltage characteristics of various types of single- and multilayer devices are compared and screened for commonalities and differences. First, different programming techniques are introduced and their advantages and disadvantages are explained. Particularly with regard to potential memory applications, endurance is

of significant importance. Therefore, the influence of a large number of switching cycles is also investigated. Related experiments are denoted as long term measurements and also include measurements which are based on the application of a specific bias voltage for a relatively long period. Besides repeated switching of the memory element state, the device response to high electric fields is subject of closer examination. Supplementary investigations are performed with memory elements which undergo a temperature treatment right after fabrication. Last but not least, the introduced memory device structures are compared and screened for commonalities and differences.

Obtained results are summarized and conclusions concerning the underlying physical switching mechanism are drawn in Chapter 6.

2 Memory Technologies

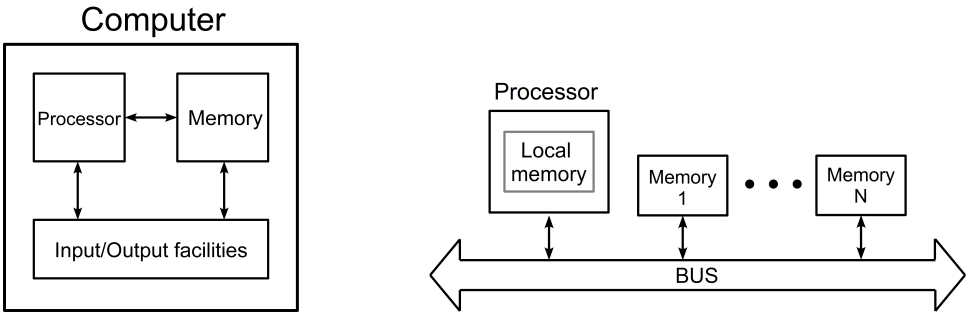
2.1 Computer Architecture

Computer architecture shows how a computer system is organized, specifies functionality of the different components, and determines their interconnection. Most of today's computer systems are based on the Von Neumann architecture (Figure 1a), which uses a stored program approach in which a program resides in memory. The three main components of a computer system are *input/output facilities*, *processor*, and *memory*. Communication between the single components takes place via a bus system and is based on the fetch-store paradigm. This criterion allows to perform either a fetch (read) or a store (write) operation between only two devices, e.g. processor and memory, at the same time. The time spent to fetch data or instructions from a memory device via memory bus (Figure 1b) is the most time-consuming operation and limits the overall system performance. This phenomenon is called Von Neumann bottleneck and can be encountered by providing a local memory (cache memory) located directly in the processor in order to reduce communication via bus system. Increasing the cache memory, which means increasing the occupied space, is still the standard solution to reduce limitations due to Von Neumann bottleneck.[9, 10]

Input facilities like keyboard, mouse, camera, and scanner provide information for the computing system, whereas output facilities such as screen, printer, and audio speakers are responsible to communicate the computed information to the outside world. Storage media like hard disk drive (HDD), solid state drive (SSD), compact disc (CD), digital versatile disc (DVD) or universal serial bus (USB) flash drive are also accessed by input/output facilities.

Processor, often denoted synonymously with Central Processing Unit (CPU), is a digital device that performs computations by carrying out instructions of the program.

The memory of a computer system stores data, program and computed results. An ideal memory device fulfills several technical requirements, namely, it exhibits a high data density, stores data non-volatile, fetches information fast (high speed) in order to



(a) *Von Neumann architecture* ***(b)*** *Memory bus system*

Figure 1: *Scheme of Von Neumann architecture with the main components: input/output facilities, processor, memory and memory bus system, which connects processor with a number of N memory devices. Taken and modified from [9].*

encounter the Von Neumann bottleneck and preferably has a low power consumption. Yet, none of today's leading memory technologies (Chapter 2.3) are capable to achieve all these requirements at once. Consequently, a compromise must be made by introducing a hierarchic memory system, which combines the advantages of today's leading memory technologies (baseline technologies). The main focus is on optimizing the performance of the memory system from an economic point of view (best performance at given costs). As a result, the memory system consists of a fast but expensive primary storage, a slower but larger secondary storage, and an extraordinary large but relatively slow tertiary storage.

- *primary storage* also called memory consists of the local memory in the processor and the main memory which is directly accessed via the memory bus system (Figure 1b).

  The local memory of the processor is based on static random access memories (SRAM). Due to the fact that SRAM requires relatively much space, it is expensive and the overall local memory space is limited to few megabyte (MB) these days. For instance, the CPU *Intel© Core™ i7-4500U* exhibits three local memories denoted as L1-Cache, L2-Cache and L3-Cache with a memory space of 128 KB, 512 KB and 4 MB, respectively. Time to get data from L2-Cache is generally below 5 ns, whereas a processor operation takes about 1 ns.[11]

  Main memory uses dynamic random access memories (DRAM), which are slower in comparison to SRAM but cheaper in production. The memory space of a single main memory module is in the gigabyte (GB) range nowadays. It takes about 60 ns [11] to fetch data from DRAM.

- *Secondary storage* is usually provided by HDD or SSD, which can store a much higher amount of information in the low terabyte (TB) range. Access takes place via input/output facilities.

- *Tertiary storage* is used as archival to store an extraordinary amount of data on e.g. magnet tapes at relatively low costs. Sony Corporation ("Sony") successfully developed magnetic tape technology that achieves an areal recording density for tape storage media of 148 Gb/in^2 (gigabits per square inch), which means that 185 TB of data can be stored per data cartridge.[12] Time to get data from tape is about 40 s.[11]

There is no clear distinction between memory and storage, but the term memory is generally associated with technologies that exhibit primary fast access times whereas the main focus of storage is on storing information non-volatile and providing a high data capacity at low costs. A future memory technology, which has the ability to meet all requirements of an ideal memory, i.e. high data density, non-volatile, and high speed, will introduce a new class of memory system - a storage class memory that will revolutionize modern computer architecture.[10]

2.2 Memory Cell

A basic design feature of each memory technology is the memory cell, which stores information in form of a data bit (0-bit or 1-bit). It can be realized in different ways, but each memory cell must fulfill the following basic requirements [13] independent of the used technology:

- Each memory cell must possess at least two metastable states, which are associated with the 0-bit and 1-bit.
- The state of a memory cell can be switched by an external stimulus in order to write or erase information.
- Different states of a memory cell can be clearly distinguished during readout.

A memory cell can be characterized by following parameters:

- *Feature Size F* is the smallest producible structure due to technical limitations of the lithographic process.

- *Cell Area* is the required floor space of one memory cell. It is expressed as a multiple of feature size F squared.

- *Read Time* indicates how long it takes to read a memory cell, which means determining its state and obtaining the stored information.

- *Write/Erase Time* indicates how long it takes to write/erase a data bit, which corresponds to switching the state of the memory cell from 0 to 1 and vice versa.

- *Retention time* indicates how long a memory cell can store a data bit until information loss occurs - a not intended state change.

- *Write Cycles* gives the minimum number of write and erase operations that can be performed until the bit cell is unusable (endurance).

- *Write/Read operation voltage* is applied to memory cell to write/read a data bit.

- *Write energy (J/bit)* is the amount of energy needed to write a data bit.

- *Volatile* memory technologies need power supply in order to retain or to refresh the stored information. On contrary, *non-volatile* technologies retain information without power supply at least ten years.[14]

- *random or serial access* characterize how memory cells of a memory are accessed. Random access allows to read any memory cell independent from its position in the memory array at any time. This can be realized by a crossbar array (Figure 2), where one memory cell is located at each intersection of the bars. Serial access only allows to read data in the same sequence as they were stored in the memory. Thereby, the access time depends on the memory cells position and is on average much longer than compared to random access.

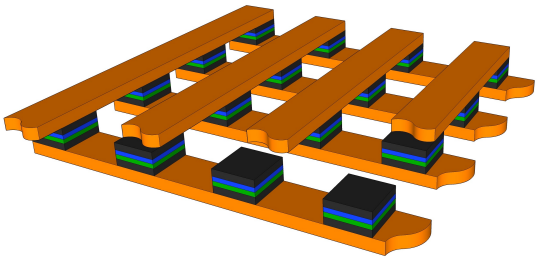


Figure 2: *Crossbar array with one memory cell at each intersection.*

2.3 Today's Leading Memory Technologies

Varieties of different memory technologies have been developed until now, but only a manageable number had the potential to satisfy mass marked needs and form today's leading memory technologies. Hence, they are an integral part of modern information technology and of course in people's everyday lives. The underlying mechanisms are based on charge storage, charge transport, and the magnetization of ferromagnetic materials in magnetic field. Although, each of today's leading memory technology has been developed continuously over years or even decades, none of them can be considered as an ideal memory system. The operation principle of the memory cell of SRAM, DRAM, flash, and HDD will be discussed in detail in the following section. If not stated otherwise, values for characteristic parameters are taken from [15] and are also listed in table 1 for comparison.

2.3.1 Static Random Access Memory

Static random access memory (SRAM) stores information in bistable latch-circuits also known as flip-flops. Each flip-flop consists of four transistors (T1-T4), stores one bit and is integrated in a crossbar array in order to permit random access. Two additional access transistors (T5, T6) per memory cell are necessary to select a specific memory cell by the corresponding word line (WL) and bit lines (BL & $\overline{BL}$). The information, 0-bit or 1-bit, is stored at Q (see Figure 3). $\overline{Q}$ is the logical negation of Q.

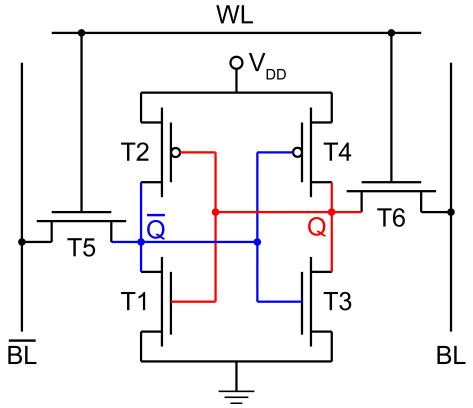


Figure 3: *Schematic circuit of a 6-transistor (T1-T6) latch-type memory cell. The information is stored in Q and $\overline{Q}$.*

A read operation is performed by applying a high-signal on the word line (WL). As a result, transistor T5 and T6 are switched on and the values of Q and $\overline{Q}$ are transferred to BL and $\overline{BL}$, respectively, which is sensed by a read-write amplifier. A write operation is performed by applying the corresponding 0 or 1 signal on BL and the inverted signal on $\overline{BL}$. After switching on T5 and T6 the flip-flop is forced to store the desired value, independent of the previous state by a read-write amplifier which is more powerful than the transistors of the memory cell and can therefore overwrite the stored information.[16]

As long as power supply is available, the stored data bit is preserved. The term *static* is derived from this property. Consequently, any loss of power causes an instantaneous data loss. Therefore, SRAM is regarded as volatile.

2.3.2 Dynamic Random Access Memory

The memory cell of a dynamic random access memory (DRAM) consists of one pass transistor and one capacitor (1T1C). Standard complementary metal-oxide-semiconductor (CMOS) technology and standard photolithography is used for fabrication. A schematic circuit is shown in Figure 1. The memory cells are integrated in a crossbar array, in which each memory cell can be accessed randomly by selecting the corresponding WL and BL. The WL controls the pass transistor that is turned on only if the WL is raised to high potential, otherwise it is turned off. The capacitor is connected through the pass transistor to the BL. A charged capacitor is associated with the 1-bit, whereas an uncharged one represents a 0-bit. Performing read and write operations requires different bias voltages denoted as V_{read} and V_{write}, respectively.[16, 17]

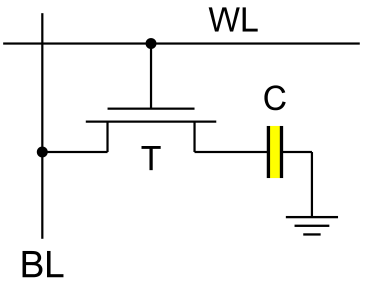


Figure 4: *Scheme of the DRAM bit cell with pass transistor T, capacitor C, and access lines.*

A write operation is performed by switching on the pass transistor first. In order to write a 1-bit, the capacitor is charged through the pass transistor with V_{write}, whereas discharging the capacitor stores a 0-bit. Switching off the pass transistor completes the write process.[16]

In order to perform a read operation, the BL is charged with V_{read} and disconnected from the charging circuit (BL is floating). Switching on the pass transistor connects the charged/uncharged capacitor with the precharged BL. Due to the fact that $0 < V_{read} < V_{write}$ the potential of BL rises, if a 1-bit was stored, and drops in case of a 0-bit. Independent of its previous state, the capacitor is not in a defined state any more when a read operation was performed. This is called a destructive read out and, consequently, the initial bit must be rewritten to maintain the original information.[16]

The main disadvantage of DRAM is its limited retention time. The capacitor discharges mainly over junction leakage due to lateral electric field near the storage node and gate induced drain leakage.[18] Consequently, data is stored volatile and in order to avoid data loss, the memory cell must be refreshed (rewritten) periodically after a period of 64 ms.[15] This behavior is indicated by the term *dynamic*.

2.3.3 Flash Memory

A flash memory cell is realized by a double gate transistor, which consists of a control gate (CG) and a floating gate (FG). The CG is the equivalent to the field effect transistor gate and controls the source-drain current. If the threshold voltage V_T is applied to the CG, a conductive channel between source and drain is formed and the transistor gets conductive. The gate oxide and tunneling oxide isolates the FG electrically (see Figure 5). Hence, electron charge can be trapped on it. A negatively charged FG is the equivalent of a 0-bit and an electrically neutral or positively [14] charged FG is associated with a 1-bit. The potential of trapped electron charge Q screens the gate voltage and, as a result, V_T is increased proportionally to Q by a ΔV_T.[14, 17] Trapping different amounts of charge allows to store more than one bit in a flesh memory multi level cell (MLC).

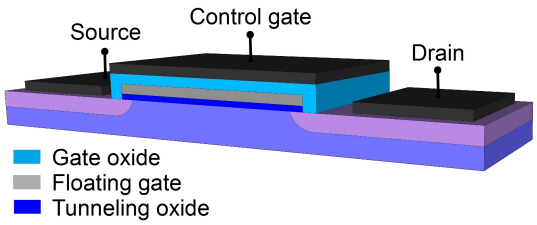


Figure 5: *Scheme of a double gate transistor with control gate and isolated floating gate.*

A reading operation is performed by applying a read voltage V_R, which must be within the range from V_T to $V_T + \Delta V_T$, to CG and measuring the source-drain current. If the FG is uncharged, then $V_R > V_T$ and, as a result, a relatively high source-drain current indicates a 1-bit. On the other hand, a 0-bit is given by zero current within the same order of magnitude, because $V_R < V_T$ due to trapped electron charge in the FG.[14]

A 0-bit is stored by performing a write operation. Here, the double gate transistor is switched on and a source-drain voltage is applied. In the electric field along the conductive channel, some electrons gain enough energy to overcome the potential barrier of the tunneling oxide and charge the FG. This process is also known as channel hot electron (CHE) mechanism. In order to store a 1-bit, the memory cell must be erased. In this context, the FG is discharged by Foler-Nordheim (FN) electron tunneling. For this purpose, a positive bias voltage is applied on bulk and a negative bias voltage on the control gate. As a result, a high electric field across the tunneling oxide in the range of 8 - 10 MV/cm is formed, which cause the trapped electrons to tunnel through the potential barrier and discharge the FG. FN tunneling can also be used to store a 0-bit by inverting the bias voltage polarity.[14]

The retention time of flash memory is stated with 10 y in [15]. Oxide stress due to high electric fields during the erase operation can cause defects in the tunneling and/or gate oxide, which lead to charge loss.[14] Consequently, the endurance of a bit cell is limited and stated with 10^5 write cycles .[15]

2.3.4 Hard Disk Drive

Hard Disk Drive (HDD) stores information by magnetizing magnetic domains, which are located on a spinning disk and are the equivalent of the memory cell. The magnetization results from the collective parallel alignment of electron spins in ferroelectric materials. In order to perform a write operation, the magnetization can be orientated up or down (↑|↓) by the magnetic field of a coil (see Figure 6). These two orientations represent the 0-bit or 1-bit, respectively. A reading head is located above the bit cells in order to read the stored information. The main component of the reading head is a nanostructured multilayer that is sensitive to the magnetization of the bit cell located just below. This multilayer consists of a ferromagnetic free layer (FL) and a ferromagnetic pinned layer (PL) separated by a non-magnetic metal layer, which acts as tunneling junction (see Figure 9). The magnetic field of the memory cell aligns the magnetization of the FL parallel to its own, but has no influence on the fixed magnetization of PL. Consequently, the magnetization of FL and PL can either be parallel or anti-parallel, which has a significant influence on the electrical resistance of the reading head. This phenomenon is known as giant magneto resistance and bases on spin dependent electron scattering. If the alignment is parallel, the reading head has a low resistance, otherwise resistance increases sharply.[17, 19]

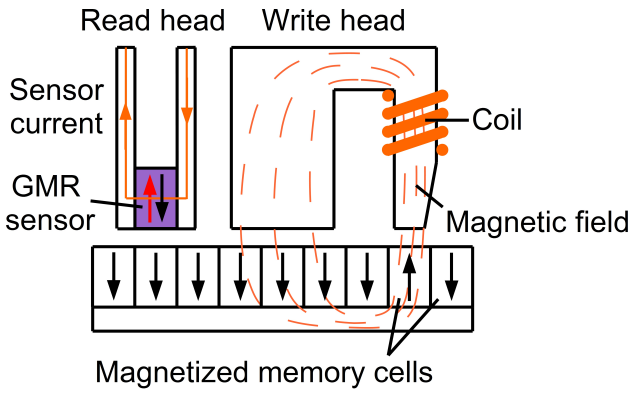


Figure 6: *Scheme of a HDD with read head, write head and longitudinally magnetized memory cells.*

The main advantage of HDD is that it stores information non-volatile and exhibits a high data density by scaling magnetic domain dimension in the nanometers range.[17] On the contrary, information is accessed serially, which is relatively slow compared to technologies basing on parallel access. Furthermore, mechanically moving parts are necessary.

2.3.5 Conclusion

A direct comparison of the characteristics of today's leading memory technologies makes the necessity of a memory hierarchy evident, which provides data for the computing system as quick as possible from an economic point of view. Memory technologies basing

on parallel access like SRAM and DRAM exhibit fast read times independent of the bit cell position in the memory array. The read time of SRAM is stated with 0.2 ns [15] and surpasses therefore DRAM (<10 ns) by one order of magnitude. On the contrary, reading data from flash and HDD takes $\sim$ 0.1 ms and 3 - 10 ms, respectively. The main reasons for the relatively long read times are that their memory cells are combined to larger units (pages or sectors) of 512 bytes or more, which must be accessed first and are read out at once. Write and erase times are equal to the corresponding read times with the exception of flash memory. Its erase time is stated with $\sim$ 1 ms.

The period, after which information loss occurs is referred to as retention time. If it is less than ten years, then the corresponding memory technology is designated as volatile, otherwise it is considered as non-volatile like flash, HDD and tape. SRAM and DRAM are volatile due to the fact that former loses information instantaneously after losing power supply and DRAM looses the stored data due to not preventable discharging of the capacitor. DRAM exhibit a retention time of 64 ms. Therefore, DRAM must be rewritten periodically. This issue has an important influence on the power consumption, e.g. Google [20] reports that even an energy-optimized server requires more than 50% power compared to peak power consumption even at very low utilization levels.

Another important aspect are manufacturing costs of a memory cell, which are proportional to the occupied floor space and amounts to $\sim 0.1 - 1$, 2, and 10 $\$/GB$ for HDD, flash, and DRAM, respectively. The required cell area of a single memory cell is expressed as multiple of the minimum feature size (F) squared. Flash has already reached the minimum possible cell area of $4F^2$. DRAM occupies a cell area of $6F^2$, but is also expected to reach $4F^2$ until 2026.[15] The occupied floor space of the SRAM memory cell is $140F^2$ and influences the manufacturing costs correspondingly. In case of HDD and tape the required memory space is expressed in bits per inch squared ($bit/inch^2$). On March 19, 2012 Seagate reported that the milestone of one terabit per square inch was reached by Heat-Assisted Magnetic Recording.[21]. Flash also offers the possibility to store two or more bits per memory cell (Multi Level Cell) by trapping different amounts of electron charge in FG.[22]

Furthermore, the endurance is an important parameter in economic point of view, which is specified as the minimum number of how often a bit cell can be repeatedly erased and rewritten (write cycles). In this context, SRAM and DRAM overcome more than 10^{16} write cycles and outperform therefore flash (10^5 write cycles) by far. Nonetheless, flash started to replace HDD. Main disadvantages of the HDD are that the mechanically moving parts e.g. the bearing can wear out or the read head, which flies just tens of

nanometer above the magnetic domains, can crash into them. Furthermore, it needs power supply to keep the spinning platter rotating at 10.000 rotations per minute.

An ideal memory cell must fulfill several requirements, namely: fast read-, write-, and erase-times, non-volatile behavior, low costs, low power consumption and high endurance. However, none of today's leading memory technologies are capable to fulfill all this requirements at once. The SRAM is non-volatile and expensive, DRAM is non-volatile too and has a high power consumption, flash exhibits a low endurance and is relatively slow and, last but not least, the HDD, which is slow and has a high power consumption. The disadvantages are related to the underlying physical processes as well as the construction of the memory cell and cannot be overcome by a further down scaling process. Hence, new approaches must be found, which are discussed in the following chapter.

2.4 Upcoming Memory Technologies

Today's leading memory technologies base on storing electric charge and its interactions with the electric field. However, considering upcoming magnetoresistive memory technologies a change in paradigm takes place. Here, a second important electron property besides the electron charge is used to store information, namely the electron spin. Such technologies are grouped under the term spintronics.

Promising new technologies are resistance switching memory devices which store information by different resistance states of the memory cell e.g. phase change memories. Replacing the dielectric material of a DRAM capacitor with a ferroelectric material also offers promising alternatives for non-volatile memory technologies.

Moreover, downscaling offers insight into the intrinsic nature of resistance switching devices and reveals unique behaviours that requires to introduce the 4^{th} fundamental, non-volatile and passive circuit element – the memristor, which claims to be the holy grail of memory technology and has indeed the potential to succeed.

2.4.1 Ferroelectric Random Access Memory

Ferroelectric random access memory (FeRAM) cells store data by polarizing ferroelectric materials in an electric field. The construction of the memory cell is similar to a DRAM (Chapter 2.3.2), but exhibit a bistable ferroelectric capacitor and an additional contact line denoted as plate line besides the mandatory BL and WL (see Figure 7). The core element of the memory cell is the ferroelectric perovskite $PbZr_{1-x}Ti_xO_3$ (PZT). This material features due to its crystal structure a semi-permanent electrical dipole which is aligned by the internal electric field of the capacitor. The two possible orientations, up and down, are associated with the 0-bit and 1-bit, respectively. The alignment of the dipoles is preserved at zero electric field and causes a remanent polarization. As a result, mobile electron charges are stored non-volatile on the capacitor plates in order to compensate the net polarization.[23]

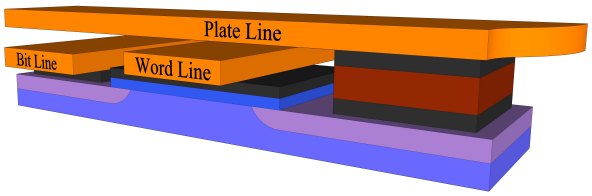


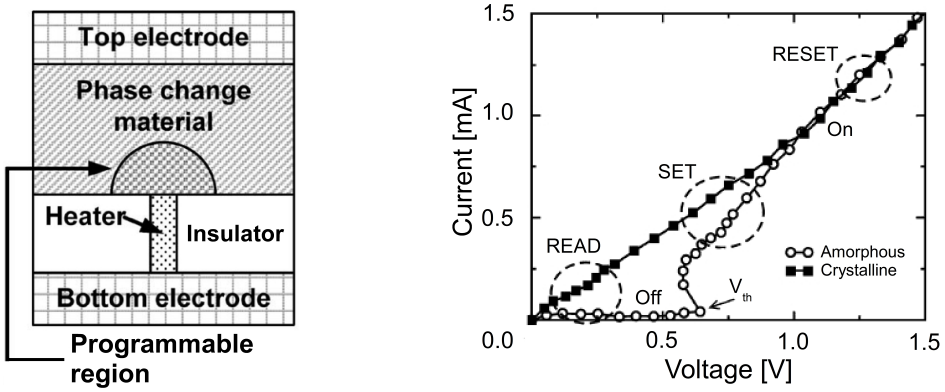
Figure 7: *Scheme of a FeRAM memory cell with access transistor, contact lines and ferroelectric capacitor.*

A 0-bit is stored by switching on the access transistor, applying a positive bias voltage on the plate line and grounding the BL. As a result, the capacitor plate, which is connected through the access transistor to the BL, is negatively charged. In order to store a 1-bit, the same procedure is conducted by applying a negative bias voltage polarity on the plate line. A read operation is performed by floating the bit line, switching on the access transistor and applying a positive bias voltage on the plate line likewise writing a 0-bit. In case of a stored 1-bit, the electric dipoles are realigned whereas in case of a 0-bit the dipole alignment remains as it is. As a consequence of the reorientation, the capacitor plates are first discharged and then recharged again with inverted polarity. The resulting change of the bit line potential indicates a 1-bit, whereas no change is associated with a 0-bit. After a read operation, the bit cell always stores a 0-bit regardless of the previous state. This is called a destructive read out. Consequently, the data must be rewritten in order to retain the stored information.[17]

The FeRAM memory cell exhibit a retention time of 10 years due to its ferroelectric capacitor and is therefore non-volatile in contrast to DRAM.[15] Furthermore, it exhibits a read time of 40 ns and an endurance of 10^{14} write cycles. Hence, it cannot compete with DRAM, but it is a possible candidate to replace flash if its minimum feature size of 180 nm [15] and the occupied cell area of $22\,F^2$ [15] can be reduced further in future. Possible applications are RFID systems, ID cards and other embedded applications.[24]

2.4.2 Phase Change Random Access Memory

Phase change random access memories (PCRAM) are based on a two-terminal memory cell which consists of a phase change material (PCM) and a heater embedded into an insulator (see Figure 8a). PCMs such as $Ge_2Sb_2Te_5$ (GST) or Ag- and In-doped Sb_2Te (AIST) can exhibit a high resistive amorphous and a low resistive crystalline phase which correspond to a off- and on-state of the memory cell, respectively. The phase transitions take place close to the heater in the programmable region and depend on the applied bias voltage. The two contact electrodes are denoted as top and bottom electrode.[25]



(a) *PCRAM crossection* ***(b)*** *I-V Characterisitc*

Figure 8: *(a) Schematic cross section of a PCRAM memory cell and (b) corresponding I/V characteristic of one switching cycle. Taken and modified from [25].*

Assuming the memory cell is in an off-state. The application of a set bias voltage leads to a crystallization of the amorphous phase due to heating what results in an increase of the device current (on-state). This process also requires a minimum electric field strength indicated by the threshold voltage V_{th} (see Figure 8b). In order to reset the memory device, the PCM is locally melted by a short reset voltage pulse and quenched subsequently. As a result, the programmable region exhibit again an amorphous phase (off-state). Typical melting temperatures are in the range from 500 °C to 700 °C.[25] Low and high read currents indicate off- and on-states and are referred to as 0-bit or 1-bit, respectively.

The device structure of a PCRAM memory cell requires a cell area of $4\,F^2$, is likewise flash capable of MLC and stores data non-volatile with a retention time longer than 10 years. It exhibits a unipolar device characteristic which allows to switch the device state independently of the bias voltage polarity. Main disadvantages are a relatively long set time of 100 ns and the necessity of a high current to reset the memory element.[15, 24, 26]

2.4.3 Magnetoresistive Random Access Memory

The core element of a magnetoresistive random access memory (MRAM) is a magnetic tunneling junction (MTJ), which forms the memory cell together with an access transistor (see Figure 9). The working principle of a MTJ is similar to the HDD read head. It is composed of three nanostructured layers: a ferromagnetic free layer (FL), a ferromagnetic pinned layer (PL) and a non-magnetic isolating spacer layer that consists of e.g. Al_2O_3 or MgO [19].

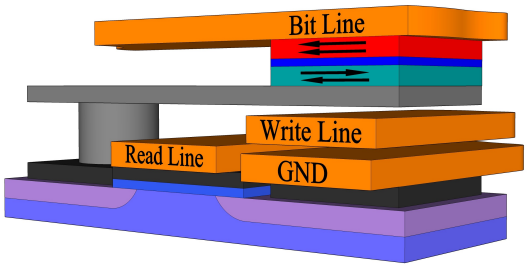


Figure 9: *Schematic illustration of MRAM cell with the MTJ located at the intersection of BL and WL.*

The data bit is stored by different resistance values of the MTJ which depend on the relative alignment of the FL and PL magnetization. Here, the separating layer between FL and PL acts as a tunneling junction through which electron transport occurs with electron spin conservation. The change in magnetoresistance is more than one order of magnitude higher than compared to the GMR effect.[27] In addition to the WL and BL, a write line is required too.[17]

A write operation is performed by adjusting the magnetic moment of the FL with the cumulative magnetic field caused by currents flowing through the BL and the write line. In order to read the stored information, the access transistor is switched on and the current through the MTJ is measured. If the magnetization of FL and PL is parallel aligned, then the memory cell exhibits a low electrical resistance. The resulting high current is associated with a 0-bit. On the contrary, a high electrical resistance due to an anti-parallel alignment causes a low current which indicates a 1-bit.[17]

MRAM stores data non-volatile and exhibits read and write times as low as 5 ns. Therefore, it has the potential to replace DRAM as well as Flash and can also compete against PCRAM as well as FeRAM. The main disadvantage of this type of memory cell is its limited down scaling ability due to large stray fields which influence adjacent memory cells. Furthermore, a high writing current around 10 mA is needed. However, the current density of contact lines is limited to $10^7\,\mathrm{Acm}^{-2}$ due to electromigration.[19]

A possibility to overcome these limitations is based on spin-transfer torque (STT) writing. Thereby, the FL is aligned by a spin-polarized current due to spin angular momentum transfer. The construction of the memory cell corresponds to a MTJ with a thick PL and a thin FL. In this connection, the PL acts as a spin polarizer by transmitting or reflecting the incoming electron flow. The polarization remains during the tunneling

event (Fermi's golden rule), but when the electrons reach the FL, they interact with the magnetization of the FL. As a result, angular momentum from the polarized electron current is transferred to the FL magnetization, which is therefore oriented parallel to the magnetization of the PL.[19, 28]

One important property is that the transferred torque per unit area is proportional to the incoming spin-polarized current density and, as a result, with a decreasing device cross section due to downscaling, the required writing current decreases proportionally. The memory cell of STT-MRAM is simpler in construction than compared to MRAM, occupies a floor space of $20\,F^2$, stores data non-volatile, and requires 35 ns to perform write or read operations.[15, 19] Furthermore, Wang et al. revealed in [29] that STT-MRAM, which couples electron and spin transport, can be considered as a memristor – the 4th fundamental nonlinear passive circuit element.

2.4.4 Conclusion

All introduced upcoming technologies are already commercially available e.g. PCRAM in mobile phones [30] or FeRAM in memory smart cards and RFID [31]. The main advantage in comparison to baseline technologies is that information is stored non-volatile and fast data access is permitted by random access. The required time to read a data bit is in the range of tens of nanoseconds and surpasses NAND flash memory by far. Write and erase operation with exception of PCRAM (100 ns) are within the same order of magnitude. Retention times are stated with 10 years or more. More detailed information about characteristic parameters is listed in table 1. In case of PCRAM, no change in bias voltage polarity is necessary to perform read, write, and erase operations what is denoted as unipolar switching in contrast to bipolar switching of FeRAM, MRAM and STT-MRAM. FeRAM overcomes 10^{14} write cycles and has therefore a higher reliability compared to PCRAM (10^9) and STT-MRAM (10^{12}). PCRAM, MRAM and STT-MRAM store information by different means of resistance values. The memory cell with two contact electrodes is located at the intersections of the cross bar array and can be accessed by addressing the corresponding word and bit line. Nevertheless, selective elements such as access transistors or diodes are necessary in order to avoid current leak paths over adjacent memory cells. Consequently, the construction of the memory cell is more complicated and the minimum possible required cell area of $4\,F^2$ has only been realized in case of PCRAM so far.

2.5 Memristor

The memristor is a fundamental electrical component and was originally introduced as the fourth basic circuit element in 1971 by Leon Chua [6] who studied non-linear circuit theory. Until then, only three such fundamental components were known, namely the resistor, capacitor, and inductor which are characterized by the resistance R (Ω), capacity C (F), and inductivity L (H), respectively. The term memristor is a portmanteau word made up of *memory* & *resistor* and denotes a passive, two-terminal, and non-linear circuit element. Passive circuit elements do not introduce additional energy into the system. The designation two-terminal indicates that such components exhibit two contact electrodes. It is important to mention that RLC-circuits alone cannot imitate memristor like behavior.[6] An electric circuit is described by the four state variables: electric current I (A), charge Q (C), voltage U (V), and magnetic flux (Φ). In linear circuit theory, resistance, capacity and inductivity are treated as constant and are defined as follows by relationships of pairs of the four state variables:

$$\begin{aligned} &\text{resistance:} && R = U/I \\ &\text{capacity:} && C = Q/U \\ &\text{inductance:} && L = \Phi/I \end{aligned}$$

The four state variables are linked by Faraday's law of induction (Equation (1)) and the basic relationship between current I and charge Q (Equation (2)).

$$d\Phi = U dt \tag{1}$$

$$dQ = I dt \tag{2}$$

In non-linear circuit theory, the resistance, capacity, and inductivity are defined by the derivative of one state variable with respect to another one, which results in following relationship for

$$\begin{aligned} \text{resistance:}\ & R = dU/dI \\ \text{capacity:}\ & C = dQ/dU \\ \text{inductivity:}\ & L = d\Phi/dI \end{aligned}$$

These three relationships as well as equation (1) and (2) are illustrated in Figure 10, in which quadrant I-III represents the non-linear capacitor, resistor, and inductor. In quadrant IV appears a new relationship, which functionally links the electric charge with magnetic flux by defining a new physical quantity called memristance M with the unit Ohm (Ω).[7]

$$\text{memristance: } M = d\Phi/dQ \tag{3}$$

The term memristance is similar to memristor a portmanteau word made up of "memory" & "resistance".[6] A passive, two-terminal, and non-linear device capable of realizing this relationship is called memristor and is characterized by the memristance M (Ω).

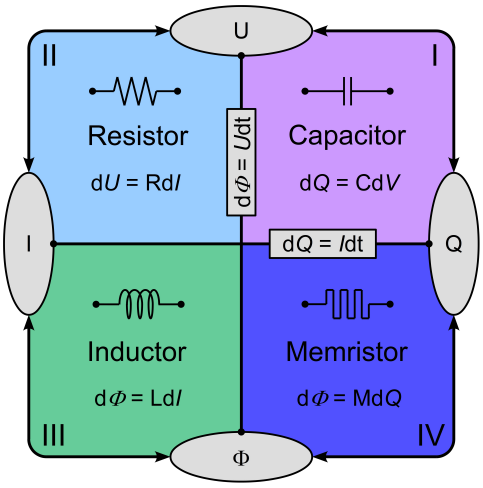


Figure 10: *Illustration of relationships between the state variables U, I, Q, and* Φ *which define the physical quantities of resistor, capacitor, inductor, and memristor. Taken and modified from [7].*

The mathematical discussion below, follows Leon Chua's argumentation in [32] in which the memristor is mathematically defining by a constitutive relation between the following two equations.

$$\varphi(t) \triangleq \int_{-\infty}^{t} u(\tau)d\tau \tag{4}$$

$$q(t) \triangleq \int_{-\infty}^{t} i(\tau)d\tau \tag{5}$$

Equation (4) and (5) can be associated with the integral version of equation (1) and (2), respectively. Therefore, $\varphi(t)$ and $q(t)$ can be considered as the magnetic flux and the electric charge. The time dependent variable $u(\tau)$ denotes the bias voltage applied at the memristor and $i(\tau)$ correspond to the current flow through it over time. If the constitutive relation between both equations can be expressed as

$$\varphi = \hat{\varphi}(q) \tag{6}$$

or

$$q = \hat{q}(\varphi) \tag{7}$$

, then the memristor is considered either as charge-controlled (Equation (6)) or flux-controlled (Equation (7)). Hence, the memristance in equation (3) is either a function of charge or magnetic flux. A differentiation with respect to the time t is derived as follows:

$$u = \frac{d\Phi}{dt} = \frac{d\hat{\varphi}(q)}{dq}\frac{dq}{dt} \tag{8}$$

$$i = \frac{dq}{dt} = \frac{d\hat{q}(\varphi)}{d\varphi}\frac{d\varphi}{dt} \tag{9}$$

With the definitions

$$R(q) \triangleq \frac{d\hat{\varphi}(q)}{dq} \tag{10}$$

$$G(\varphi) \triangleq \frac{d\hat{q}(\varphi)}{d\varphi} \tag{11}$$

, the memristance R(q) (Ω) and the memductance G(φ) (S) are obtained as a function of q and Φ, respectively. Inserting equation (1) and (2) results in:

$$u = R(q)i \tag{12}$$

$$i = G(\varphi)u \tag{13}$$

Equation (12) and (13) describe charge- and a flux controlled memristors, respectively. One can observe that the deduced memristor equations correspond to Ohm's law, but with the exception that the resistance R(q) depends on the entire past history of i(t). Similarly, the conductance G(φ) depends on the entire past history of v(t). R(q) is the memristance and G(φ) is the memductance of a memristive system. Memductance is similar to memristor a portmanteau word made up of *memory* & *conductance*.

Basically, the memristor obeys Ohm's law at any time like a resistor. However, a more comprehensible way of understanding such unique behavior is opened up by considering the variable resistance as a function of an internal state of the memristor device. The internal state can be described by a dynamical state variable x whose evolution in time is modeled by a differential equation called the state equation. Hence, a memristor can also be defined by a state dependent Ohm's law and a memristor state equation which is specified in case of a charge controlled memristor as follows:

$$\text{State dependent Ohm's law: } u = R(x)i \tag{14}$$

$$\text{Memristor state equation: } dx/dt = f(x, i) \tag{15}$$

In case of an ideal charge controlled memristor $f(x, i) = i$. Solving equation (15) by integrating with respect to time results in x being equal to q and, consequently, equation (14) corresponds with (15) to the equivalent of the state dependent Ohm's law of an ideal charge controlled memristor (Equation (12)). The overall amount of charge q that has been flown through the device determines the current state x as governed by equation (5). Generally, x can be a vector containing a number of internal state variables depending on the device material as well as underlying physical processes.[32]

A distinct fingerprint of a memristor is a pinched hysteresis loop. Pinched means that the device characteristic passes through the origin ($v = 0, i = 0$) of the I-V plane. Moreover, the device characteristic is confined to the first and third quadrant, due to the fact that the memristor is passive and therefore the memristance always greater than zero. A consequence of the passivity is that if one disconnect or short circuit the device, the current and voltage will become zero and the values for $q(t)$ and $\varphi(t)$ will not be changed anymore. Therefore, the memristor is non-volatile and can be considered as a continuously tunable resistor. In principal, a memristor can exhibit an enormous number of states similar to different states of multi-level flash cell. Two states are required in order to store one data bit. These states are denoted similar to PCRAM as off-state or

high resistive state (HRS) and on-state or low resistive state (LRS) and are indicated by a low (0-bit) and high device current (1-bit), respectively.[32]

Leon Chua proposed in [32] that all two terminal, passive, and non-volatile memory devices that bases on unipolar/bipolar resistance switching and exhibit a pinched hysteresis loop can be considered as memristors regardless of the switching mechanism and underlying physical processes. In order to model such behavior, the ideal memristor state equation is unfolded.

$$\frac{dx}{dt} = a_1 x + a_2 x^2 + \dots a_m x^m + b_1 i + b_2 i^2 + \dots b_n i^n + \sum_{j,k=1}^{p,r} c_{jk} x^j i^k$$

The experimental data can be fitted by choosing different values for the unfolding parameters a_j,b_k, and c_{jk} and the memristor model be adapted correspondingly.

Memristive behavior can also be observed from many unrelated phenomena such as discharge arcs, mercury lamps, synapsis and arises naturally due to nano structuring what can be observed in a number of solid state devices e.g. in oxide thin films or spin-transfer magnetic tunneling junctions.[7, 29, 32–34]

2.5.1 Inorganic Memristor

The first observation of a memristive system was announced by Hewlett-Packard researchers around Stan Williams in journal Nature [7] in 2008. The reported system was a nanostructured two-terminal devices which consisted of two platinum contact electrodes separated by a titanium oxide (TiO_2) thin film (see Figure 11). The TiO_2 is divided into two layers. One with pure insulating TiO_2 and another one that is conductive due to the presents of oxygen vacancies (TiO_{2-x}). The vacancies act as +2-charged dopants and can move in an electric field.[7] The overall device resistance is determined by the resistance of the doped TiO_{2-x} and undoped TiO_2 layer. The interface position of these two layers is indicated by the state variable w in Figure 12a. Applying an bias voltage results in an electric field in which the vacancies start to move and, as a result, the interface position is moved correspondingly. As a consequence, the TiO_{2-x} layer thickness increases while decreasing the TiO_2 layer thickness and vice versa. Simplified borderline cases are a totally doped or undoped regions, which extend over the whole device crossection like illustrated in Figure 12b. Resulting device resistances are denoted as R_{Off} and R_{On} and are associated with the HRS and LRS, respectively. The interface position w can vary in the range from 0 to the overall device thickness D, what corresponds to an equivalent variation of the device resistance in the range from R_{On} to R_{Off} (see Figure 12c).

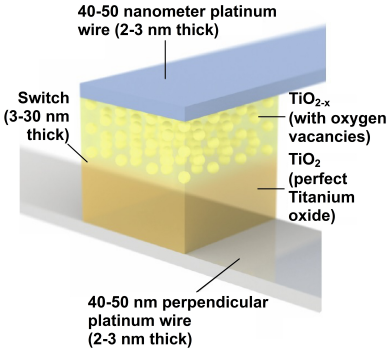
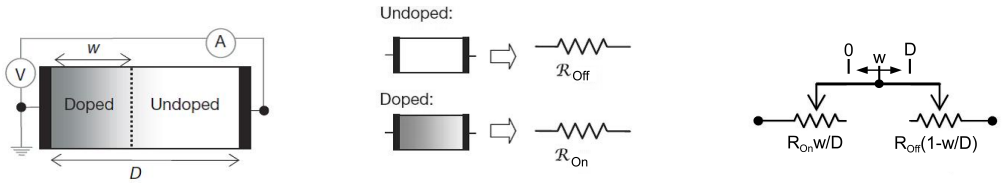


Figure 11: *Illustration of a memristor device located at the intersection of a crossbar array. Taken and modified from [7].*



(a) *Schematic crossection* ***(b)*** *On/off state* ***(c)*** *Equivalent circuit*

Figure 12: *Schematic cross section and equivalent circuit of a TiO_2 memristor. Taken and modified from [7].*

The total device resistance is obtained by adding the resistances of the doped and undoped layer.

$$R_{total} = \left(R_{On} \frac{w}{D} + R_{Off} \left(\frac{D-w}{D} \right) \right) \tag{16}$$

The memristor is defined as discussed before by a state dependent Ohm's law and a memristor state equation:

$$u(t) = R(w)i(t) \tag{17}$$

$$\frac{dw}{dt} = f(w,i) \tag{18}$$

The state dependent Ohm's law of the system is obtained by inserting equation (16) into equation (17).

$$u(t) = \left(R_{On} \frac{w}{D} + R_{Off} \left(1 - \frac{w}{D} \right) \right) i(t) \tag{19}$$

The required state variable is the interface position w. Its derivative with respect to time according to equation (19) is its moving speed which corresponds to the moving speed of the oxygen vacancies in electric field.

$$\frac{dw(t)}{dt} = \mu_V E \tag{20}$$

Variable μ_V denotes the oxygen vacancy mobility and E is the electric field strength. Assuming the simplest case of ohmic electronic conduction, then a uniform electric field and average mobility results in following relationship.[7]

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{On}}{D} i(t) \tag{21}$$

Integration with respect to time gives the interface position.

$$w(t) = \mu_V \frac{R_{On}}{D} q(t) \tag{22}$$

Inserting equation (22) under the assumption of $R_{On} \ll R_{Off}$ in equation (19) yields the memristance as a function of q.

$$M = \frac{u(t)}{i(t)} = R_{Off} \left(1 - \mu_V \frac{R_{On}}{D^2} q(t) \right) \tag{23}$$

Despite a number of simplifications, two important findings can be obtained. First, the

memristance depends on the overall amount of charge that has been flown through the devices and, therefore, the device is a charge controlled memristor. Second, the charge dependent term in equation (23) scales with one over devices thickness squared (D^{-2}) and, as a consequence, the memristance arise naturally due to nanostructuring of the device. It is important to stress that the memristance can only be varied in experiment in the range from R_{On} to R_{Off} what corresponds to the confinement of the interface position in the interval [0,D]. This limitation is initially respected in equation (16), but does not appears any longer in equation (23). A reported I/V characteristic is illustrated in Figure 13 below. The observed device characteristic is bipolar due to the fact that the diffusion direction of oxygen vacancies depends on the applied bias voltage polarity. Therefore, set and reset operations indicated by the red arrows requires different bias voltage polarities.

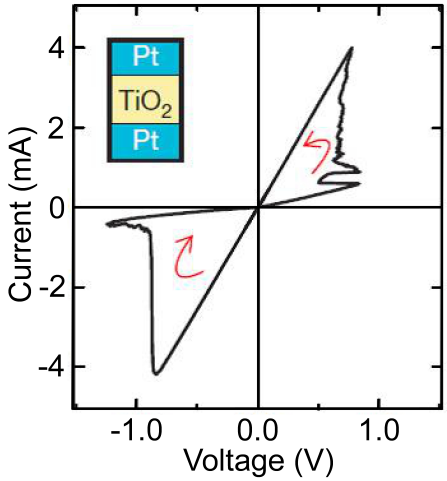


Figure 13: *Bipolar device characteristic of a $Pt/TiO_2/Pt$ memristor. Taken and modified from [7].*

The two straight curves that passes through the origin are associated with the HRS and LRS of the device and correspond accordingly to R_{Off} and R_{On}. Switching from HRS into LRS and vice versa occurs step like what can be explained by non-linear atomic drift.[7]

The memristor is concerning memory technology a resistive memory element that stores information by different resistance values of the memory cell comparable to PCRAM and STT-MRAM. However, due to its property of "remembering" previous stimulation, the memristor also behaves like a synapses what opens up the possibility to develop learning networks.

2.5.2 Organic Memristor

Electrochemical devices with a variable conductivity, which depends on the redox state of a polymer, can be considered as an organic memristor. The memristive device is comparable in construction to an electrochemical field effect transistor (FET), but has nothing in common with its working principle. A FET is a three-terminal device, what is actually inconsistent with the originally definition of a memristor in [6]. However, the definition was extended in such a way that if the current or voltage applied on a third terminal does not influences the internal state, then the three-terminal device can also be considered as a memristor.[32] The three contacts are denoted analogue to a FET as source (S), gate (G), and drain (D). A schematic device crossection is illustrated in Figure 14, in which a substrate with two contact electrodes denoted as S and D carries a thin film of a conductive polymer such as polyaniline (PANI). The memristive behavior resides in this film, due to the fact that its conductivity can be varied by redox processes. For this purpose, polyethylene oxide (PEO) doped with lithium chloride (LiCl) is applied on top of the PANI, whereby PEO acts as a solid electrolyte. In order to provide a reference potential for the redox reaction, the PEO is electrically contacted and grounded just as the source contact. The bias voltage applied on the drain contact controls the potential at the reaction zone close to the gate contact. Due to the fact that G and S are grounded, the device can basically be considered as a two-terminal component.[35]

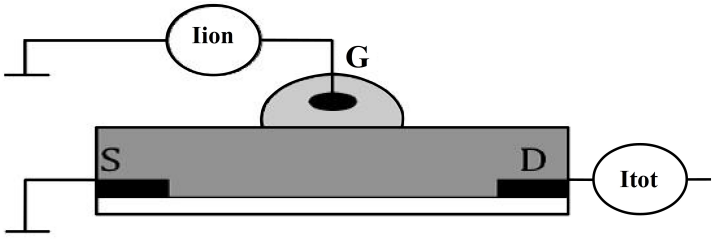
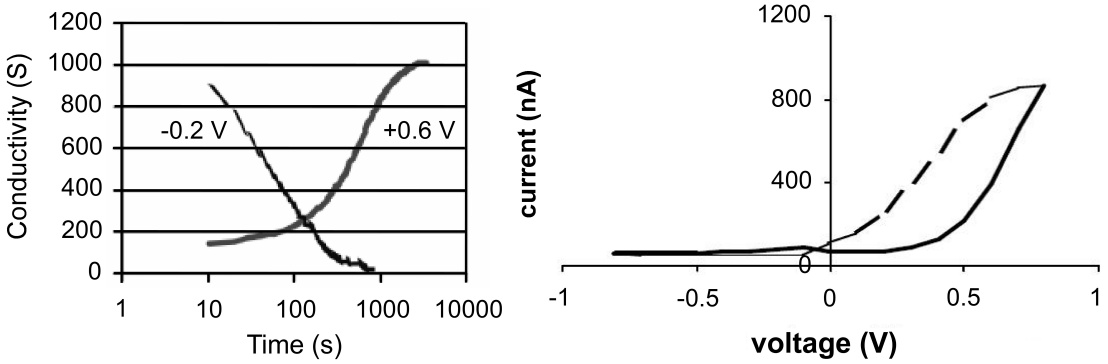


Figure 14: *Schematic cross section of an electrochemical FET. The solid electrolyte reservoir is contacted by gate contact on top of the conductive polymer. Taken and modified from [35].*

Oxidized PANI is positively charged and more conductive than in comparison to its reduced state. Figure 15a shows the change in conductivity of PANI layer over time due to oxidation and reduction processes. The corresponding redox reaction is described by the equation below, where the oxidized PANI state is on the left and the reduce one on the right.[35]

$$PANI^{+} : CL^{-} + Li^{+} + e^{-} \Leftrightarrow PANI + LiCl \tag{24}$$

As a consequence of the oxidation process, PANI requires a negatively charged ion, which is in this case a chloride ion (Cl^{-}) provided by the lithium salt. The resulting ionic current I_{Ion} is proportional to oxidation rate and sensed by the equivalent gate current. Therefore, the oxidation state, which varies the conductivity, is proportional to the amount of charge that has flown over the gate contact. In this connection, the device can be considered as a charge controlled memristor. The oxidation (reduction) process takes place above (below) a certain bias voltage, at which the necessary oxidation (reduction) potential is formed. During the reduction process, chloride and lithium ions are forming again LiCl and the positively charged PANI takes an electron from the channel. Therefore, it exhibit a neutral form and, as a consequence, the conductivity of the PANI layer decreases. During the reduction process the sign of the gate current changes with respect to the oxidation process. Figure 15b shows the differential current given by the difference between the total current through the device and I_{Ion}. The change in conductivity is reported with about two orders of magnitude (see Figure 15b).



(a) *PANI conductivity* ***(b)*** *Differential current*

Figure 15: *(a) Change in conductivity during oxidation and reduction processes. (b) Differential current illustrates different device states. Taken and modified from [35].*

Erokin et al. showed in [35] that the change in conductivity is correlated with the amount of transferred ionic charge. The change is gradual for oxidation and reduction processes as can be seen in Figure 15a. The organic memristor is non-volatile due to the fact that a redox potential is required for a state change. Therefore, this device can really be considered as a memristor. A possible application is modeling of neuromorphic circuits, which are able to learn by altering the conductivity of its signal pathways likewise synapses of a brain.

2.5.3 Conclusion

A memristor is similar to PCRAM and (STT-)MRAM a resistive memory element that stores information non-volatile by means of different resistance values. Moving ionic charge under an external bias voltage is responsible for variation in device resistance and, therefore, responsible fore the observed memristic behavior. In case of the introduced organic memristor, chloride ions are attached to a conductive polymer during a reversible oxidation process. The discussed inorganic TiO_2 memristor exhibit oxygen vacancies acting as +2-charged dopants, which move in electric field. The memristive behavior bases on an inherent property of these devices, namely, an internal state indicated by a state variable x. The state variable can generally be a vector $\vec{x}$ consisting out of a number of state variables $(x_1, x_2, \ldots, x_n)$ that depend on material properties as well as underlying physical processes, but they may not be influenced by any external variable e.g. magnetic field or charge or current applied to a third terminal of the considered device.[32] The internal state defines the resistance of the memristor. Hence, it is an state dependent resistor. Changes in x depends on charge flow (charge controlled) or magnetic flux (flux controlled) through the device. It is important to emphasize that the memristor obeys Ohm's law at any time. Its passivity is an important property that confines the I/V curve to the first and third quadrant of the I-V plane. Consequently, it passes through the origin. Furthermore, each state of the memristor is an equilibrium state that is maintained even without power supply and is therefore non-volatile.

Memory cells basing on memristors have the potential to meet all the requirements on an ideal memory element at once. Inorganic memristors with sub-nanosecond switching times [36], a minimum feature size of 30 nm, endurance of 10^{12} write cycles [37] and a minimum required floor space of $4\,\mathrm{F}^2$ [38] have been demonstrated. Due to the fact that the memristor is non-volatile unlike SRAM and DRAM, no rebooting of computer systems that bases on memristive memory devices will be necessary after losing power supply.

Because of its unique property compared to other two-terminal devices, namely "remembering" its history, the memristor can be considered as a hardware based emulation of synapses that form the interconnections of brain cells in living beings. This behavior allows to design neuromorphic networks that are capable of learning and memorizing due to changing the conductivity of their interconnections just as synapsis do due to repeated use – learning. Such networks can be used e.g. for intelligent sensors, information processing, decision making and for emulating functions of a human brain.[15, 35]

2.6 Characteristic Parameters

Device parameters for current baseline (SRAM, DRAM, flash) and prototypical memory technologies are listed in Table 1 below. The corresponding values are taken from [15]. In case of flash and DRAM parameters for stand alone applications are listed. Parameters for flash are referred to NAND flash memory.

Table 1: *Characteristic memory parameters*

Type	SRAM	DRAM	Flash	FeRAM	STT-MRAM	PCRAM
Non-volatile	No	No	Yes	Yes	Yes	Yes
Feature Size F (nm)	45	36	16	180	65	45
Cell Area [nm^2]	140 F^2	6 F^2	4 F^2	22 F^2	20 F^2	4 F^2
Read Time	0.2 ns	<10 ns	0.1 ms	40 ns	35 ns	12 ns
Write-/Erase-Time	0.2 ns	<10 ns	1/0.1 ms	65 ns	35 ns	100 ns
Retention Time	[A]	64 ms	10 y	10 y	>10 y	>10 y
Write Cycles	>1E16	>1E16	1E5	1E14	>1E12	1E9
Write voltage (V)	1	2.5	15-20	1.3-3.3	1.8	3
Read voltage (V)	1	1.8	4.5	1.3-3.3	1.8	1.2
Write Energy [J/bit]	5E-16	4E-15	4E-16	3E-14	2.5E-12	6E-12

[A] SRAM maintains information without refresh cycles as long as power supply is available.

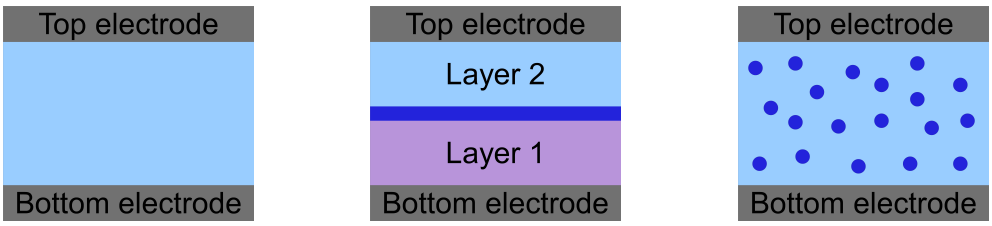
3 Organic Memory Elements

Organic technology can basically be used to fabricate organic counterparts of entrenched inorganic memory technologies which serve as templates for the technical implementation. Due to its diverse nature, however, organic technology also opens up more elegant possibilities for the realization of an organic memory element. Different mechanisms such as space charges and traps, filamentary conduction, mobile ions, donor-acceptor complexes in polymer or small molecule based bistable devices have been reported so far.[13, 39, 40] In this context, bistable means that the information is stored by at least two different resistance states of the memory cell. A major advantage of these systems is that the respective states of the memory device are non-volatile and reversible. As a result, no power supply is required in order to maintain the device state which can be changed repeatedly.

Although, the basic mechanisms of charge transport in organic semiconductors are well understood, the underlying physical mechanisms responsible for reversible resistance switching are for a majority of the reported polymer or small molecule based device structures still under debate. In order to adjust device properties and improve the performance, a complete understanding of memory device physics is necessary. The focus of this work is exclusively on memory elements which device structure corresponded to a plate capacitor (two-terminal device) and stored information reversibly by means of different resistance values of the bit call.

3.1 Device Structure

The sandwich device structure is favored in case of two-terminal memory elements due to the fact that a layer-by-layer fabrication process allows a straightforward realization of a large variety of different memory device types. The basic design correspond to a plate capacitor where the actual memory element is formed by the overlapping regions of the electrodes. Only two electrodes, which are denoted as top electrode (TE) and bottom electrode (BE), are required in order to control a single memory element completely.



(a) *Single layer* ***(b)*** *Hybride multilayer* ***(c)*** *Blend of nanoparticles*

Figure 16: *Schematic cross sections of different types of organic memory elements fabricated as sandwich structure. Dark grey regions indicate top and bottom electrodes, organic compounds are colored light blue and purple, respectively. Metallic interlayers and incorporated NPs are colored blue.*

The active material separates them and can basically consists of any organic compound. Additionally, hybrid organic/inorganic systems are investigated which exhibit metallic interlayers or incorporated nanoparticles (NPs). Cross sections of different memory element structures are illustrated in Figure 16.

Single layer devices correspond most closely to a plate capacitor. Here, two electrodes are separated by only one layer of polymers or small molecules. On the contrary, multilayer devices exhibit at least two layers of different polymers or small molecules, which form together the separating material. Furthermore, hybrid systems with metallic interlayers (Figure 16b) or metallic nanoparticles blended into the organic host (Figure 16c) are in focus of current research work and intensively discussed.[13, 39–43] The metallic interlayer in Figure 16b can consists of a continuous or percolating film or separated islands (nanoparticles) and is discussed in detail in Chapter 3.4.1.

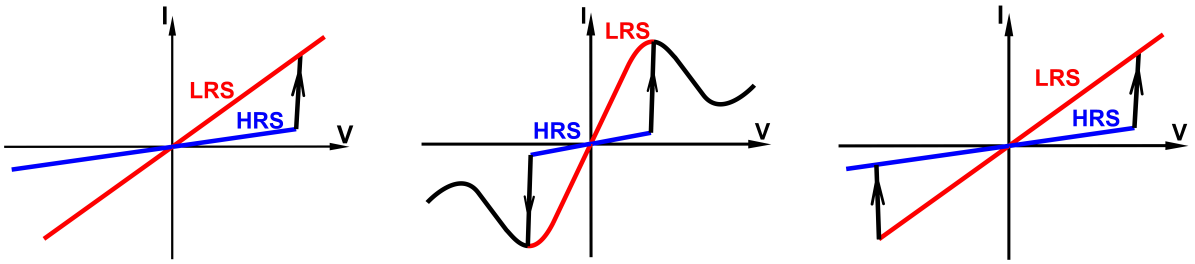
Layer thicknesses are usually in the nanometer regime. However, the horizontal dimensions can be much larger e.g. in the millimeter range. As a result, the occupied memory area can correspond to several mm^2. Due to the fact that the observed switching ability is an inherent nature of the memory element and belongs therefore on the interplay of the electrodes and the active material, the highest possible integration density of $4\,\mathrm{F}^2$ can be achieved for single memory elements.

3.2 Device Characteristic

Organic bistable memory devices store information by means of two different resistance states of the memory cell which are denoted as high resistance state (HRS) and low resistance state (LRS). Switching between these two states as well as the state determination is performed electrically by current/voltage (I/V) measurements. The determination of

the device state is also referred to as reading operation and is performed at a certain read voltage. High and low device resistances cause according to Ohm's law low and high currents which are associated with the 0-bit and 1-bit, respectively. The at least two stable resistance states of the memory device are indicated by a bistable region of the I/V characteristic, in which two different current values are related to one certain bias voltage. The observation of a bistable region is a necessary condition for a given device structure to be considered as a resistive memory element. The switching process changes the resistance of the device and is controlled by applying a bias voltage with appropriate amplitude and polarity. If a certain critical bias voltage is exceeded, then an abrupt or continuous state transition can be observed. In case of an abrupt state transition, the corresponding bias voltage is denoted as threshold voltage V_T. The device can generally be set into a specific state by performing a program operation. In particular, the state transition from HRS into LRS and from LRS into HRS is also referred to as a writing and erasing operation, respectively.

According to literature [39], typical I/V characteristics of resistive switching and nonvolatile organic memory devices can be classified as: Write once and read many (WORM), unipolar and bipolar switching behavior.



(a) *WORM* ***(b)*** *Unipolar* ***(c)*** *Bipolar*

Figure 17: *Typical I/V characteristics of organic bistable memory devices. HRSs and LRSs are colored blue and red, respectively. Black arrows indicate state transitions form HRS into LRS and vice versa.*

WROM devices exhibit initially a HRS and can be switched into LRS only once (Figure 17a). Hence, the state transition is irreversible. On the contrary, switching from HRS into LRS is reversible in case of unipolar and bipolar memory elements. Their corresponding device characteristics are illustrated schematically in Figure 17b & 17c and are explained in the following Chapters.

3.2.1 Unipolar Device Characteristic

In case of a unipolar device characteristic, the electrical resistance of the memory element is controlled by the amplitude of the external applied bias voltage and is generally independent of its polarity. Unipolar device characteristics are symmetric to the origin of the I/V plane and exhibit at low bias voltages around the origin the so called bistable region, in which two I/V curves appear. These two curves correspond to the HRS and LRS state of a bistable device. A characteristic feature of a unipolar device characteristic is a negative differential resistance (NDR) range. It appears between the local maximum at V_{max} and the local minimum at V_{min} of the corresponding bias voltage range. Within the NDR, the measured device current decreases with increasing bias voltage amplitude and vice versa. A state transition from HRS into LRS occurs abruptly at the threshold voltage V_T. Now the question arises how can a complete I/V characteristic of a unipolar and bistable organic memory element be obtained?

1. Suppose that the device is initially in the HRS state (blue curve). Then, the bias voltage is swept up steadily starting at 0 V. The current stays low and the HRS can be observed in the positive bias voltage range until the threshold voltage V_T is reached at which the current increases significantly. Therefore, the device performs a state transition from HRS into a more conductive state. This switching process is finished after the local maximum of the device characteristic at V_{max} is reached. Now the device is set into the LRS.

2. With a further increase of the bias voltage, the device current decreases until the local minimum at V_{min} is reached. Hence, the NDR range of the memory element is observed.

3. After V_{min} is exceeded, the device current increases again with increasing bias voltage until the voltage sweep is stopped and the applied bias voltage turned instantaneously to 0 V. Repeating the whole bias voltage sweep will reveal the same device characteristic (blue & black curve in Figure 19b). Hence, high bias voltages beyond V_{min} set the device into a HRS.

4. A further bias voltage sweep is performed now. However, it is stopped at V_{max} and the bias voltage is turned instantaneously back to 0 V. Subsequently, another sweep is performed during which the measured current is significantly increased and LRS is revealed (see red curve in Figure 19b). The corresponding I/V curve

hits the initial curve (black curve) at V_{max} and is identical with it at bias voltages higher than V_{max}.

5. The voltage sweep is stopped at $V > V_{min}$ and, as a result, the device is set into the HRS again.

6. Due to the fact that unipolar switching behavior is independent of the bias voltage polarity, the identical operations (point 1 to 5) can be performed likewise in the negative bias voltage range by inverting the applied bias voltage polarity.

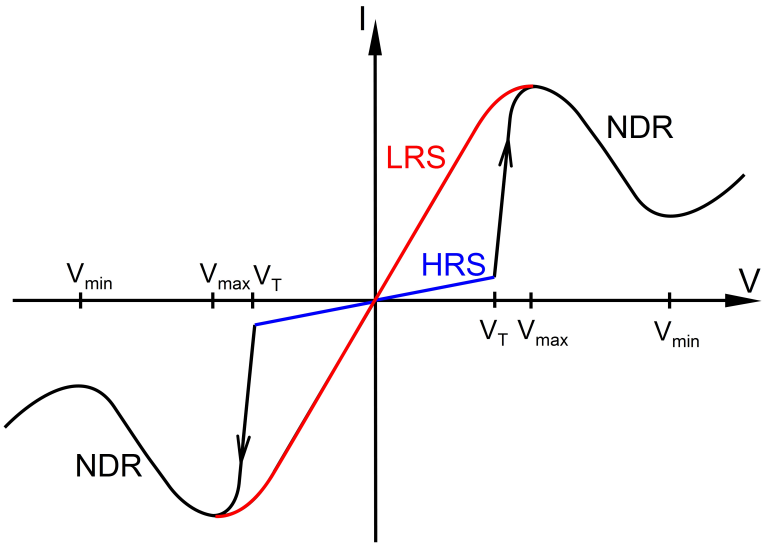
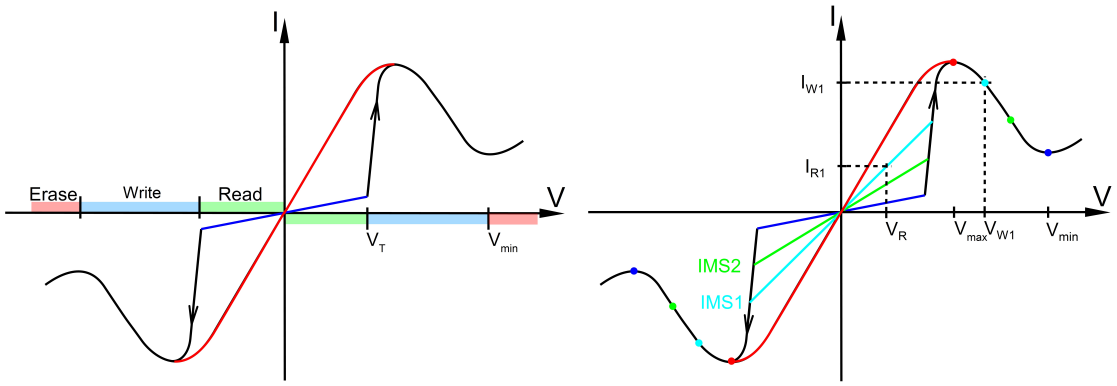


Figure 18: *Unipolar device characteristics are generally symmetric to the origin of the I/V plane. The bistable region appears at low bias voltage amplitudes around the origin. HRS and LRS are colored blue and red, respectively. Directly adjacent to the bistable regions are the NDR ranges which extends from V_{max} to V_{min} in the corresponding bias voltage range.*

It is important to stress that, the current device state only depends on the amplitude of the right before applied bias voltage that corresponds to program region (write + erase region) of the device (see Figure 19a). As a consequence, reading, writing and erasing operations can also be performed independently of the current device state by applying a bias voltage pulse which amplitude corresponds to the read, write, or respectively erase region of a unipolar device characteristic (see Figure 19a).

The term bistable is misleading due to the fact that it only refers to the HRS and LRS which are actually boundary cases of a continuously range of possible device states. Device states which appear between HRS and LRS in the I/V plane are denoted as

intermediate states (IMS). They can be addressed by applying a corresponding write voltage within the NDR range (see Figure 19b).



(a) *Basic operations* ***(b)*** *Multistable device*

Figure 19: *(a) Read, write, and erase regions of a unipolar device characteristic. (b) IMSs are programmed by applying bias voltages which amplitude correspond to the NDR range.*

During the programming operation, the device is set into a specific state which remains after the bias voltage is returned to 0 V. Afterwards, a bias voltage sweep is performed within the read region in order to determine the programmed device state. Therefore, two different currents can be associated with one specific device state, namely, the write current I_W at V_W and the read current I_R at V_R with $0 < V_R < V_T$.

Reading, writing and erasing operations can be performed independently of the applied bias voltage polarity. Furthermore, programmed device stats are also symmetric to the origin of the I/V plane as long as the applied bias voltage correspond to the read region. Unipolar device characteristics are reported from polymer and small-molecule based MIM structures. Filament formation [44] and charging of incorporated nanoparticles are suggested as mechanisms responsible for unipolar and reversible resistance switching.[13]

3.2.2 Bipolar Device Characteristic

Resistance switching of bipolar memory devices depends, in contrast to unipolar resistance switching, on the bias voltage amplitude and the polarity of the applied bias voltage. State transitions occur similar to unipolar devices abruptly at a certain threshold voltages which are denoted as V_{T1} and V_{T2} in Figure 20. Applying higher bias voltage amplitudes than compared to the threshold voltage in the corresponding bias

voltage range, then resistance switching also takes place. A bipolar device characteristic is obtained in the following manner:

1. Suppose that the device is initially in the HRS state (blue curve in Figure 20) and the bias voltage is ramped up starting at 0 V. The device remains in the HRS until the threshold voltage V_{T1} is reached at which a sharp increase of the current indicates the transition from the low conductive HRS into the high conductive LRS (red curve). A further increase of the bias voltage has generally no influence on the device state.

2. Then the bias voltage is decreased until the threshold voltage V_{T2} is reached in the opposite bias voltage range at which a steplike decline of the current indicates the transition from LRS into HRS. The region of bistability is revealed in the bias voltage range from V_{T1} to V_{T2}. A further decrease of bias voltage has generally no influence on the device state.

3. Finally, the bias voltage is swept up to 0 V and the complete bipolar device characteristic is revealed.

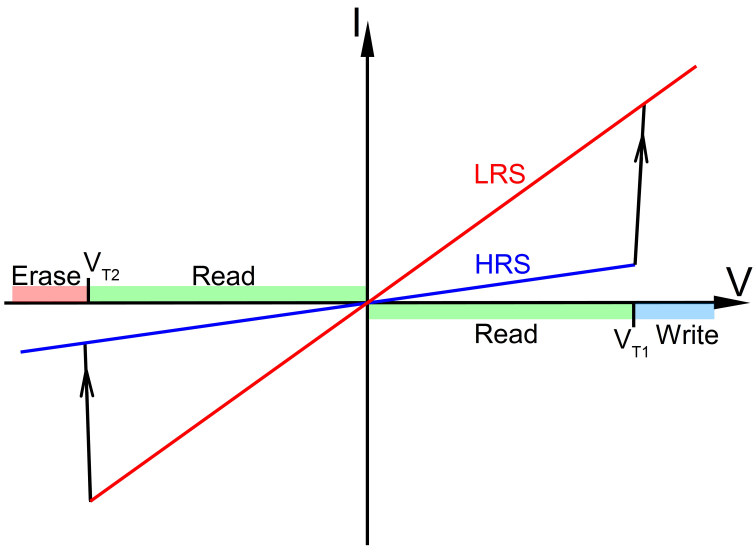


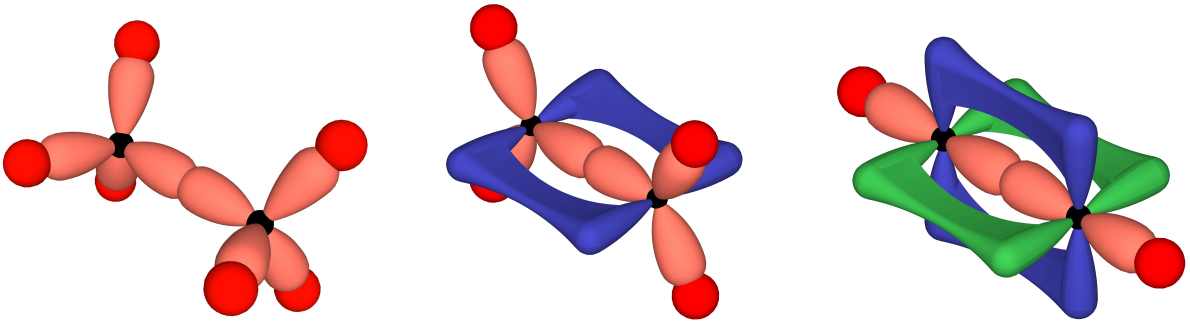
Figure 20: *Scheme of a bipolar device characteristic. HRS and LRS are colored blue and red, respectively. State transitions occur at the threshold voltages V_{T1} and V_{T2} and are indicated by black arrows. Read operations are performed within the bistable region between the threshold voltages.*

The device characteristic can again be divided into the read, write, and erase region. Bipolar device characteristics are reported for inorganic memristive systems and organic counterparts based on electrochemical processes.[7, 35]

3.2.3 Organic Semiconductors

Carbon is the key building block of organic compounds and makes a substantial contribution to their versatile nature well known from various products such as polyvinyl chloride (PVC) bottles, Teflon, composite material such as fiber-reinforced polymers or innovative high-end OLED displays. As a member of group 14 on the periodic table, the carbon family, carbon exhibit a $1s^2 2s^2 2p^2$ electron configuration. Due to its relatively small size and medium electronegativity [45], it can form chemical compounds with virtually any other chemical element such as hydrogen, oxygen, nitrogen, flour, sulfur etc. A great variety of organometallic compounds are also known e.g. Alq3. Here, organic compounds (ligands) are bonded to a metallic centering atom and form a metal complex.

The relatively small energy gap between the 2s- and 2p-orbitals is of significant importance for its versatility. It allows a promotion of one 2s-electron and, as a result, one carbon atom can form covalent bonds with up to four other atoms. During this process, a so called hybridization takes place which leads to a formation of sp^1-, sp^2- or sp^3-hybrid orbitals, respectively. The type of the bonding influences the steric configuration of the corresponding molecule as well as its electrical and optical properties. Prime examples for such bonds are ethane (C_2H_6), ethane (C_2H_4), and ethyne (C_2H_2) which exhibit two carbon atoms bonded by a single, double or triple covalent bond, respectively (see Figure 21).[45]

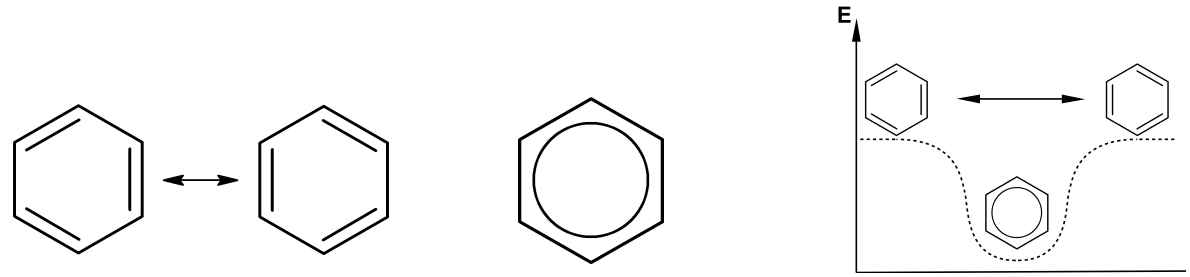


(a) *Ethane* ***(b)*** *Ethene* ***(c)*** *Ethyne*

Figure 21: *Schematic illustration of bonding MO of ethane, ethene and ethyne. The position of the carbon atoms are indicated by black spheres. Orbitals involved in a sigma bonding are colored red. π-bonds are colored blue and green.*

Two different types of covalent bonds appear in Figure 21 above: The σ-bond is formed by head-on overlap of involved orbitals and is symmetrical with respect to rotation about the bond axis. π-bonds are formed between two p-orbitals of adjacent atoms. Here, both lobs of one involved p-orbital overlap with both lobs of another one. The formed π-bond does not exhibit a rotational symmetry and, as a result, the ability for twisting is disabled in contrast to the σ-bonds. Furthermore, π-bonds are weaker in comparison to sigma bonds due to a reduced overlap of the involved orbitals.

Molecule orbital (MO) theory assumes that each molecule exhibit a uniform electron system [45] which is delocalized and can extend over the whole molecule skeleton. This effect is in case of chains of carbon atoms with a sequence of single and double bonds of significant importance (conjugated polymer), especially considering organic semiconductors. The double bonds consist, according to Figure 21b, of a sigma- and a π-bond (sp^2-hybridization). A prime example is benzene (C_6H_6). Its six carbon atoms are arranged to a ring and the bonding between them consists of three single and three double bonds. Therefore, two so called contribution structures of benzene are thinkable as shown in Figure 22a. However, they are boundary cases of a resonance structure in which all bond lengths are in fact equal. This phenomenon is denoted as mesomerism and is a consequence of the delocalization of the π-electron system which extends over the whole molecule as schematically indicated by the circle in Figure 22b. The driving force for this process is an energy reduction of the entire system (see Figure 22c).

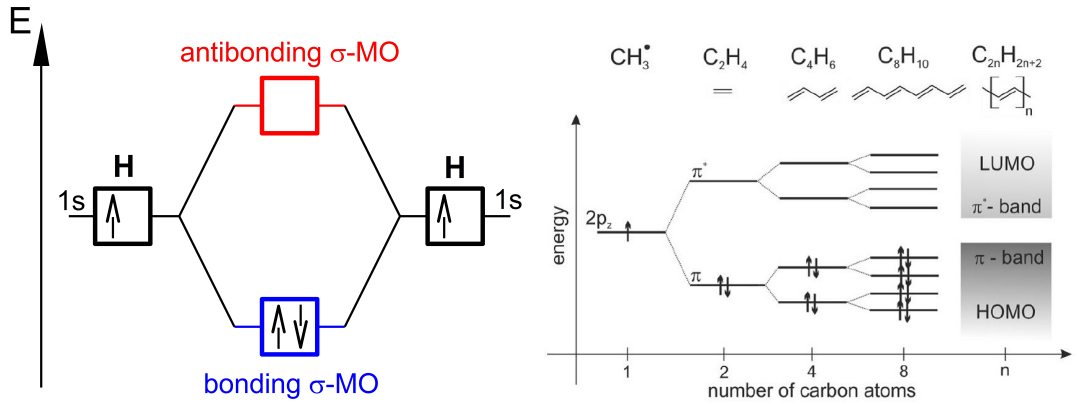


(a) *Contribution structures* ***(b)*** *Resonance structure* ***(c)*** *System energy*

Figure 22: *Contribution and resonance structures of benzene as well as a schematically comparison of the resulting system energy.*

According to linear combination of atomic orbitals (LCAO) theory, a MO can be approximated by a linear combination of the involved atomic orbitals.[45] In this process, always the same number of bonding and antibonding MOs are formed. Bonding MOs exhibit a lower energy and are therefore occupied first. A simple example is the H_2 molecule (see Figure 23a). Here, two 1s-atomic orbitals form a bonding and an anti-

bonding sigma MO, whereas the bonding MO is occupied by both electrons and the antibonding MO remains unoccupied. The energy gap between the bonding and antibonding MO is essential for the electrical properties. If only σ-bonds are involved, then the organic compound is an insulator because the band gap between the bonding and antibonding MO is too large. However, a delocalized π-electron in unsaturated hydrocarbons systems (sp^2 hybridization) exhibit a lower band gap and is therefore essential for organic semiconductors based on polymers or small molecules.



(a) *H_2* ***(b)*** *Alkenes*

Figure 23: *Schematic illustration of MO energy levels. (a) Bonding and antibonding H_2 sigma MO formed by two involved 1s hydrogen orbitals. (b) Energy levels of the delocalized π-electron system of alkenes (conjugated polymers) with increasing number of carbon atoms. Taken from [46].*

Another important aspect is the number of carbon atoms involved in a delocalized π-electron system. The energy gap between the bonding π-orbitals and the antibonding π^*-orbitals is reduced with increasing number of involved p-orbitals (see Figure 23b). Moreover, the number of π- and π^*-states increases proportionally. As a consequence, the energy levels of the π- and π^*-MOs become closer spaced what leads finally to a continuous π- and π^*-energy band.

The highest occupied molecule orbital (HOMO) and the lowest unoccupied molecule orbital (LUMO) are in this context of significant importance due to the fact that they determine physical properties of the corresponding organic compound. Furthermore, they influence the charge carrier transport in multilayer devices based on polymers or small molecules.

Alq3

Alq3 is the abbreviation for Tris(8-hydroxyquinolinato)aluminum. This chemical compound with the empirical formula $C_{27}H_{18}AlN_3O_3$ (Hill Notation) is a coordination complex wherein three conjugated 8-hydroxyquinoline ligands (C_9H_6NO) are bonded to a centering aluminum atom (see Figure 24). It is used as electron transport and hole blocking material in OLEDs and exhibit an HOMO and LUMO of 5.8 eV and 3.1 eV, respectively.[47]

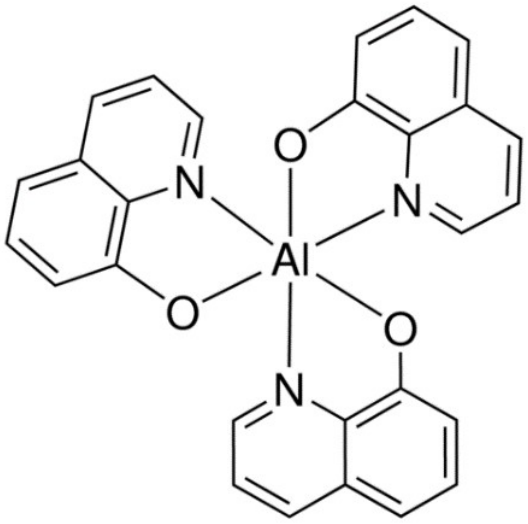


Figure 24: *Chemical structure of Alq3. Taken from [47].*

3.3 Charge Carrier Transport in Organic Semiconductors

Organic memory elements must obey the fundamental charge carrier transport mechanisms in systems based on organic technology which differs from band transport in single crystals. This is due to the fact that the overlap of delocalized π-electron systems with adjacent molecules is reduced by defects in the chemical structure as well as impurities and local disorder.[48, 49] As a consequence, organic semiconductor films exhibit localized states in contrast to a valence and conduction bands of single crystal systems. The charge carrier transport occurs via thermally assisted hopping processes between these localized states. Therefore, the charge carrier mobility increases with increasing temperature. On the contrary, the probability of phonon scattering is also increased with increasing temperature. Furthermore, interface effects play an important role for the

conduction process in organic semiconductors. The main conduction mechanism are Direct Tunneling, Fowler-Nordheim Tunneling, Thermionic Emission, Schottky Emission, Pool-Frenkel Emission, and Variable-Range Hopping.[17]

Direct Tunneling is a quantum mechanical effect during which electrons tunnel through a potential barrier such as an insulating layer between two metal electrodes. It is also used in the grain boundary model which describes the temperature independent charge carrier mobility at low temperatures. In this case, the organic semiconductor layer exhibit a granular structure with a trap free crystal grain and a grain boundary with a high trap density. As a consequence, the charge carrier mobility is relatively low at the grain boundary in comparison to the trap free crystal grain. The charge transport through the grain boundary is described by tunneling process at low temperatures which explains the temperature independence of the mobility, whereby a thermally activated tunneling process takes place at intermediate temperatures. The charge transport process changes to thermionic emission at high temperatures at the grain boundaries.[17, 46, 50]

Fowler-Nordheim tunneling is similar to direct tunneling. In this process, a large applied bias voltages leads to a bend bending and, as a consequence, the potential barrier is deformed and can be assumed to be triangular. Hence, the potential barrier thickness is reduced what results in an increase of the tunneling current.[17]

Thermionic emission describes the excitation of electrons to higher energies by phonons what allows them to overcome a potential barrier in contrast to tunneling mechanisms. Schottky emission is similar to thermionic emission. Here, enhanced band bending at the metal-organic interface region due to a combination of applied high bias voltages and electrostatic forces (mirror images) results in a reduction of the potential barrier height. As a consequence, even electrons at lower energies than compared to the Fermi energy can overcome the potential barrier.[17]

Poole-Frenkel conduction relies similar to thermionic and Schottky emission on thermally excitation of electrons. In this case, charge carriers are excited from traps or donor states in the in the conduction band of the organic semiconductor and contribute correspondingly to the conduction process.[17]

Variable-Range Hopping describes the charge carrier transport in organic semiconductors between localized states. This process can take place either by a thermally activated hopping process from one site to another due to phonon absorption or by quantum mechanical tunneling between states of equal energy. These two processes contribute with each other what is taken into account by maximizing the resulting conductivity in the corresponding model.[17] Different models are used in order to describe the distribution

of states e.g. the model developed by Bässler et al. [51] which is based on a Gaussian state distribution.

Different charge transport mechanisms occur in organic semiconductors. In summary, Direct tunneling, Fowler-Nordheim tunneling rely on quantum mechanical tunneling processes, whereby the latter case assumes a triangular potential barrier due to high applied bias voltages. Moreover, tunneling processes are also taken into account by variable range hopping. These processes are conduction limited in contrast to thermionic emission, Schottky emission and Pool-Frenkel emission processes which are injection limited. Thermally activation plays a significant role which leads to an increase of the conductivity with increasing temperature. However, the probability for phonon scattering also increases. Furthermore, the local electric field plays an important role, due to the fact that band bending occurs which reduces the potential barrier width.

3.4 Resistive Switching Mechanism

Resistive switching mechanisms responsible for reversible and unipolar resistance switching of hybrid organic memory devices are still under debate. They can generally be divided into highly localized processes or effects that extended over the entire device area. The former case is denoted as filamentary conduction, high-mobility pathways or conducting micro channels.[13, 39, 52] In the latter case, extended phenomenon such as redox reactions [13, 53] or space-charge fields due to charges trapped on NPs [42, 54] are under discussion. In the following, favored hypothesis are described and summarized.

3.4.1 Switching Based on Charge Trapping

Charge trapping on NPs is proposed as one possible mechanism for reversible and unipolar resistance switching. For this purpose, NP are embedded into an organic host material during device fabrication. This can be done with the help of ionized cluster beams, thermal co-evaporation or by an organic blend of NPs.[13] Moreover, NPs in form of disconnected islands of a granular film can be introduced by adding a thin metallic internal layer.[43] Using aluminum as interlayer material allows to cover the formed NPs (islands) easily with an oxide shell by oxidization due to the oxygen affinity of aluminum. Such oxide shell opens up the possibility to store electric charge reversibly and enduring at proper electric fields on the NPs. Moreover, introducing NPs by means of an inter-

mediate metal layer allows to control their position between the contact electrodes as well as their size which depends on the evaporation process.

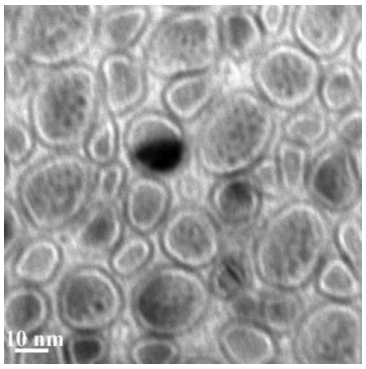


Figure 25: *Aluminum NP with oxide shell embedded into AlQ3. Taken from [54].*

The switching process based on charging of NPs was described by Simmons and Verderber [55] in 1967. They claimed that trapped charge carriers inhibit the charge carrier injection by building up a space charge field. Here, introduced NPs are considered as charge traps, which could be charged and discharged electrically what enables and disables the space charge field, respectively. Observed unipolar device characteristics can be explained in the following way:

Assuming that the device is in the LRS, then, the aluminum core shell NPs are uncharged and the device current is determined by the charge transport abilities of the organic bulk. However, electric charge can be stored on the NPs by a tunneling process at bias voltages that correspond to the NDR region of the I/V characteristic and, consequently, the space charge field is formed. It opposes the applied electric field and leads to a reduction of the charge carrier injection rate at the metal-organic interface. As a result, the device is switched into the HRS. The charge is trapped nonvolatile on the NP and will remain there as long as the applied bias voltage amplitude does not succeed the threshold voltage of the corresponding bias voltage range. The memory device can be switched back into the LRS by applying the threshold voltage which results in an abrupt discharge of the NPs what disables the space charge field.

Introduced nanoparticles can also facilitate filament formation, what is also a possible and heavily discussed explanation of unipolar as well as bipolar resistive switching in hybrid organic memory elements.

3.4.2 Filamentary Conduction

Switching mechanisms based on filamentary conduction are localized phenomena [56] which affects a relatively small regions of the device area. Besides the description of unipolar and reversible resistance switching, it is also capable to explain memory device initialization and influences on the device characteristics of repeated resistance switching as discussed in Chapter 5.

Filamentary conduction can be imagined by a metallic bridge between the two electrodes which is embedded into the organic host and can be ruptured and reformed repeatedly. According to Nau et al. [44], the conductivity of the memory device states is generally independent of the device capacity. Therefore, the organic host and the filament can be modeled as a parallel connection of resistors. The resulting overall device resistance is given by Equation 25.

$$R_{overall} = \frac{R_{fil} \cdot R_{bulk}}{R_{fil} + R_{bulk}} \tag{25}$$

A possible mechanism for the filament formation was described by You et al. [52] in 2012, who suggested that the migration of polarized metal atoms towards regions of higher electric field strength within an inhomogeneous electric field is responsible for filament formation. The driving force for such a migration process is a reduction of the potential energy W of a dipole $\overrightarrow{P}$ (polarized atom) in an inhomogeneous electric field $\overrightarrow{E}$.

$$W = -\overrightarrow{P} \cdot \overrightarrow{E} \tag{26}$$

Therefore, nanoscale tips are required for the filament formation process which can be formed e.g. during the deposition process due to rough surface morphology of the organic film or film defects. Also the formation as a result of the application of high bias voltages is thinkable. This process is also called burn-in.[57] When a bias voltage is applied, the electric field strength at the tip apex is higher than compared to flat interface regions [58] what leads to a non-uniform electric field. As a consequence, polarized metal atoms start to migrate toward the tip apex in order to reduce their potential energy within the electric field.

Suppose, the device is in the HRS and exhibit therefore a ruptured filament. Then the current will be carried mainly by the high resistive organic host and low bias voltages will have generally no influence on the condition of the filament. However, after succeeding a critical threshold voltage, the tip starts to grow abruptly and forms a filament [52] what results in a state transition from HRS into LRS of the memory element. The overall

device resistance can be approximated in this case by the filament resistance under the assumption of a relatively large on/off ratio. Corresponding device currents are given by Ohm's law and are therefore invers proportional to the device resistance.

The application of an erase voltages ruptures the filament by Joule heating and sets the memory device into the HRS. Program bias voltages, which correspond to the NDR range, ruptures the filament partially and set the device into an IMS.[59]

4 Experimental Methodology

In the following sections, the fabrication of organic memory devices is explained in detail. Additionally, performed measurement routines, which were used for dive characterization, and preconditioning are explained. Fabrication and characterization were carried out in an argon atmosphere glove box cluster by using state of the art laboratory equipment.

4.1 Device Fabrication

All organic memory elements fabricated during this work exhibited a sandwich like structure corresponding to a plate capacitor. Square glass plates with an edge length of 1 inch and a thickness of 1 mm were used as substrates. Each substrate carried eight memory elements, which were arranged in a (4x2)-memory array (see Figure 26) and shared one common bottom electrode (BE). The BE always corresponded to the first layer on the glass substrate. All other device layers were applied layer by layer on top of the BE. The fabrication process was finalized after the deposition of the top electrode (TE). The actual memory element was formed by the overlapping region of the TE and BE.

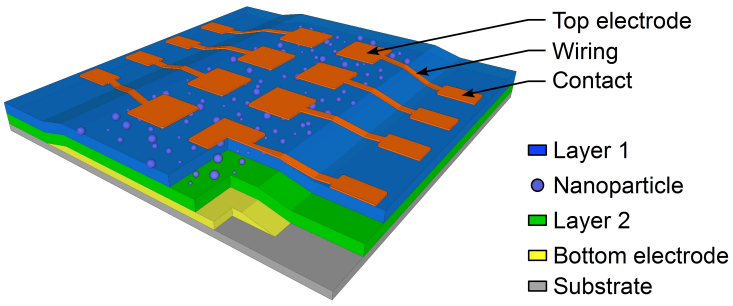


Figure 26: *Illustration of a substrate carrying eight hybrid organic/inorganic multilayer memory elements. TE and BE are separated by two different layers. Additionally, nanoparticles are incorporated into the interface region between layer 1 and layer 2.*

4.1.1 Substrate Preparation

Indium tin oxide (ITO) covered glass plates were used as substrates if not stated otherwise. In order to act as BE, the ITO layer had to be structured by a wet-chemical etching process. Therefore, the shape of the BE was masked off with a tape on the ITO surface. The exposed ITO was completely covered with process zinc powder (Sigma-Aldrich), which acted as a catalyst for the etching process. The etching was conducted in hydrochloride acid (HCl; 37%) and took approximately 25 s. As a result, the exposed ITO was taken off completely and the glass substrate was uncovered. Rinsing the etched substrate with deionized water removed the remaining acid and stopped the etching process completely. After peeling away the tape, the substrate was cleaned mechanically with acetone (aprotic and polar solvent) in order to remove remaining mask components. Edges of the ITO BE were smoothed by a second etching process in HCl. Here, the cleaned substrate was etched without mask and catalyst for approximately 3 s. After rinsing the substrate again with deionized water, the structuring process of the ITO BE was finished.

Each substrate had to be cleaned thoroughly just before the device assembly was started. For this purpose, a multi-step cleaning process was performed with polar and nonpolar solvents in order to remove dust particles and other kinds of impurities from the surface. First, the substrate was cleaned with acetone by wiping it with a lint-free cloth. This step was repeated afterwards with the nonpolar solvent isopropanol. The cleaning process was then finalized by cleaning the substrate in an ultrasonic isopropanol bath for 15 min. After each cleaning step, the substrate was dried by compressed air.

4.1.2 Device Assembly

Organic memory elements fabricated during this work exhibited a sandwich like structure. Depending on the layer material, either a physical evaporation or a spin-coating process was used for layer-by-layer device assembling. Organic layers based on small molecules, metallic intermediate layers (IMS) and metal top electrodes were applied by using a state of the art vapor deposition unit (VDU). The deposition process was conducted under vacuum conditions and was started after a pressure value $p \approx 10^{-6}$ mbar was reached. The layer growth as well as the evaporation rate were monitored by an oscillating quartz crystal and adjusted automatically to the programmed desired value.

The organic semiconductor Alq3 was mainly used as separating material. The corresponding evaporation process was performed with an evaporation rate of 1 Å/s until the

required layer thickness was reached. A metallic intermediate layer (IML) was applied in order to incorporate metallic nanoparticles (NPs) into the interface region of the two separating layers as shown in Figure 26. For this purpose, the layer thickness and the evaporation rate were set to 15 nm and 0.2 Å/s, respectively (for more details see Chapter 5.2). In order to cover the aluminum NPs with an oxide shell, the vacuum chamber was ventilated for 45 min after the deposition of the aluminum layer was finished. The remaining oxygen in the argon atmosphere oxidized the bare surface of the aluminum nanoparticles and formed a continuous oxide surface. Silver was used as raw material for the TE. It was deposited with an evaporation rate of 10 Å/s until a layer thickness of 100 nm was reached if not stated otherwise.

Polymer films were applied by spin-coating which is a solution based process. Dissolved polymers were quickly and evenly applied with a micro-pipette on the entire substrate. Then, the substrate was rotated at constant speed for a specific period. Appearing centrifugal forces catapulted most of the solution away and the remaining material formed a thin and continuous film. Its layer thickness was in the nanometer regime. The rotation speed and the duration of the coating process influenced the layer thickness. In case of water based solutions such as PEDOT:PSS, the wettability of the substrate surface could be improved by activation due to an O_2 plasma treatment. In this context, "activation" means that OH groups were added to the surface and improved its wettability (more hydrophilic). Plasma treatment was performed under vacuum conditions at 0.8 mbar and lasted about 10 min. The spin-coating was conducted with a rotation speed of 2500 rpm under ambient conditions for 40 s. As a result, the applied PEDOT:PSS formed a continuous and about 60 nm thick film. The remaining water in the PEDOT:PSS layer was removed by heating the substrate under ambient conditions at 200 °C for 5 min.

4.1.3 Preconditioning

A preconditioning procedure was performed for certain devices. In this process, the device was temperature treated in a heating chamber under vacuum conditions right after the fabrication. The adjusted temperature and period is specified in corresponding chapters. The pressure in the heating chamber was below 10^{-2} mbar. In order to perform a preconditioning, the finished devices had to be moved from one facility to the other and were thereby exposed to the argon atmosphere.

4.2 Device Characterization

Fabricated devices were characterized by current/voltage (I/V) measurements, which were performed with an Agilent B1500A parameter analyzer by using two source measurement units (SMUs). One SMU was utilized for applying the bias voltage, while the caused device current was measured with both. Substrates were fixed on a probe station in order to contact the TE and BE with pins. Coaxial cables were used for wiring. Stated bias voltages were always applied on the BE while the TE was grounded. Due to the fact that the evaporation unit and probe station were placed in the glove box cluster, the devices did not have to be exposed to the atmosphere during moving them from one facility to another.

4.2.1 Current/Voltage Characteristics

All investigated memory devices exhibited unipolar device characteristics. Therefore, the switching behavior was technically considered independent of the bias voltage polarity and the introduction of the measurement routines could be limited without concerns to the positive bias voltage range for practical reasons.

Measurement routines were programmed initially on the parameter analyzer and carried out automatically. However, the measurement could be interrupted manually at any time if necessary. During a measurement, the bias voltage was gradually increased by 100 mV steps starting from 0 V. After each step, the bias voltage was held constant for 500 ms while three current measurements were performed automatically. Each current value illustrated in I/V graphs corresponds to the average value of three measurements.

The examination, whether a considered device structure behaves like a reversible switchable memory element, was done by repeated sweeping of the bias voltage over the entire voltage range in which resistance switching was expected. The memory device state was in principal unknown after fabrication. Therefore, it could be in any initial state. Furthermore, it was possible that a newly fabricated device did not exhibit a memory like behavior at all and had therefore to be initialized. This was done by applying high bias voltages (burn-in) or performing several I/V sweeps until an abrupt current increase of more than one order of magnitude was observed (see Chapter 5.4.1). Then the I/V sweep was terminated immediately and started again. If the measured I/V curve exhibited a significantly higher current in the low bias voltage range than compared to the previous sweep, then a HRS (previous sweep) and LRS (current sweep) was observed (please compare with Figure 27a).

In order to determine whether reversible resistance switching between these two states was possible or not, the applied bias voltage was increased further until the local maximum at V_{max} and the NDR range could be observed. The I/V sweep was stopped at the local minimum at V_{min} which specified together with V_{max} the NDR range. Afterwards, a further voltage sweep was started again. If a HRS was revealed and a sudden rise of the current could be observed again, then the device could be switched reversibly.

The bias voltage at which the current increased abruptly was designated as threshold voltage V_T and indicated a state transition of the memory element state from HRS into LRS. If such measurement could be repeated several times, is independent of the applied bias voltage polarity and the set device state maintains without power supply, then the device could be considered as an organic non-volatile, unipolar and reversibly switchable memory element.

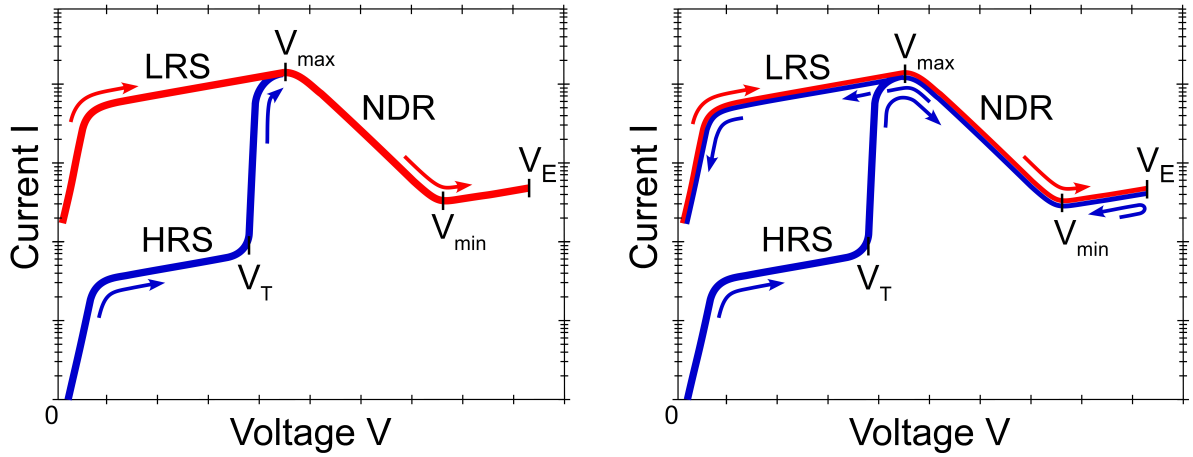
States of the device which were between the HRS and LRS in the I/V plane, were denoted as intermediate states (IMS) and could be programmed by stopping a voltage sweep at an appropriate bias voltage in the range of V_{max} to V_{min} and turning the bias voltage instantaneously to 0 V.

A complete switching cycle consisted of a write and erase operation. Two types of switching cycles were mainly used for device examination. The difference is that the switching into the LRS was performed either by a single sweep or by a double sweep as illustrated in Figure 27a and 27b, respectively.

In case of single sweeps, the device initially exhibited a HRS. Then, the applied bias voltage was increased steadily until resistance switching, which was indicated by an abrupt current increase at V_T, could be observed. Once the local maximum was reached, the bias voltage was turned instantaneously to 0 V. As a result the device was set into a LRS.

In case of double sweeps, the device initially also exhibited a HRS. Here, the bias voltage was swept steadily from 0 V to an erase voltage V_E and back to 0 V. During the I/V measurement, the HRS, LRS and the whole NDR range were revealed. State transitions from HRS into LRS occurred abruptly at V_T as well as continuously from LRS into HRS and vice versa by sweeping the bias voltage along the NDR range. The device exhibited a LRS after performing a double sweep.

The erasing operation was performed by sweeping the bias voltage from 0 V to V_E. The differences between the two switching operations are discussed in Chapter 5.2.1. Alternatively, switching by voltage pulses could be performed by applying a bias voltage of corresponding amplitude (see Chapter 5.2.2).



(a) Switching cycle with single sweep *(b) Switching cycle with double sweep*

Figure 27: *Schematics of complete switching cycles of a unipolar memory element. The device exhibits initially a HRS and is switched into the LRS (blue curves) by (a) a single sweep and (b) a double sweep. Afterwards, it is switched into the HRS again (red curves).*

4.2.2 Long Term Measurements

Long-term measurements were performed in order to investigate the influence of large number of switching operations. Depending on the intended purpose, two different approaches were chosen. Either by performing various voltage sweeps or by applying large number of voltage pulses. In case of voltage pulses, the corresponding bias voltage was applied for each pulse for 500 ms. Additionally, the device response to an applied constant bias voltage as a function of time was investigated.

4.2.3 Probing

Probing was used to determine the state of the memory element by sweeping the bias voltage within the read region starting at 0 V. In order to prevent unintended state transitions, the applied bias voltage amplitude was usually limited to 1 V. Probing is also referred to as reading whereby the current measured at a bias voltage of ± 1 V was used for comparison.

5 Experimental Results and Discussion

5.1 Introduction

In this chapter, organic memory devices, which were fabricated during this work and based on Alq3 as separating material, are introduced and discussed in detail in order to examine the underlying physical mechanism responsible for reversible resistance switching. For this purpose, current-voltage characteristics of various types of single- and multilayer devices were measured, compared and screened for commonalities and differences. Besides repeated switching of the memory element state, the device response to high electric fields as well as long term measurements were investigated. Furthermore, the influence of temperature treatment on newly fabricated devices was elaborated.

5.2 Memory Elements and Programming

Programming (writing and erasing) operations were performed with single memory devices by voltage sweeps and voltage pulses. The former case allowed, in contrast to voltage pulses, to reveal the whole device characteristics in the corresponding bias voltage range from 0 V to the respective read, write or erase bias voltage.

Several studies [41, 42, 54, 60] reported that resistance switching of hybrid organic/inorganic memory elements strongly depends on the morphology of the aluminum inter-layer, which forms separated aluminum nanoparticles (Al NPs) with an oxide shell under appropriate conditions. Based on these findings, similar multilayer memory devices with an ITO/Alq3/Al NPs/Alq3/Ag structure were fabricated for detailed investigations.

Each Alq3 layer exhibited a layer thickness of 30 nm and was covered with an evaporation rate of 1 Å/s. The formation of Al NPs depends on the evaporation process, which, according to Reddy et al. [41], must be performed with an evaporation rate below 1 Å/s under vacuum conditions ($p \approx 1 \times 10^{-6}$ mbar). The average size of the Al NPs increases with increasing Al layer thickness until a layer thickness of 15 nm is achieved. At this point the Al NPs start to coalescence [41]. A continuous film is formed at a sufficient

thick layer of 20 nm or more [54]. Based on these reported data, the Al inter-layer deposition parameters *layer thickness* and *deposition rate* were set to 15 nm and 0.2 Å/s, respectively, for device fabrication.

In order to ensure that the Al NPs were covered with an aluminum oxide (Al_2O_3) shell, the vacuum was broken for 45 min after the evaporation process of the aluminum inter-layer was finished. It is reported, the thickness of the oxide layer should be between 1.5 and 2 nm, regardless of the NPs size due to oxidation under vacuum conditions [54]. The existing oxide shell can grow until the proportion of the metallic core remains with about 50% [42] after exposure to air. We decided to steer a middle course by carrying out the oxidation process under Ar-atmosphere with a residual oxygen content in the ppm range.

Programming of the fabricated ITO/Alq3/Al NPs/Alq3/Ag multilayer memory elements was performed by voltage sweeps and voltage pulses and is discussed in the following sections.

5.2.1 Switching by Voltage Sweeps

The switching operations discussed in this section were performed by increasing the bias voltage steadily starting from 0 V and stopping the voltage sweep manually in the corresponding write or erase region of the memory device I/V characteristics. Details of the investigated ITO/Alq3/Al NPs/Alq3/Ag multilayer memory device structure were already described above.

The completed device had to be initialized first (as described in Chapter 5.4.1) until repeatable resistance switching was observed. In this process, the local minimum (see Chapter 4.2.1) of the I/V curve was found at 5.4 V. The local minimum was not clearly recognizable during measuring the I/V curve, therefore, the erase voltage V_E was set slightly above V_{min} to 6 V.

After the state of the device was erased, two voltage sweeps were performed in order to run through a complete write and erase cycle (see Figure 28). The first sweep was stopped at the presumed local maximum at 3.2 V and revealed the HRS at bias voltages below the threshold voltage V_T of 2.1 V. An abrupt current increase at V_T indicated that a state transition of the memory element from HRS into LRS took place, which decreased the overall device resistance and was completed after reaching the local maximum at V_{max}. The next voltage sweep ranged from 0 V to 6 V. It confirmed the switching into the LRS and revealed the so called bistable region at bias voltages below V_{max}. The negative differential resistance region is specified together with V_{max} and V_{min}, which

were obtained at bias voltages of 3.3 V and 5.3 V, respectively. Device states were determined by the current at the read voltage V_R of 1 V. Characteristic parameters of the I/V curves, which are illustrated in Figure 28, are listed in Table 2.

Table 2: *ITO/Alq3/Al NPs/Alq3/Ag memory device parameters of I/V curves illustrated in Figure 28 on the right. Characteristic currents of HRS and LRS were obtained at a read voltage V_R of 1 V and were used to calculate the on/off ratio.*

Parameter	Voltage [V]	Current [A]
HRS	1	4×10^{-5}
LRS	1	1×10^{-3}
Threshold voltage (V_T)	2.1	1×10^{-4}
Local max. (V_{max})	3.3	8×10^{-3}
Local min. (V_{min})	5.4	1×10^{-3}
On/Off ratio	1	25 [1]

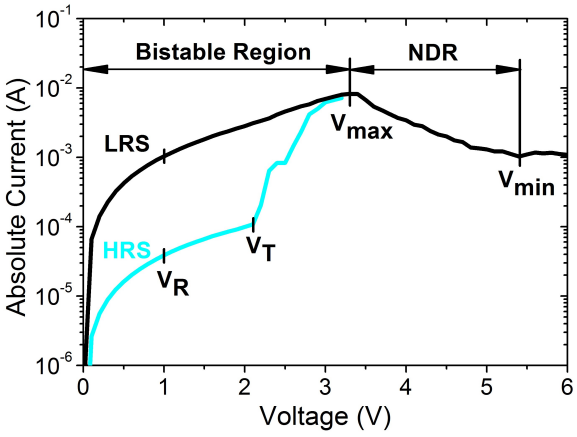
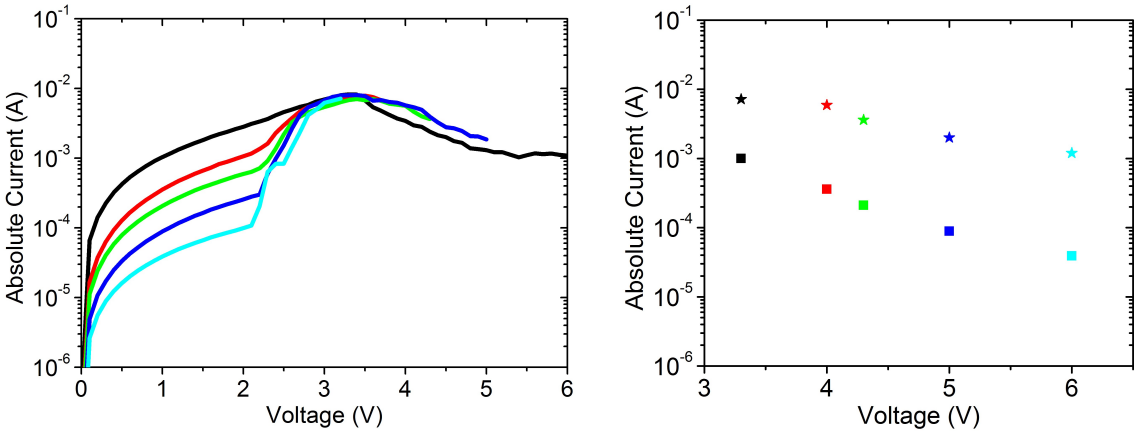


Figure 28: *Write (cyan) and erase (black) operations were performed by I/V sweeps with an ITO/Alq3/Al NPs/Alq3/Ag memory device. Corresponding write and erase bias voltages were* 3.2 V *and* 6 V*, respectively.*

The obtained HRS and LRS were boundary cases limiting the continuous range of possible intermediate states (IMS) of the device in the I/V plane. An IMS was programmed by stopping any voltage sweep within the NDR range and turning the bias voltage instantaneously to 0 V. The following bias voltage sweep revealed the programmed IMS, whose I/V curve was shaped comparably to that of the HRS, but was shifted towards higher currents in the I/V plane. After reaching the threshold voltage, the current increased significantly until the local maximum at V_{max} was reached. All I/V curves were generally congruent at bias voltages higher than V_{max}. However, minor shifts towards higher currents occurred due to variations in device performance. Three different IMS denoted as IMS 1, IMS 2, and IMS 3 in Figure 29a were programmed by stopping the voltage sweep at 4.0, 4.3, and 5.0 V, respectively.

Two different current values can be associated with one specific device state, namely the program current and the read current. The program current is measured during a programming operation is performed and the read current is measured at V_R which is used to determine the programmed state of the device, where $0 < V_R < V_T$. Obtained

program and read currents for all investigated device states are illustrated in Figure 29a and are plotted with respect to the state defining programming voltage in Figure 29b.



(a) *Intermediate states* ***(b)*** *Write and read currents*

Figure 29: *Intermediate states of the investigated ITO/Alq3/Al NPs/Alq3/Ag device with enclosing HRS (cyan) and LRS (black) on the left and state determining write (star symbols) and read currents (square symbols) plotted with respect to the write voltage of the corresponding memory device state on the right. LRS, IMS 1 (red), IMS 2 (green), IMS 3 (blue) and HRS were programmed at 3.2, 4.0, 4.3, 5.0 and* 6.0 V*, respectively. Identical states are colored equally.*

The following important findings could be obtained from Figure 29:

- Each programmed memory device state was non volatile. This was indicated by the fact that the measurement was interrupted after a programming operation was performed and the following I/V measurement still revealed the intended change in the memory device state.
- All characteristic currents increased with increasing bias voltage in the range from 0 V to V_{max}. Such behavior was independent of the programmed device state. Hence, device states exhibiting a higher resistance could only be addressed in the NDR range at bias voltages higher than V_{max}.
- Considering the LRS, each possible program current could be obtained while the bias voltage was swept from 0 V to V_{max}, but no state change could be observed. As a consequence, the applied bias voltage must be considered as state defining parameter in contrast to the measured device current.
- Write and read currents decreased while the corresponding write voltage was increased.

- The difference between the program current and the read current which correspond to one specific state of the memory element increased with increasing program voltage.

In comparison to similar memory devices as reported in [41, 42, 54, 60], in which charging of NPs is proposed as the underlying mechanism for reversible resistance switching, substantial differences could be observed. Instead of an expected abrupt state change at the threshold voltage V_T that was finalized after V_{max} was reached, the transition from HRS into LRS occurred over a voltage range of 1.2 V, which was therefore twelve times larger than compared to one single step of the voltage sweep. This behavior was unexpected due to the fact that switching of the reported devices mainly took place within one single step. The on/off ratio of 25 was lower than compared to similar devices with a 15 nm thick Al layer and an on/off ratio of 1.54×10^2 as reported in [54]. Furthermore, the current of the LRS at V_R was about two orders of magnitude higher than compared to values reported in [54]. Possible explanations for this deviating behavior are discussed in Chapter 5.3.3.

A question of interest was how reliable could different states of a memory device be programmed. For this reason each so far presented device state was programmed three times. The measured I/V curves are plotted in Figure 30 and revealed a relatively stable device performance.

One can observe that the device characteristics were shifted slightly towards higher currents in the NDR range. Single shifts occurred during the measurement and remained for all later measured I/V curves. In this case, a possible explanation could be instabilities in device performance which could not be controlled so far or it could also point to an inherent device property, which influenced the device characteristics and is discussed later in Chapter 5.3.3.

The capability for reversible resistance switching of the investigated devices was independent of the bias voltage polarity and it was, therefore, defined as a unipolar memory device. Additionally, the device characteristics were in general symmetric to the origin of the I/V plane (see Figure 32). The illustrated curves were directly successive measured by performing write and erase operations at bias voltages of ± 3.2 V and ± 6.5 V, respectively.

Setting the device into a LRS by stopping the voltage sweep manually after a significant current increase was observed caused variations of the LRS due to the fact that one could not be sure whether the local maximum was reached or not. As a result, the presumed LRS partly exhibited a step like increase of the current around the threshold

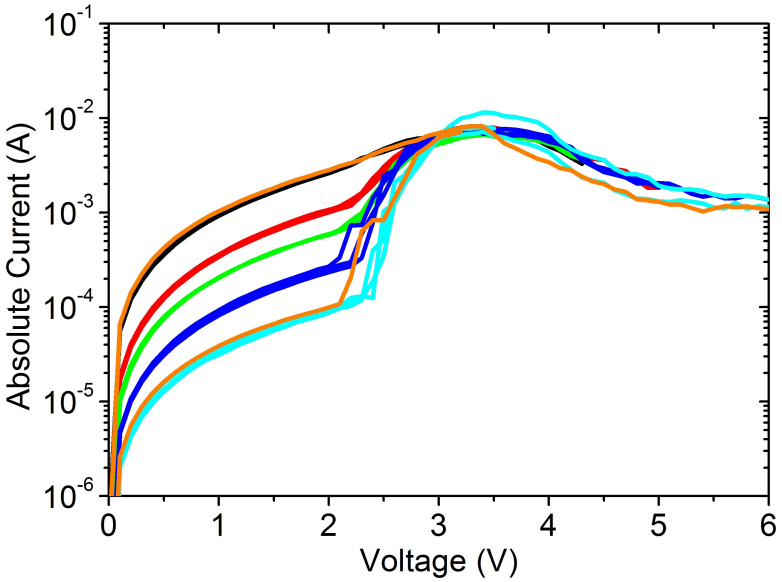


Figure 30: *HRS, LRS and the three IMSs illustrated in Figure 29a were programmed three times consecutively. States set by identical programming voltages are colored equally. The initially discussed HRS and LRS are illustrated additionally as a reference and are colored orange.*

voltage, which indicated that the transition from HRS into the actual LRS was not finished completely. In order to encounter this problem, the LRS write operation could be performed by so called *double sweeps*, which were introduced in Chapter 4.2.1. The differences between these two write operations are illustrated in Figure 31.

The memory device was first programmed into a LRS and erased afterwards by single voltage sweeps, which were stopped at the presumed local maximum at $-3.2\,\mathrm{V}$ and at an erase voltage of $-6.5\,\mathrm{V}$, respectively. Subsequently, the bias voltage was swept from $-6.5\,\mathrm{V}$ to $0\,\mathrm{V}$ in order to write a LRS. The current increased until the local maximum was reached. Afterwards the memory element remained in the actual LRS. Its read current at $-1\,\mathrm{V}$ was five times higher than compared to the LRS written by stopping the I/V sweep manually at the presumed local maximum. Such behavior was independent of the applied bias voltage polarity, therefore, the memory device could be considered as unipolar. Measured device characteristics were generally symmetric to the origin of the I/V plane (see Figure 32).

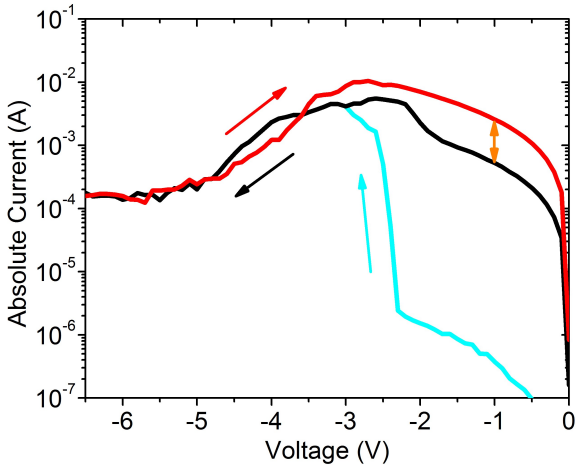


Figure 31: *Two ways to switch from HRS into LRS: Either, stopping the voltage sweep after the presumed local maximum (cyan curve) was reached and, therefore, risking not to write the actual LRS (black curve) or sweeping the bias voltage back to* 0 V *(red curve) after erasing the ITO/Alq3/Al NPs/Alq3/Ag device at* −6.5 V*. The difference in the written LRS states is indicated by the orange arrow.*

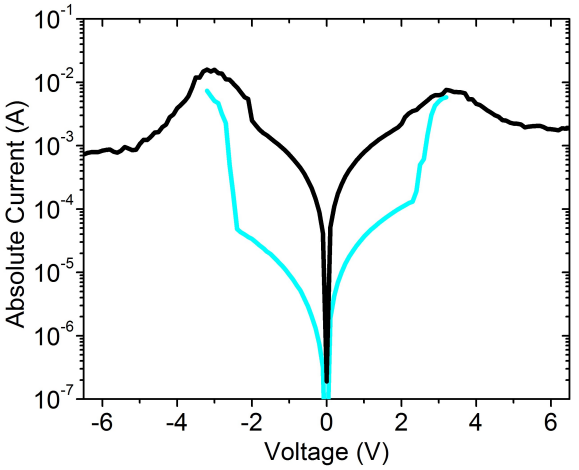


Figure 32: *I/V characteristics of an ITO/Alq3/Al NPs/Alq3/Ag device. Absolute current values are plotted in order to improve comparability. Cyan curves were measured after erasing the device at* ±6.5 V*. Switching from HRS into LRS was performed by stopping the voltage sweep at the presumed local maximum.*

5.2.2 Switching by Voltage Pulses

Resistance switching can also be performed by voltage pulses, which amplitude corresponds to the write-, or erase bias voltage range of the corresponding device characteristics. The pulse duration was set to 500 ms which was as long as the standard hold time of a single measurement point of any voltage sweep. Studied memory elements exhibited an ITO/Alq3/Al NPs/Alq3/Ag structure, its fabrication was already explained in Chapter 5.2. In order to determine optimal parameters for programming, a memory element was initialized and then switched repeatedly by I/V sweeps. I/V curves of one write-erase cycle are illustrated in Figure 33. Based on these device characteristics, bias voltage amplitudes of $-3\,\mathrm{V}$ and $-6.5\,\mathrm{V}$ were chosen for write and erase operations, respectively.

The bias voltage polarity generally had no influence on the device ability for reversible resistance switching and was changed for practical reasons. Characteristic parameters of the obtained I/V hysteresis are listed in Table 3.

Table 3: *ITO/Alq3/Al NPs/Alq3/Ag memory device parameters of I/V curves illustrated in Figure 33 on the right. Characteristic currents of HRS and LRS were obtained at a read voltage V_R of $-1\,\mathrm{V}$ and were used to calculate the on/off ratio.*

State	*Voltage*[*V*]	*Current*[*A*]
HRS	-1	3×10^{-7}
LRS	-1	3×10^{-4}
Threshold voltage (V_T)	-2.7	4×10^{-6}
Local max. (V_{max})	-2.2	3×10^{-3}
Local min. (V_{min})	-6.2	6×10^{-5}
On/Off ratio	-1	10^3 [1]

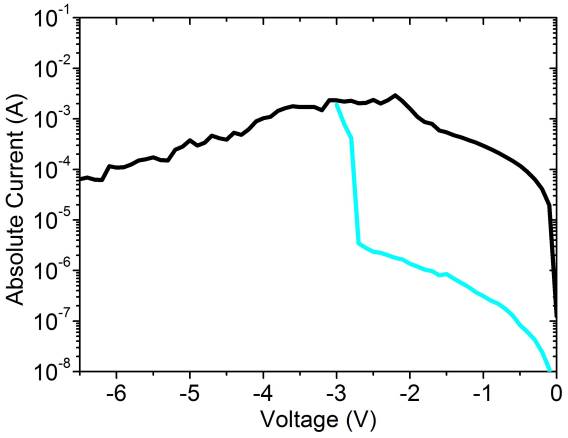
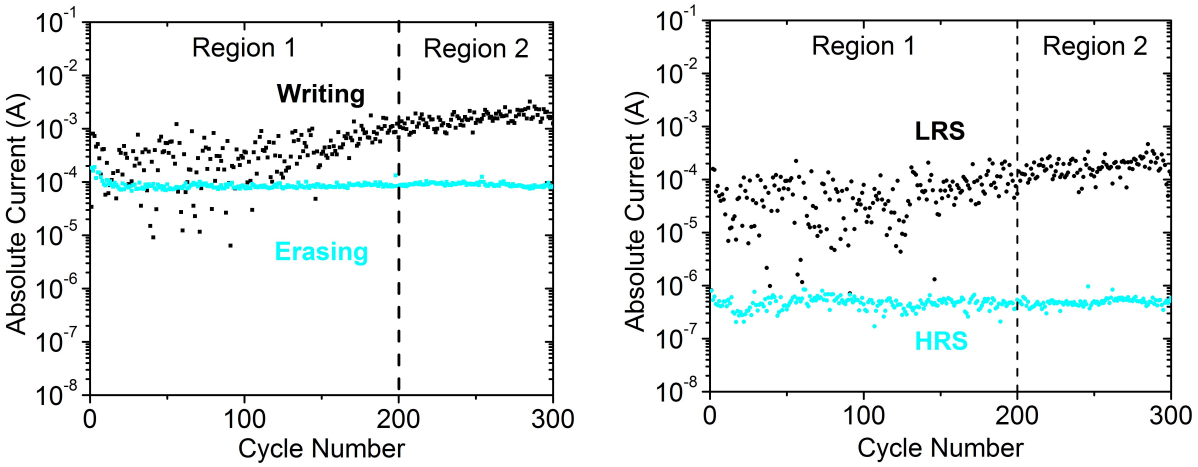


Figure 33: *Measured I/V sweeps of an ITO/Alq3/AlNPs/Alq3/Ag device during run in reverse direction. LRS (black curve) and HRS (cyan curve) were programmed by stopping the voltage sweep at bias voltages of $-3\,\mathrm{V}$ and $-6.5\,\mathrm{V}$, respectively.*

Switching by voltage pulses was performed in cycles. Each cycle consists of four consecutively performed operations, namely:

1. Write a LRS by applying a $-3\,\mathrm{V}$ voltage pulse.
2. Read the written state of the device by applying a $-1\,\mathrm{V}$ voltage pulse.
3. Erase the state of the memory element by applying a $-6.5\,\mathrm{V}$ voltage pulse and
4. Read the state of the device again by applying a $-1\,\mathrm{V}$ voltage pulse.

This cycle was repeated several times. Characteristic currents of the first 300 cycles are illustrated in Figure 34.



(a) Programming *(b) Reading*

Figure 34: *Program and read currents of a repeated switched ITO/Alq3/Al NPs/Alq3/Ag memory device are plotted with respect to the cycle number. Read, write, and erase operations were performed at $-1\,\mathrm{V}$, $-3\,\mathrm{V}$, and $-6.5\,\mathrm{V}$, respectively.*

The cycle number range illustrated in Figure 34 was divided into region 1 and region 2, which ranged from cycle number 1 to 200 and 201 to 300, respectively. The following discussion refers to absolute values of the applied bias voltages and characteristic currents for practical reasons.

Program and read currents of the LRS exhibited relatively strong variations over one and respectively two orders of magnitude in region 1, which were markedly reduced in region 2. Such behavior could be ascribed to variations of the threshold voltage and made the necessity of device initialization until a stable performance was observed evident. Erasing and HRS read currents were not significantly affected by 300 switching operations.

Strong variations of the write and LRS read currents could be ascribed to variations of the threshold voltage. If the initially defined write voltage was lower than the actual threshold voltage of the investigated memory element during a write operation was performed, then the intended write operation did not take place and the memory device remained in the HRS. As a consequence, the measured write current corresponded to the HRS and was therefore lower than the erase current (see Figure 34). This phenomenon was also subject of a closer examination and is discussed in detail in Chapter 5.3.1.

Write currents comparable to erase currents could be attributed in case of filamentary conduction to a partially reformation of the filament, which set the device into an IMS. Considering the initially discussed device in Chapter 5.2 (see Figure 28), its transition from HRS into LRS took place over a voltage range of 1.2 V, helps to understand the origin of strong write current fluctuations in region 1 (see Figure 34a). The data suggested that a similar behavior could be considered due to which V_T was shifted towards 0 V while V_{max} remained more or less constant. If the initially defined write voltage was between the shifting threshold voltage and V_{max}, then the device was set into an IMS. As a consequence, an increased write current was measured as well as a higher read current during the following read operation. Once, switching behavior was stabilized, the fluctuations were substantially reduced which could be observed especially in region 2. In order to explain this process, it is strongly believed that during device initialization material transport along the filament took place which provided additional material for extending the filament. If enough material was available at the rupturing region, then the switching process was stabilized and the write currents as well as LRS read currents started to increase due to the extended filament. As a consequence, the filament exhibited a reduced electrical resistance.

Comparable low variations of the write and LRS read currents in region 2 indicated that the threshold voltage was shifted permanently to bias voltages below the initially defined write voltage and the fluctuations were due to variations of V_{max}. Furthermore, V_{min} exhibited comparable variations, which resulted in minor fluctuations of the erase and HRS read currents. Such behavior could again be explained by filamentary conduction where the shape of the filament at the rupturing region was subject of random variations and, therefore, influenced the local electrical field strength as well as the filament formation process. The obtained I/V curves were in agreement with those reported by Sebastian et al. in 2011 [61], who performed comparable measurements with ITO/Alq3/Al and ITO/Alq3/Ag memory device structures. Filament formation was suggested as responsible switching mechanism such as discussed in [56, 58].

The investigated device exhibited incorporated oxide shell Al NPs, because the initial intention was to investigate reversible resistance switching based on charging of deliberately embedded Al NPs as reported in [41, 42, 54, 60]. However, based on further investigations, it turned out that oxide shell Al NPs were not necessary for the observation of unipolar and reversible resistance switching in organic memory devices. Alternatively, switching due to accidentally introduced NPs as a consequence of evaporating the TE as suggested by Tang et al. [62] in 2005 could also be a possible explanation and the origin of filamentary conduction in organic unipolar memory devices.

5.2.3 Conclusion

Within this section it was shown that switching between the HRS and LRS could be performed by I/V sweeps and voltage pulses. The investigated hybrid organic/inorganic memory devices exhibited an ITO/Alq3/Al NPs/Alq3/Ag multilayer structure and showed reversible resistance switching independent of the bias voltage polarity. The device characteristics were generally symmetric to the origin of the I/V plane. The programmed device state only depended on the last applied bias voltage that corresponds to the program region, which is specified together with the threshold voltage V_T and the local minimum at V_{min} of the I/V characteristics. Applying bias voltages within the NDR range set the device reliably into an IMS, its I/V characteristics were between those of the HRS and LRS boundary states in the bias voltage from 0 V to V_{max}.

The advantage of switching the device state by I/V sweeps was that the whole device characteristics were revealed, but with the consequence that the device also underwent higher stress. In order to reduce the device stress and to perform also a large number of switching cycles, switching by voltage pulses was introduced what was particularly important with regard to potential memory applications.

One major disadvantage regarding switching the device into LRS was the fact that it was not possible to ensure that the applied bias voltage corresponded indeed to V_{max}. Therefore, switching by sweeping the bias voltage from V_E to 0 V (double sweeps) provided a practical solution. Switching the device into the HRS faces similar problems, which could be overcome by the assumption that bias voltages slightly higher than V_{min} also set the device into the HRS. Switching by voltage pulses with constant bias voltages for write and erase operations faced the same problem. Only an examination of the device performance over a large number of switching cycles in combination with I/V sweeps allowed to draw conclusions which kind of states were observed and how the device characteristics were affected.

In order to overcome these problems, memory elements exhibiting relatively stable switching behavior and large on/off ratios must be developed. Reported on/off ratios of 10^5 [41] for I/V sweeps performed with similar device structures but with an overall Alq3 layer thickness of 100 nm could not be reproduced. Possible explanations for this deviation could only insufficiently be attributed to variations in device structure and will be discussed more detailed in the following chapters. However, the investigated devices showed unipolar and reversible resistance switching, which was performed by voltage sweeps and voltage pulses. Furthermore, the studied memory elements exhibited a relatively stable performance after device initialization. This made the necessity of running-in processes evident.

5.3 Long Term Measurements

Long term measurements were used to investigate the influence of a large number of switching operations on the device characteristics as well as the response to applied constant bias voltages for a period lasting significantly longer than the standard hold time of 500 ms for single I/V measurement points.

5.3.1 Sub-Threshold Switching

The threshold voltage indicated at which bias voltage the device current increased sharply due to an abrupt transition from HRS into LRS. Threshold voltages varied over a certain bias voltage range even if write and erase voltages were hold constant. Now the question arose, whether a switching process from HRS into LRS could be forced by applying a certain sub threshold bias voltages V_{ST} where $0 < |V_{ST}| < |V_T|$. The investigations were performed with a memory element exhibiting an ITO/Alq3/Al NPs/Alq3/Ag structure. Each Alq3 layer was 30 nm thick. The investigation of sub threshold switching was performed by applying a constant bias voltage V_{ST} after an erasing operation was performed at -6.5 V. The complete measurement routine consisted of 5 parts, in particular:

1. A LRS was written by decreasing the bias voltage steadily starting at 0 V until a state transition from HRS into LRS was supposed to be finished. Afterwards, the device was erased again by performing an additional voltage sweep ranging from 0 V to an erase voltage of -6.5 V.

2. The programmed HRS was confirmed by sweeping the bias voltage from 0 V to a certain sub threshold voltage V_{ST}, where $0 < |V_{ST}| < |V_T|$ with the V_T value from point 1.

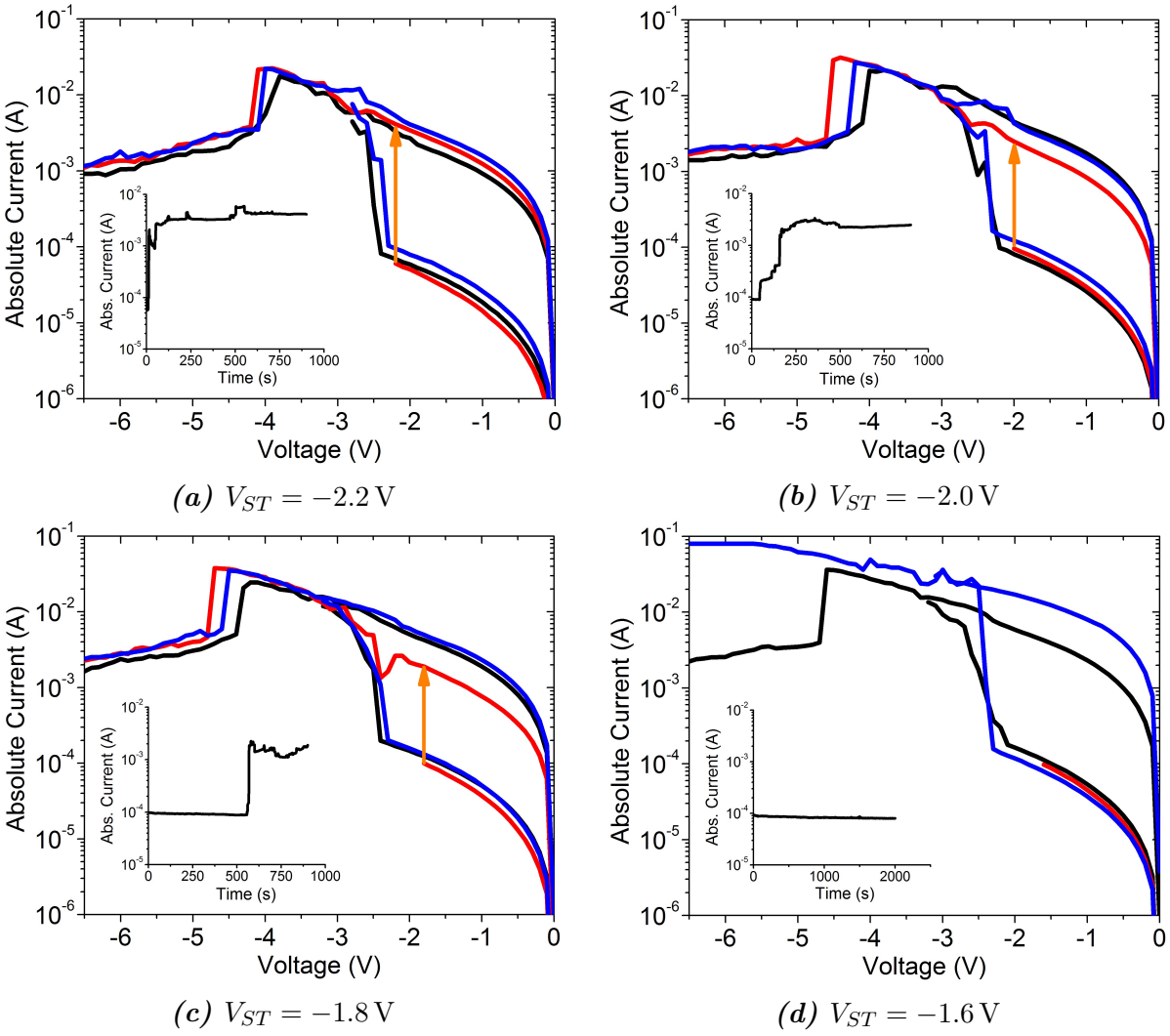
3. A current measurement over time (I/V-t measurement) was performed with a constant bias voltage of V_{ST} until a step like increase in current, which indicated a switching process, was observed.

4. Confirmation of the state transition was done by sweeping the bias voltage from 0 V to the erase voltage. In this process, the written device state was revealed and the memory device was erased again.

5. Repeat point 1) in order to check for variations of V_T.

This procedure was conducted for different sub threshold voltages of −2.2 V, −2.0 V, −1.8 V, and −1.6 V. The obtained I/V and I/V-t curves are illustrated in Figure 35. Threshold voltages observed during writing operations performed by I/V sweeps (part 1 and 5) were mostly between −2.4 V and −2.2 V and, therefore, varied insignificantly. Sub threshold switching could be observed indeed for sub threshold voltages of −2.2 V, −2.0 V, and −1.8 V and occurred after V_{ST} was applied for 10 s, 156 s, and 567 s, respectively. The I/V-t measurement performed at −1.6 V was terminated after 2000 s due to the fact that no switching could be observed. Delay time of switching events increased disproportionately with decreasing absolute values of V_{ST}. The threshold voltage was shifted by more than 20% from about −2.3 V to −1.8 V due to time delayed switching. As a consequence, the applied average electric field along the device contact electrodes was also decreased proportionally during the state transition and, therefore, also the electric field strength at the rupturing region of filament which is suggested as responsible for atomic transport and the reformation process.

The obtained results were in agreement with findings as reported in [63]. Similar experiments were conducted by You et al. [52] who studied time delayed switching as a function of temperature and layer thickness and suggested filament formation due to migration of metal atoms under high electric fields as a possible explanation. Such formation process is independent of the bias voltage polarity and is therefore capable to explain symmetric I/V characteristics as well as increased delay time due to cooling the device, increasing the layer thickness or reducing the average electric field by applying sub threshold voltages. The reported delay times for the latter case range from a few seconds to 10^4 s.[52]



(a) $V_{ST} = -2.2\,\mathrm{V}$ *(b)* $V_{ST} = -2.0\,\mathrm{V}$

(c) $V_{ST} = -1.8\,\mathrm{V}$ *(d)* $V_{ST} = -1.6\,\mathrm{V}$

Figure 35: *Investigation of resistance switching at sub threshold bias voltages* V_{ST} *of a)* $-2.2\,\mathrm{V}$*, b)* $-2.0\,\mathrm{V}$*, c)* $-1.8\,\mathrm{V}$*, and d)* $-1.6\,\mathrm{V}$*. Programming operations were performed by voltage sweeps before and after sub threshold switching was investigated. The corresponding I/V curves are colored black and blue, respectively. Red curves indicate the HRS in the range of* $0\,\mathrm{V}$ *to* V_{ST} *and the programmed LRS due to I/V-t measurements performed at* V_{ST} *for a certain period (see inset graphs). The write process at* V_{ST} *is suggested by orange arrows. Erase operations are always performed by sweeping the bias voltage form* $0\,\mathrm{V}$ *to* $-6.5\,\mathrm{V}$*.*

5.3.2 Voltage Pulses

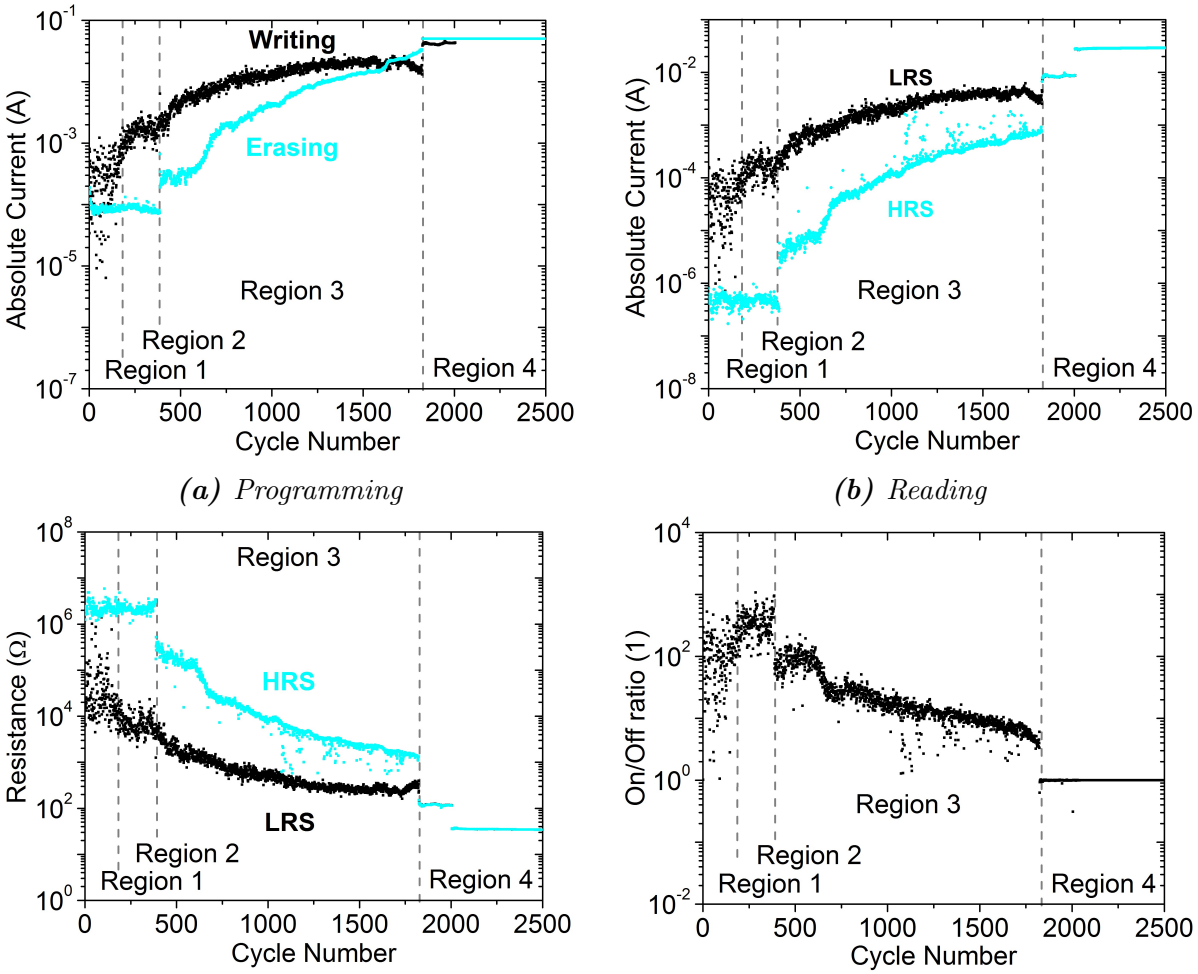
Characteristic parameters such as V_T and the LRS can be influenced by the measurement routine. Now, with regard to potential memory applications, the question arises if and how do large numbers of write and erase operations influence the device characteristics. In order to examine these questions, two complementary methods were chosen for investigation. The previously introduce switching by voltage pulses was used to perform a large number of switching cycles. Additionally, memory devices were switched repeatedly by voltage sweeps in order to reveal the complete device characteristics. Presented measurements were performed with identical ITO/Alq3/Al NPs/Alq3/Ag memory devices with which programming by voltage pulses was introduced. Initially discussed graphs were limited to the first 300 of 2500 switching cycles in total, because the focus was previously on device initialization as well as programming and not on the evolution of characteristic device currents with increasing cycle number. Bias voltages for read, write and erase operations were therefore $-1\,\mathrm{V}$, $-3\,\mathrm{V}$, and $-6.5\,\mathrm{V}$, respectively. Obtained device characteristics are plotted with respect to the cycle number in Figure 36. Four different regions could be observed:

Region 1 ranged from cycle number 1 to 200 and exhibited the strongest fluctuations of the LRS, which made the necessity of device initialization evident. We suspect that they originated from variations of the local maximum and the threshold voltage where V_T could either be higher or lower than the initially defined V_{Write}. For detailed explanation see Chapter 5.2.2.

Relatively stable device performance could be observed in Region 2, which ranged in this case from cycle number 200 to 386. The remaining cycle number range was divided at cycle number 1824 in Region 3 and 4 in which significant change of the characteristic currents could be observed.

The overall trend was a steady shift of the device characteristics towards higher currents (see Figure 36a and 36b) until the current compliance of $50\,\mathrm{mA}$ was reached in region 4. As a result, the device resistance at the read voltage decreased, accordingly to Ohm's law, inverse proportional to the current (see Figure 36c). Clearly distinguishable device states approached each other with increasing cycle number what caused a continuous decrease of the on/off ratio in region 3. The current increased abruptly at the end of region 3 and a constant on/off ratio of one in the adjacent region 4 indicated that the memory device was damaged and lost the ability for reversible resistance switching.

Comparable results were reported for ITO/Alq3/Al and ITO/Alq3/Ag memory devices by Sebastian et al. [61], who suggested filament formation as the underlying



(a) Programming *(b) Reading*

(c) Resistance *(d) On/off ratio*

Figure 36: *Read, write, read, and erase operations were performed cyclically and the obtained characteristic currents are plotted with respect to the cycle number. The illustrated device resistances were calculated by Ohm's law and the measured read currents. On/off ratios were calculated by the ratio of the reading currents of the corresponding cycle number. Read, write, and erase operations were performed at* $-1\,\mathrm{V}$, $-3\,\mathrm{V}$, *and* $-6.5\,\mathrm{V}$, *respectively.*

mechanism responsible for reversible resistance switching. It is important to stress that besides filamentary conduction, where metallic bridges [53] connect the two contact electrodes, also the formation of high conductive pathways [64] with variable conductivity is thinkable. Both mechanisms are in contrast to charging of NPs highly localized effects, which strongly depend on the local conditions of the switching region.

Minor fluctuations of characteristic currents within just a few cycles could be attributed to random variations of these localized conditions. Filament formation (switching into the LRS) strongly depends on the local electric field strength and, therefore, on the shape of the remaining filament in the rupturing region. In case of smoother surfaces, the localized electric field was reduced. As a consequence, the device required either a higher absolute write voltage in order to complete the filament formation on time or a longer pulse period which, however, was limited to 500 ms. These assumptions were in accordance with the previously introduced sub threshold switching and explain minor variations of the LRS. Minor variations in HRS could be explained by the assumption that the filament was completely ruptured and the remaining parts acted as a high conductive pathway with varying conductivity.

The characteristic currents rose rapidly at cycle number 387, which indicated a significant change in device performance. Within certain limits, a constant HRS read current increased by about one order of magnitude and tended to rise steadily afterwards. Comparable behavior could be observed for the erase current, whereby the sudden increase was less pronounced. Write and LRS read currents also increased steadily with increasing cycle number but did not exhibit abrupt changes. The formation of additional filaments could explain the increased characteristic currents.

Alternatively, an influence on the switching region due to repeatedly resistance switching is thinkable. Material was released from the contact electrodes, migrates through the device, and extends the already existing filament. After extending the filament at the rupturing region, the initially set erase voltage of $-6.5\,\mathrm{V}$ was not sufficient to rupture the formed filament completely. As a consequence, the erase current and HRS read current increased abruptly within one cycle and the programmed HRS was actually an IMS, which was indicated by an increased read current measured during the directly following read operation. Furthermore, a permanent connected filament may also support atomic transport which lead to a further extension and, therefore, to a steadily decrease of the device resistance with an increasing cycle number (see Figure 36c).

Isolated abrupt changes of HRS read current appeared in the range from cycle number 1000 to the end of region 3. During the following cycle(s) the memory device showed

again reversible resistance switching comparable to cycles measured just before the isolated abrupt change was observed. Such major deviations appear likewise in the on/off ratio and in the device resistance graph, due to the fact that these device parameters depend on the measured HRS read currents. Their origin could be related to random variations of the switching mechanism, which appeared more often with increasing cycle number (e.g. around cycle number 1250) and, therefore, with increasing characteristic currents. Previously discussed influences on the switching region could be used as explanation. During one write operation, the filament was more extended as usual due to disproportional material transport and the applied erase voltage pulse was not sufficient to erase the state of the device. The actually programmed device state was determined by the read operation and exhibited a lower resistance, which could even be comparable to the LRS. The following write and read operation switched the memory element into the normal LRS and confirmed a state transition into LRS, respectively. The next erase operation was then capable to erase the state of the device again or program it into an IMS with at least higher electrical resistance. This argumentation also applied for two abrupt and irreversible current increases in region 4 at cycle number 1824 and 2006. The process was initially the same, random variations lead to a disproportional extension of the filament but, in this case, the cyclic applied erase voltages were not sufficient to reset the device in a state with higher resistance values. As a result, the device lost the ability for reversible resistance switching, which was confined by a unity on/off ratio in region 4.

Due to the abrupt increase of the HRS read current at cycle number 387 and in combination with its steadily increase with increasing cycle number, the maximum on/off ratio of three orders of magnitude appeared in region 2 at cycle number 285.

5.3.3 Voltage Sweeps

Repeated switching by voltage sweeps was performed with two different memory device structures. First, the measured device characteristics of an ITO/Alq3/Al NPs/Alq3/Ag memory element were discussed and compared with results obtained from switching by voltage pulses. Identical device structures (they were located on the same substrate) and equal bias voltages for read, write and erase operations allowed a direct comparison as well as a combination of the obtain results. Secondly, memory elements without incorporated aluminum oxide shell NPs were investigated.

Switching of the ITO/Alq3/Al NPs/Alq3/Ag device was performed by decreasing the bias voltage steadily starting at 0 V and stopping the voltage sweep at the write or erase

voltage. Write and erase voltages were set for comparison with switching by voltage pulses to $-3\,\mathrm{V}$ and $-6.5\,\mathrm{V}$, respectively. The device current at $-1\,\mathrm{V}$ was associated with the read current.

After device initialization, six sets of write and erase operations were performed. The first and last set is illustrated in the middle of Figure 37. The obtained results were in good agreement with observations made on switching by voltage pulses. Within five switching cycles, characteristic currents were shifted significantly towards higher currents. The HRS read current was increased due to repeated switching from $3.1 \times 10^{-7}\,\mathrm{A}$ to $1.2 \times 10^{-5}\,\mathrm{A}$, whereby a major step of about one order of magnitude occurred during one single sweep. Erase currents increased meanwhile from $6.4 \times 10^{-5}\,\mathrm{A}$ to $6.6 \times 10^{-4}\,\mathrm{A}$. Similar behavior was also observed in case of switching by voltage pulses (see Figure 36b). An excerpt of already presented data is illustrated for comparison to the left and to the right in Figure 37. Horizontal lines indicate characteristic currents of the first and last set of switching operations. Performed I/V sweeps made the evolution of the device characteristic due to repeated resistance switching by voltage sweeps, especially in case of HRS read and erase currents, evident. Initially obtained characteristic currents (solid lines) were in good agreement with currents obtained during switching by voltage pulses at cycle numbers that correspond to region 2. As a consequence, a good comparability of both presented devices was enabled. Dashed lines map characteristic currents after five sets of switching operations performed by voltage sweeps. Their intersections with data of switching by voltage pulses were in case of HRS read and erase currents around cycle number 630. Therefore, switching by voltage pulses required in this case at least 250 cycles in order to evolve the device characteristic correspondingly.

The significant deviation could be related to increased stress due to voltage sweeps and of cause random variations in device performance, which cannot be controlled so far. In case of switching by voltage pulses, each operation lasted 500 ms. Write and erase operations performed by sweeping the bias voltage required 15.5 s and 33 s, respectively. Erasing the device stressed most due to the fact that the device was initially in the LRS and, as a result, the dissipated power was in the range from 0 V to V_{Write} increased by a factor that corresponded to the on/off ratio. Sweeping the bias voltage further to V_{Erase} made also an additional contribution to the overall dissipate power, which heated up the device locally. The temperature is, besides electric field strength and duration, an important parameter for filament formation. Only a slight change could be observed in case of the LRS read and write currents, which was comparable to the minor variations of the LRS read and write currents and, therefore, not significant.

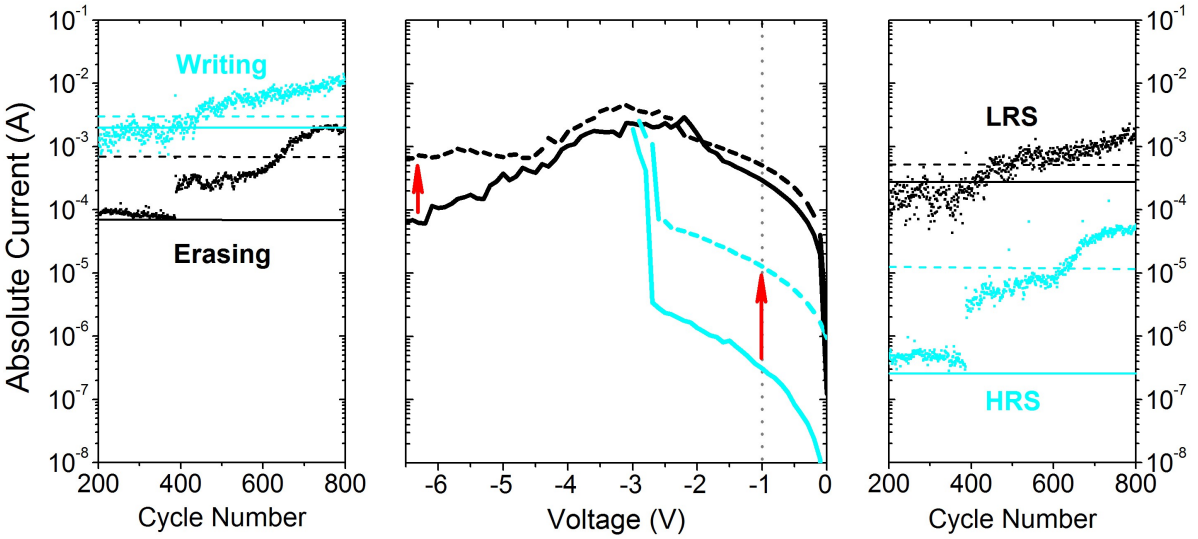


Figure 37: *Evolution of ITO/Alq3/Al NPs/Alq3/Ag memory device characteristics due to voltage pulses (left and right) and voltage sweeps (middle). Write and erase operations were performed at bias voltages of* $-3\,\mathrm{V}$ *and* $-6.5\,\mathrm{V}$*, respectively. Horizontal lines correspond to characteristic currents of illustrated I/V sweeps in the middle. Red arrows indicate the shift towards higher currents due to five cycles of write and erase operations performed by voltage sweeps.*

The on/off ratio decreased with increasing cycle number from about three orders of magnitude to about 40, which was also in agreement with previously obtained findings.

Postulated resistance switching mechanisms, which base on formation of metallic filaments or high conductive pathways do not require deliberately incorporated metallic NPs. Therefore, a simpler device structure was chosen for further investigations. It consists of a single layer of Alq3 between an ITO and Ag contact electrode. The Alq3 and Ag layers were both 300 nm thick. The main difference compared to previously incorporated devices was that this type of memory element did not exhibit incorporated NPs and the organic layer thickness was increased by a factor of five. The device was temperature treated at 100 °C under vacuum conditions during preconditioning (see Chapter 5.5). The change of the device characteristics due to long term measurements was investigated in the positive and negative voltage range by voltage sweeps. In order to improve the comparability, switching from the HRS into the LRS was performed by double sweeps. One write and erase operation was again combined to one switching cycle. Erase operations were performed by sweeping the bias voltage from 0 V to $\pm 7\,\mathrm{V}$. Currents caused by a bias voltage of $\pm 1\,\mathrm{V}$ were used to determine the device state and are denoted as read currents.

The investigated device was initialized by performing two switching cycles in the positive bias voltage range whereby bistable behavior could be observed right from the beginning. Afterwards, one switching cycle was performed each in the positive and negative bias voltage range. Measured I/V curves were used as a reference for investigation of the evolution of the device characteristics due to repeated switching (see Figure 38). The investigated bias voltage range revealed the overall device characteristics with local minima at $-5.2\,\mathrm{V}$ and $6.3\,\mathrm{V}$, which specify together with local maxima at $-2.8\,\mathrm{V}$ and $2.7\,\mathrm{V}$ the NDR ranges of $2.4\,\mathrm{V}$ and $3.6\,\mathrm{V}$ under negative and positive bias voltage polarity, respectively. Obtained HRS read currents of $1.3 \times 10^{-7}\,\mathrm{A}$ and $5.5 \times 10^{-7}\,\mathrm{A}$ indicated that erase voltages of $\pm 7\,\mathrm{V}$ set the device into comparable states. Two different LRSs of the initially measured reference curves could be observed. The lower LRS exhibited a read current of $1.5 \times 10^{-4}\,\mathrm{A}$ and was written during the switching operation in the positive bias voltage range. Hence, it should be symmetric to the origin at low bias voltages. This was confirmed during the erase operation of the following switching cycle, which exhibited a read current of $-1.4 \times 10^{-4}\,\mathrm{A}$. The following write operation revealed the HRS of the negative bias voltage range and programmed a higher LRS, which exhibited a read current of $6.7 \times 10^{-4}\,\mathrm{A}$. Shifts of LRSs towards higher currents in the I/V plane were irreversible and were indeed a feature of evolving device characteristics.

Subsequently, ten switching cycles were performed in order to study the evolution of device characteristics. The final two double sweeps are plotted for comparison with the initial ones in Figure 38. I/V curves in the negative bias voltage range were always measured directly after the previous switching cycle in the positive bias voltage range was finished.

The main finding was a significant change in characteristic parameters (HRS and LRS read currents as well as write and erase currents), which depended on the bias voltage polarity. LRS read current was increased from $1.5 \times 10^{-4}\,\mathrm{A}$ to $7.4 \times 10^{-4}\,\mathrm{A}$ in the positive bias voltage range. Symmetric states could be observed again, if the bias voltage polarity was changed between two switching cycles. The position of the local maximum was clearly influenced. First, I_{max} was increased accordingly to the LRS read current and V_{max} was additionally shifted towards the corresponding erase voltage from $-2.8\,\mathrm{V}$ and $2.7\,\mathrm{V}$ to $-3.5\,\mathrm{V}$ and $3.8\,\mathrm{V}$, respectively. Local minima of the device characteristics underwent a similar shift, which was much more pronounced in the positive bias voltage range. As a result the NDR regions ranged from $-6.5\,\mathrm{V}$ to $-3.5\,\mathrm{V}$ and from $3.8\,\mathrm{V}$ to at least $7\,\mathrm{V}$. The local minimum could not be observed in the investigated positive bias voltage range. Hence, the device state set by an erase voltage of $7\,\mathrm{V}$ was

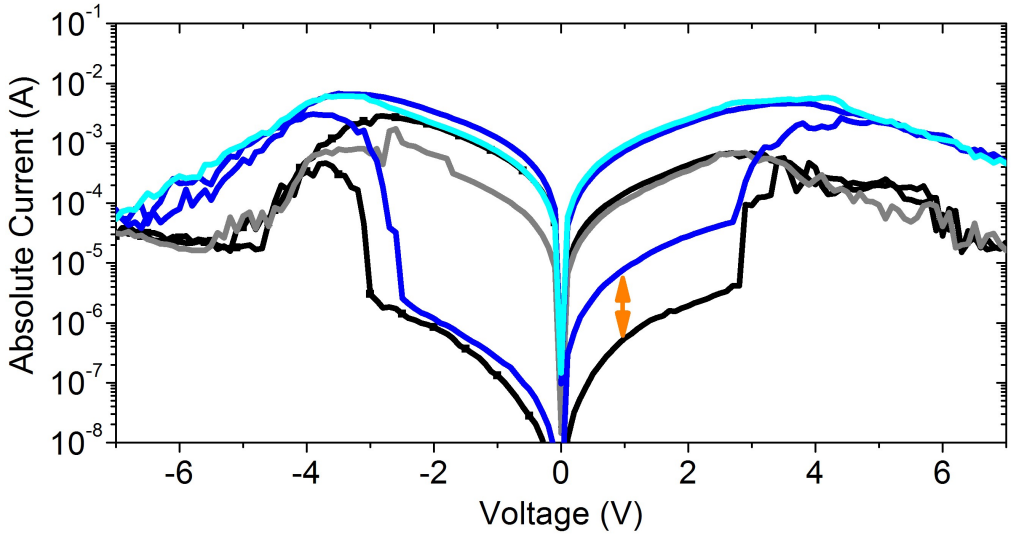


Figure 38: *Asymmetric evolution of ITO/ALq3/Ag memory device characteristics due to repeatedly switching by voltage sweeps. Illustrated switching cycles were measured before (black and grey curves) and after (blue and cyan curves) 10 switching cycles were performed. Each switching cycle consists of an erase operation (cyan and grey curves) which was followed by a write operation (black and blue curves). The erase voltage was set to* $\pm 7\,\mathrm{V}$.

actually an IMS determined by a read current of $8.1 \times 10^{-6}\,\mathrm{A}$, which was more than one order of magnitude higher than the HRS read current of the following switching cycle in the negative bias voltage range. Obtained on/off ratios of 90 and 4600 of the final I/V characteristics as well as different NDR ranges appeared also during the following measurements. Therefore, random variations in device performance could be excluded and the asymmetric evolution of the device characteristic is indeed a significant device property, which must be explained by the physical processes suggested as underlying mechanisms for organic memory devices based on reversible unipolar resistance switching. These asymmetric evolution, which depended on the bias voltage polarity, suggests that memristor like behavior is part of a complete description of the physical mechanisms responsible for reversible resistance switching.

Based on these measurements, it is possible to draw the conclusion that besides the formation of additional filaments also a change in the switching region of the filament(s) must be considered. This is in good agreement with the previously introduced mechanism of material transport from the top electrode towards the switching region, which leads to a extended filament which could not be completely ruptured. The asymmetric

evolution may originate from additional atomic transport due to electromigration, which depends on the bias voltage polarity.

The findings are comparable with the ITO/Alq3/Al NPs/Alq3/Ag structure and suggest that the incorporation of Al NPs is not necessary.

5.3.4 Asymmetric Device Characteristics

Properties of an asymmetric device characteristic are discussed in this section. For this reason, ITO/Alq3/Ag memory devices were fabricated. The Alq3 layer was 300 nm thick. In order to accelerate the evolution of the device characteristics during device initialization a temperature treatment was performed under vacuum conditions at 100 °C (for more details see Chapter 5.5) after the device fabrication was finalized. First, HRSs were investigated in the positive and negative bias voltage range. Then, programming with bias voltages which correspond to the extended NDR range and, in this process, the change of characteristic parameters was elaborated. Finally, specific device states were investigated in both bias voltage ranges.

The local minimum was obtained at −5.5 V while the memory element was erased by sweeping the bias voltage from 0 V to −6 V. Afterwards, a double sweep was performed within the same bias voltage range, which revealed the appropriate HRS, LRS, and NDR range (see Figure 39a). Measured read currents of the HRS and LRS of 1.0×10^{-9} A and 1.3×10^{-4} A, respectively, resulted in an on/off ratio of five orders of magnitude at −1 V. The state transition from HRS into LRS occurred at a threshold voltage of −2.8 V during the double sweep. The device exhibited a NDR region that ranged from −5.8 V to −2.7 V and extended therefore over a voltage range of 3.1 V. Due to the performed double sweep, the state of the memory device corresponded to the LRS in the end of the switching operation.

Subsequently, an erase operation was performed in the positive bias voltage range by increasing the bias voltage steadily starting from 0 V until an erase voltage of 10 V was reached. Because of the extended NDR, a relative high erase voltage of 10 V was necessary in order to switch the memory device into the HRS. The local maximum and minimum could be observed at 4 V and 8.5 V, respectively. As a result, the NDR region ranged over 4.5 V, which is about 50% longer than compared to the NDR range in the negative bias voltage range.

After the memory element was erased at a bias voltage of 10 V, a further voltage sweep was performed in the positive bias voltage range. The revealed device state exhibit a read current of 2.2×10^{-9} A. Therefore, it was comparable to the HRS which was

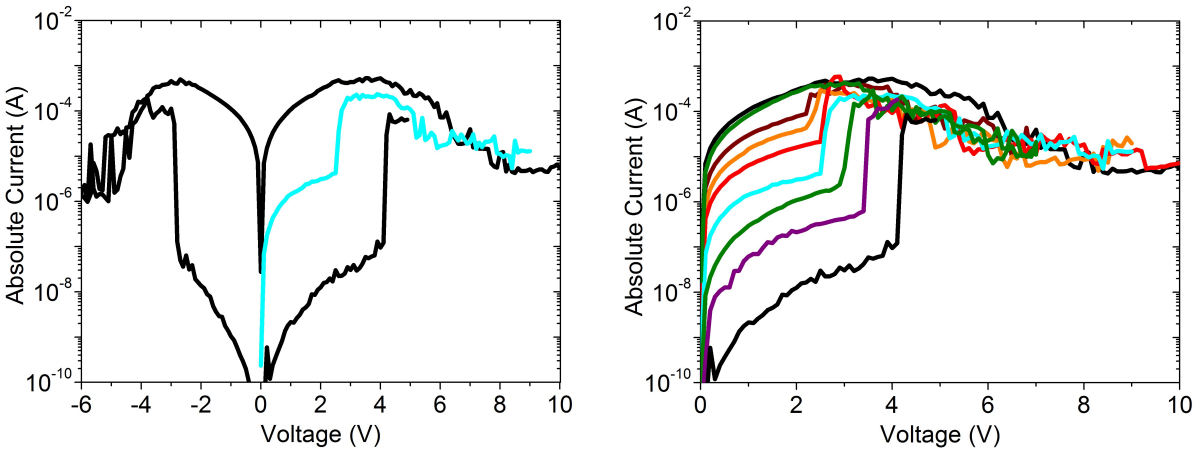
programmed previously by applying an erase voltage of $-6\,\mathrm{V}$. Besides the difference in the erase voltage also the threshold voltage was affected. Here, the resistance switching took place at a threshold voltage of $4.1\,\mathrm{V}$, which is significantly higher than compared to previously measured $2.8\,\mathrm{V}$ in the negative bias voltage range.

A HRS was initially programmed by erasing the device at $-6\,\mathrm{V}$. In this process, the local minimum of the device characteristic appeared at $-5.5\,\mathrm{V}$. Due to the asymmetric device characteristics and the accompanying extended NDR, an applied bias voltage of $5.5\,\mathrm{V}$ programmed an IMS. The state defining read current of this IMS was $1.5 \times 10^{-6}\,\mathrm{A}$ at $-1\,\mathrm{V}$ and, therefore, was by a factor of about 700 higher than compared to the HRS read current in the negative bias voltage range (see the black and cyan curves in Figure 39a). Sweeping up the bias voltage revealed the complete IMS until resistance switching occurred at a threshold of $2.5\,\mathrm{V}$. The illustrated device characteristics were denoted as asymmetrical due to the fact that the corresponding NDR ranges were extended differently. Furthermore the programmed device state depended on the bias voltage amplitude as well as on the bias voltage polarity what could be an indication of memristor like behavior.

In order to investigate the relationship between the programmed device state and the threshold voltages, the device was programmed with different bias voltages that correspond to the NDR range. The measured I/V curves are illustrated in Figure 39b. The previously obtained finding that read currents decreased with increasing programming voltage was confirmed here again. Furthermore, also an increase of the threshold voltage with increasing program voltage could be obtained. This was not clearly evident for devices without extended NDR introduced in Section 5.2.1 (see Figure 30).

The observed increase of the threshold voltage with increasing programming voltage could be explained by extended filaments, which are also supposed to be responsible for the extended NDR. Due to the fact that a higher bias voltage was required in order to erase the state of the device, more power was dissipated. As a result, more damaged was caused to the filament which therefore required more time or higher bias voltages for the reformation process. Besides the formation and rupturing of filaments, additional processes which depend on the bias voltage polarity such as electromigration must be considered in order to explain the observed asymmetric I/V characteristics.

In case the memory element exhibited an asymmetric device characteristic, then performed programming operations with equal bias voltage amplitudes but inverted polarities programmed different device states. These states were investigated in both bias voltage ranges afterwards.



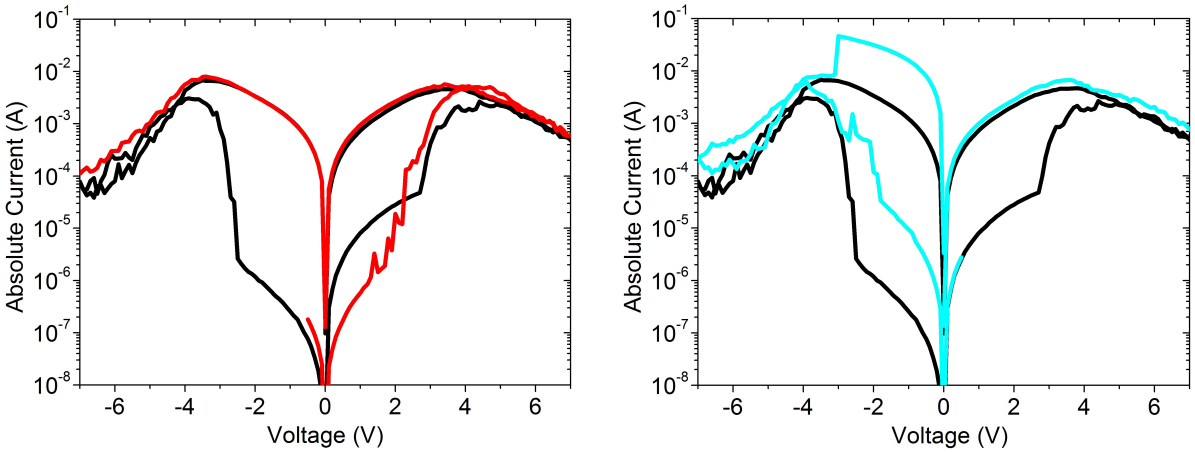
(a) Asym. device characterisitc *(b) IMSs*

Figure 39: *Different states of an ITO/Alq3/Ag memory device with asymmetrical hysteresis loops were addressed. I/V sweeps for state determination were always performed in the same bias voltage range as the corresponding programming operation. The applied program voltages were -6 (black), 3.6 (wine), 4.1 (orange), 4.9 (green), 5.5 (cyan), 7 (olive), 9 (purple), and 10 V (black). The color of the programmed state is indicated in brackets. Identical I/V curves are colored equally.*

After six switching cycles were performed in each bias voltage range, a distinct asymmetric device characteristic was established (see black curves in Figure 40). A single switching process consisted of an erase operation followed by a double sweep. The erase voltage was adjusted to $\pm 7\,\mathrm{V}$ and set the device into states, which correspond to a read current of $2.6 \times 10^{-7}\,\mathrm{A}$ and $8.1 \times 10^{-6}\,\mathrm{A}$ in the negative and positive bias voltage range, respectively. The asymmetric behavior was reproducible and not a result of variations in device performance. Hence, the state defining read currents depended on the bias voltage polarity and differed by a factor of thirty. These findings arose the question whether a state programmed by bias voltages of $\pm 7\,\mathrm{V}$ is symmetrical to the origin at low bias voltages or not.

First, a programming operation was performed in the negative bias voltage range in order to set the device into a HRS, which was confirmed by probing the device state. For this purpose, the bias voltage was swept from $0\,\mathrm{V}$ to $-0.5\,\mathrm{V}$ (see Figure 40b). The measured current was in comparison to the black reference curves increased by a factor of two higher. This minor deviation could be related to the shift of the local minimum from $-6.6\,\mathrm{V}$ to bias voltage lower than $-7\,\mathrm{V}$. Afterwards, a double sweep was performed in the positive bias voltage range. As a result, an identical state of the device was revealed. Switching into the LRS occurred steplike in the voltage range from $1.7\,\mathrm{V}$ to about $4\,\mathrm{V}$.

The NDR range and LRS were congruent with the reference curves. The same procedure was repeated with an inverted bias voltage polarity (see Figure 40a). The programmed device state was again symmetric to the origin at low bias voltages. The transition into the LRS occurred again steplike. Afterwards, NDR could be observed. However, after the local maximum was reached during sweeping the bias voltage towards 0 V, an abrupt current increase could be observed. This, in combination with a constant device resistance of 64 Ω, indicated that the device was short circuited.



(a) *Polarity flipped from - to +*

(b) *Polarity flipped from + to -*

Figure 40: *Investigation of states of asymmetric device characteristics. Reference curves (black) were measured after erasing the state of the device at ±7 V. Red/cyan curves indicate an erasing operation followed by an probing operation in the negative/positive bias voltage range. Subsequently, the bias voltage polarity was flipped and a double sweep was performed in the positive/negative bias voltage range.*

The conducted measurements showed that an asymmetric device characteristic is indeed a property of organic memory elements and did not originate from random variations in device performance which cause on average a steady shift of the device characteristic toward higher currents as elaborated in the previous chapters. Programmed device states were symmetric to the origin at low bias voltages and independent of the erase voltage polarity. What kind of state was programmed depended on the specific property of the respective NDR range. An erase operation performed at −7 V set the device into the HRS which was again symmetric to the origin of the I/V plane. However, the corresponding device state exhibited a higher resistance than compared to the device state programmed at 7 V. Therefore, the extended NDR could not be attributed to an improved charge injection, which contributed additionally to the measured current, due to modifications at the metal organic interface. As a consequence, the asymmetric device

characteristic must be considered as a key feature of the underlying physical mechanism responsible for reversible resistance switching in unipolar organic memory devices. Due to its dependency on the charge flow, a memristor model is suggested to be necessary for a detailed description of the device behavior.

5.3.5 Conclusion

Characteristic parameters such as HRS and LRS read currents of memory elements must be constant over a large number of switching cycles (endurance) with regard to potential memory applications. However, it was shown that properties of memory elements could be influenced by the measurement routine. The threshold voltage could be reduced by 20 % due to applying bias voltages for an according longer period. Furthermore, an evolution of the device characteristic took place what resulted in a significant change of characteristic parameters but opens up the opportunity to gain a progressive insight into the underlying physical mechanisms responsible for unipolar and reversible resistance switching.

The steady increase of characteristic currents could be related to stress due to repeatedly switching which in case of voltage sweeps was much higher than compared to switching by voltage pulses. Particularly disadvantageous was the fact that the LRS read currents increased slower than in comparison to HRS read currents. This resulted in a decreased on/off ratio at higher cycle numbers. Besides the shift towards higher currents, characteristic bias voltages were shifted towards the erase voltage of the corresponding bias voltage range. This shift was in case of V_{min} asymmetric and proceeded faster if a positive bias voltage was applied to the BE, hence, during operating the device in forward direction where electrons were injected over the TE into the memory device. This suggest that in case of filamentary conduction, electromigration due to momentum transfer from moving electrons to metal atoms of the filament may play a crucial role in case of asymmetric device characteristics. As a consequence, memristor like behavior must be considered as a relevant part of a complete description of organic memory elements.

The presented findings also illustrated that incorporated Al NPs are not necessary for reversible resistance switching, therefore simpler device structures could be used to model memory elements. The performed measurements showed that asymmetric device characteristics are indeed a property of organic memory elements and support mechanisms based on rupturing and reformation of filaments which extend with increasing number of switching cycles. A larger diameter of the filament also requires a higher cur-

rent for the rupturing process. This could be responsible for the observed enlargement of the NDR region because the local minimum was shifted to higher bias voltages. In this process, also an increase of the threshold voltage with increasing program voltage could be obtained, which was not clearly evident for devices without extended NDR.

Programmed device states were even in case of asymmetric device characteristics symmetric to the origin at low bias voltages and independent of the erase voltage polarity. Therefore, variations in charge carrier injection due to changed bias voltage polarities could be excluded as a main mechanism for the observed asymmetric behavior.

5.4 Influence of High Electric Fields

5.4.1 Memory Element Initialization

Fabricated memory elements do not always exhibit bistable and reversible resistance switching from the beginning. Instead, they show device characteristics that correspond to the existing device structure, e.g. an organic light emitting diode (OLED). Therefore, in a step called initialization, such devices must be forced to develop reversible resistance switching. Two different approaches are possible for this process. First, initialization can be carried out by current voltage sweeps where the bias voltage is swept steadily from 0 V to relatively high bias voltages that correspond to the erase region. Alternatively, relatively high and constant bias voltages can be applied similar to sub threshold switching until a state transition is observed. These procedures are also called burn-in [57].

Device initialization by voltage sweeps is introduced first, using an ITO/PEDOT:PSS/Alq3/Al NPs/Alq3/Ag device structure. The 60 nm thick PEDOT:PSS layer was applied by spin coating. Other layers were assembled similarly to devices introduced in Chapter 5.2. Both Alq3 layers were 30 nm thick and separated by a layer of aluminum core shell nanoparticles.

In the beginning of the initialization process, a positive bias voltage was applied and voltage sweeps were performed starting at 0 V. During the first 25 sweeps the erase voltage was increased from 10 V to 16 V. However, there were no indications of resistance switching. Emission of green light was observed at bias voltages higher than 7 V due to the fact that the additional PEDOT:PSS layer improved the injection of holes, which form excitons in the Alq3 layer and recombine luminously (see dashed green curve in Figure 41b).

A further increase of the erase voltage was necessary in order to initialize the memory element. Therefore, the erase voltage was increased further to 18 V and three additional bias voltage sweeps were performed. The first one revealed an OLED device characteristic behavior within the bias voltage range from 0 V to 18 V (black curve in Figure 41). Again, emission of green light was observed. The next one (red curve) showed an I/V characteristic exhibiting a significantly higher current in the bias voltage range from 2 V to 10 V than in comparison to the previous voltage sweep. Furthermore, current fluctuations appeared around 6 V. The third I/V measurement showed a curve that was similar to the second one, but the voltage sweep was terminated at the end of the region of appearing current fluctuations at 7.5 V, which could be considered as first indications

of an establishing resistance switching behavior (orange curves). Indeed, during the next bias voltage sweep a state transition was observed, which was indicated by an abrupt current increase from 7.3×10^{-7} A to 1.3×10^{-5} A at a threshold voltage of 2.8 V (see green curve in Figure 41a).

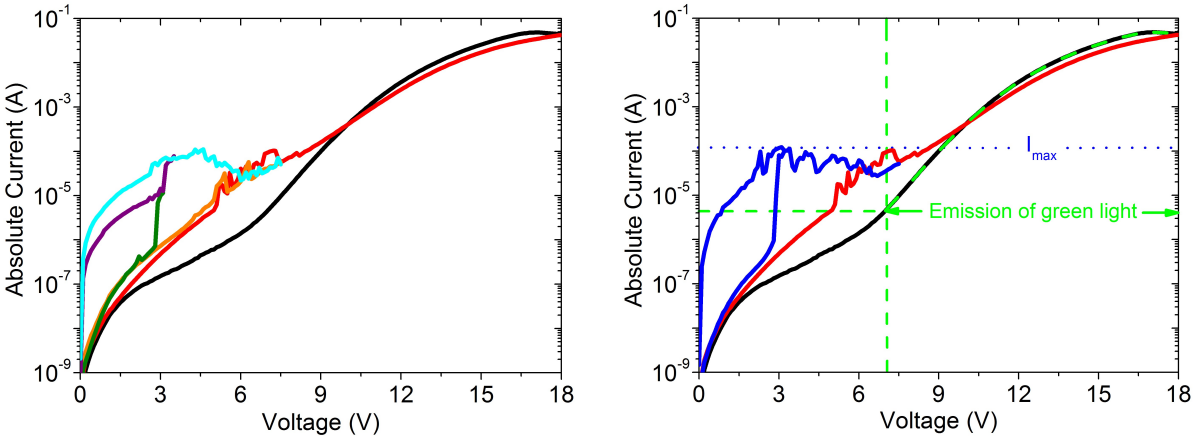
The state transition was confirmed by the next bias voltage sweep, which however revealed an IMS and finally switched the device into the LRS (purple curve). Sweeping the bias voltage from 0 V to 7.5 V revealed the LRS as well as the NDR region ranging from 4.3 V to 6.0 V and set the device into the HRS (cyan curve). Subsequently, a complete switching cycle was performed by stopping the next voltage sweep at the presumed local maximum at 3.2 V after an abrupt current increase at a threshold voltage of 2.8 V was observed. The performance of an additional voltage sweep in the range from 0 V to 7.5 V completed the switching cycle. State defining read currents of 2.7×10^{-8} A and 6.0×10^{-6} A for the HRS and LRS, respectively, resulted in an on/off ratio of 200 at 1 V. The local maximum appeared at 3 V with a corresponding I_{max} of 1.2×10^{-4} A.

Comparing I_{max} with the corresponding current of the initial OLED device characteristic (black curve) at 3 V, then the current increased by a factor of 800 due to device initialization and state transition from HRS into LRS can be observed. Furthermore, currents equal to or higher than I_{max} could only be observed initially at bias voltage higher than 9.2 V while emission of green light took place (see Figure 41b).

It is important to stress that most part of the later obtained current voltage characteristics exhibited higher currents in the bistable region than compared to the initial OLED I/V characteristic at 7 V, at which electroluminescence took place. However, no emission of light could be observed at bias voltages that corresponded to the established bistable region and NDR range (compare with Figure 41b). Similar results were reported by Wang et al. in 2009 who concluded that the absence of electroluminescence in combination with high currents through devices in LRS might be due to some localized conducting micro-channel [63] such as filaments or high conductive pathways instead of a current distributing over the entire device area.

Based on the proposed switching mechanism of filament formation due to migration of metal atoms towards regions of higher electric field strength [52], irregularities at the metal organic interface were needed. High stress due to high electric fields may enhance their formation at the metal-organic interface as well as following filament formation. The investigated device showed, as all other already presented types of memory elements, unipolar device characteristics in the positive and negative bias voltage range.

The following example dealt with memory device initialization by applying a constant

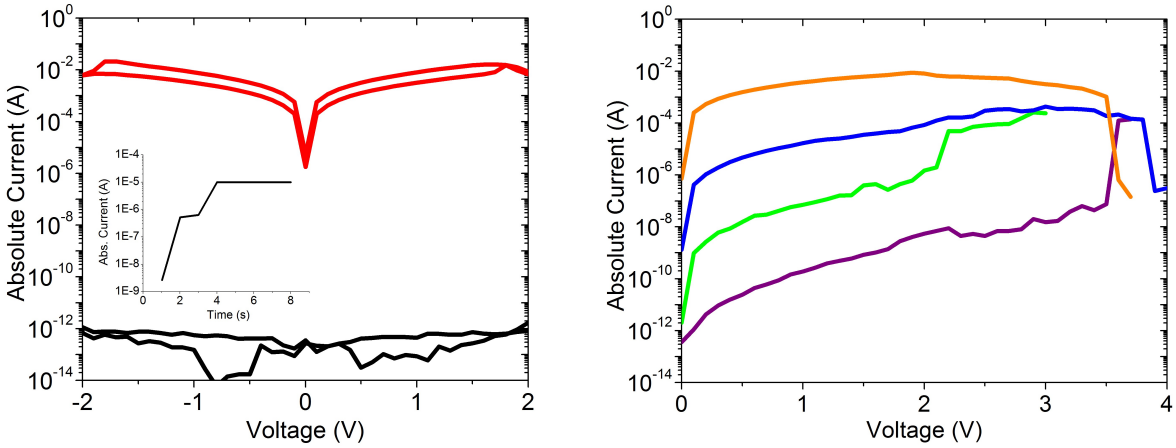


(a) Initialization *(b) Switching and light emission*

Figure 41: *Device initialization process of an ITO/PEDOT:PSS/Alq3/Al NPs/Alq3/Ag memory device. a) OLED device characteristics during run in forward direction (black). First indications of device initialization (red and orange) and state transition into IMS (olive) and LRS (purple). LRS and NDR are colored cyan. b) Complete switching cycle (blue) with OLED device characteristics (black) and I/V curve indicating device initialization (red) from Figure 41a. Emission of green light was observed in the range of the dashed green curve.*

high bias voltage. In this case, a glass/Ag/PMMA/Ag device structure was investigated, whereby contact electrodes as well as the PMMA (Polymethylmethacrylat) layer were fabricated by a wetchemical printing process as described in [65]. The investigated device was fabricated and kindly provided by Markus Postl. The PMMA layer was roughly 600 nm to 800 nm thick. Initially, the device state of the newly fabricated device was determined by sweeping the bias voltage from 2 V to −2 V and back again to 2 V (see Figure 42a). The corresponding current was in the range of 10^{-13} A and was equal to the leakage current. Hence, no significant current across the device could be determined. A constant bias voltage of 15 V was applied in order to initialize the device. For this purpose, the current compliance level was set to 10^{-5} A due to the fact that the applied bias voltage was in the range of the expected break down voltage [66] and the current should be limited to the expected current range of the LRS in case of a break down. The current increased sharply starting from 3×10^{-9} A and reached the set compliance level after 4 s (see inset in Figure 42a). Afterwards, a bias voltage sweep was performed alike to the initial one. Due to the burn-in the state defining read current was increased by at least ten orders of magnitude and reached 3×10^{-3} A at a read voltage of 1 V (see Figure 42a). The corresponding device resistance was given by Ohm's law and results in about 300 Ω. Interestingly, the read current was by a factor of about 400 higher

than the initially set current compliance value of 10^{-5} A. A possible explanation for this result is that a break down occurred indeed and a short circuit was formed. However, the set current compliance limited the current and prevented the device from severe damage. Performing a voltage sweep from 0 V to 3.7 V set the memory element into a HRS (see orange curve in Figure 42b). Afterwards, reversible resistance switching could be observed. However, the device showed a poor performance, because the transition from LRS into HRS takes place suddenly, in the same manner like switching from HRS into LRS. Furthermore, stopping the voltage sweep at the presumed local maximum at 3.7 V set the device in a significantly lower IMS than compared to the LRS (see Figure 42b).



(a) *Initialization by burn-in* ***(b)*** *Switching*

Figure 42: *Device initialization process of a printed glass/Ag/PMMA/Ag memory device. a) Device state before (black) and after (red) initialization by applying a bias voltage of* 15 V*. The corresponding current with respect to time is illustrated in the inset. b) Bistable region of the initialized device with HRS (purple), IMS (green) and LRS (blue). The orange curve shows the removal of the short circuit.*

The on/off ratio correspond to five orders of magnitude. It is important to emphasize that the state, which was set by the burn-in, was about two orders of magnitude higher than the final LRS. This behavior supports the idea of filamentary conduction. Applying bias voltages which are in the order of the breakdown voltage cause usually serious damage to the device and leads to the formation of a short circuits. Due to the current compliance the damage to the device was limited and the established localized short circuit was removed after sweeping the bias voltage beyond 3.5 V. A possible explanation for this process is Joule heating, which removed the short circuit and is also suggested to be responsible for the appearance of a NDR [59]. The remaining parts of the short

circuit acted as filament and were considered to be responsible for the observed reversible resistance switching.

5.4.2 Super Off State

The previous discussion was based on the assumption that bias voltages, which correspond to the erase region, set the device into the HRS. Motivated by the findings of sub threshold switching and an asymmetric evolution of the hysteresis loop, the influence of high erase voltage amplitudes was investigated in the positive and negative bias voltage range. For this experiment an ITO/Alq3/Ag device structure was used, which was temperature treated at 100 °C under vacuum conditions ($p = 10^{-3}$ mbar) for 30 min right after fabrication. The Alq3 layer as well as the Ag electrode were 300 nm thick.

In order to investigate the influence of high bias voltage amplitudes the measurement cycle described below was performed first in the negative bias voltage range and was immediately afterwards repeated in the positive bias voltage range. Due to the fact that there was no difference in the two performed measurement cycles with exception of the bias voltage polarity, the instructions of the measurement routine is limited to the positive bias voltage range for practical reason. The corresponding I/V curves are illustrated in Figure 43. Bistable behavior was already observed and the device was initially set into the LRS by sweeping the bias voltage from the erase region towards 0 V.

1. The LRS of the device is erased by increasing the bias voltage steadily starting at 0 V until the erase voltage of 7 V was reached. Additionally, a double sweep was performed by sweeping the bias from 0 V to 7 V and back to 0 V in order to obtain a complete reference curve for comparison (black curve).

2. A relatively high erase voltage of 12 V was applied to the device by increasing the bias voltage steadily starting at 0 V (red curve).

3. A double sweep was performed in the range from 0 V to 12 V in order to reveal the influence of high bias voltages on the device characteristics (green curve).

4. Point one was repeated for comparison (blue curve).

Several important findings were obtained from the recorded I/V characteristics: First, applying high bias voltages did not influence the shape of the reference curves measured during executing point one and four of each measurement cycle. All of them were

recorded after erasing the state of the device with a bias voltage amplitude of 7 V in the corresponding bias voltage range. State transitions from HRS into LRS appeared at threshold voltages of ±2.7 V for the initial and at −2.7 V and 2.8 V in case of the final reference curve. Local maxima appeared around the threshold voltages and the corresponding currents are in the mA range. Missing local minima in the positive bias voltage range from 0 V to 7 V suggest that an evolution of the device characteristics already took place. However, only a slight difference in HRS read currents could be determined, which were around 8.5×10^{-8} A and 3.5×10^{-7} A in the negative and positive bias voltage range, respectively. LRS read currents around 1 mA result in on/off ratios of 2×10^4 and 3×10^3 at ±1 V.

Erasing the state of the device by sweeping the bias voltage from 0 V to 12 V (red curve) significantly influenced the shape of the I/V curve measured immediately afterwards. The erased device exhibited a by about one order of magnitude reduced conductivity, compared to the particular HRSs (green curves). Measured read currents were 3.8×10^{-9} A and 2.6×10^{-8} A in the negative and positive bias voltage range, respectively. While the bias voltage amplitude was increased, the current increased steadily. Beside minor fluctuations, especially in the positive bias voltage range, no distinct increase in current, which characterizes a state transition of the device, was observed. The remaining parts of the I/V curve were comparable with already recorded reference curves.

The observations can again be explained by filamentary conduction which is supported by previously discussed findings. High erase voltages may damage the established filament(s) seriously and, as a consequence, the reformation takes longer than the period to sweep the bias voltage from V_{max} to V_{min}. Without intact filaments the main part of the current is not a result of localized effects. Instead the current is carried across the whole device area obeying the based conduction mechanisms of organic devices. It was shown previously that the average field strength plays an important role for the formation process and even a few variations can influence significantly the period required for switching from HRS into LRS. As a result of the double sweep, the bias voltage is swept steadily from ±12 V to 0 V instead of setting it instantaneously to 0 V like it was in the case of the previously performed erase operation. During the steady sweep towards 0 V, the bias voltage reached a region in which the device ability for resistance switching was restored and the reformation process could take place. After reaching V_{min}, the filament was already restored and a continuous transition from HRS into LRS by sweeping along the NDR range took place.

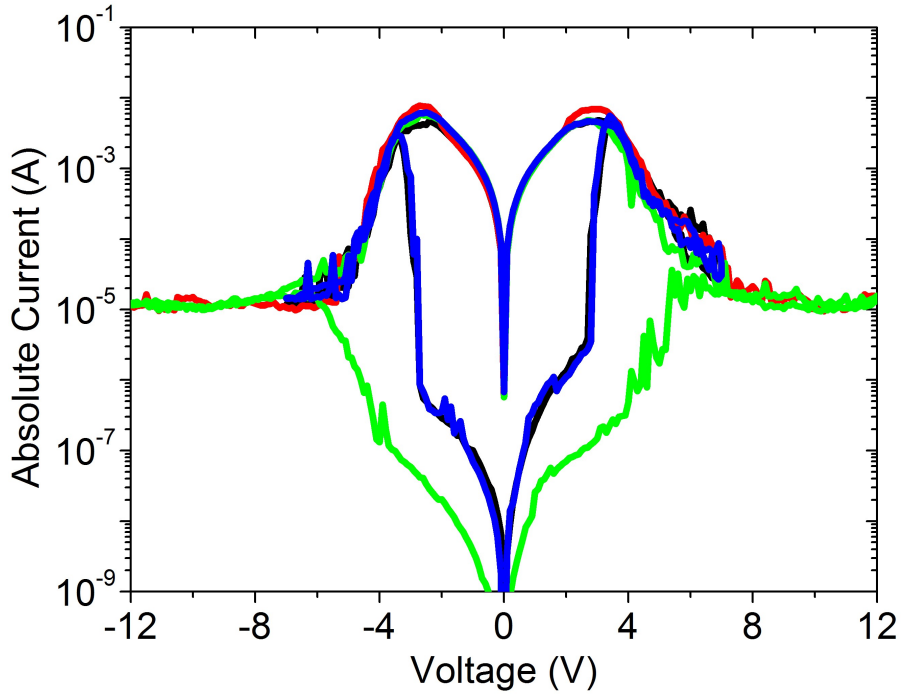


Figure 43: *Illustration of double sweeps measured during executing the previously described measurement routine. Black and blue colors indicate reference measurements before and respectively after the device was set in the Super Off State (green).*

Similar behavior was reported by Wang et al. [63] who suggested that conducting micro-channels are disabled by applying bias voltages in the range from V_{min} to $2 \times V_{min}$ and, as a result, they will not contribute to the switch on effect. However, applying bias voltages around V_{min} will enable them and resistance switching is observed again in the following. Similar behavior was also observed for ITO/Alq3/Ag/Alq3/Ag and ITO/Alq3/Al NPs/Alq3/Ag device structures.

5.4.3 Conclusion

The fabricated devices did not always show memory like behavior from the very first beginning. Instead, they showed I/V characteristics that correspond to the charge carrier transport abilities of their different layers as well as interface effects. However, such devices can be forced to develop non-volatile and reversible resistance switching by applying high bias voltages. Two different approaches were presented, namely:

a) Sweeping the bias voltage steadily from 0 V to relatively high bias voltages that correspond to the erase region. In this context, an OLED device structure was investigated, which developed the ability for reversible resistance switching after

sweeping the bias voltage from 0 V to 18 V. As a consequence, the next obtained I/V characteristic exhibit a significantly higher current in the bias voltage range from 2 V to 10 V, which correspond to the HRS of the device. Stopping the voltage sweep around the presumed local minimum allowed the device to perform a state transition from HRS into LRS during the next sweep due to the fact that too high erase voltages disable the switching ability of the device temporarily as shown in Chapter 5.4.2.

b) Applying a constant high bias voltage of 15 V to a glass/Ag/PMMA/Ag device structure lead to a state transition within a few seconds. In order to avoid irreversible short circuits, the current compliance level was set to 10^{-5} A. The set device state exhibited a relatively low read resistance of 300 Ω, which corresponding read current was substantially higher than the current compliance level set during device initialization. Increasing the bias voltage beyond 3.5 V set the device into a HRS. Following that a complete switching cycle was performed, which LRS is significantly lower than the initially set device state by burn-in. This example was a strong indication for filamentary conduction as underlying mechanism due to the fact that reversible resistance switching could be observed after a short circuit was established by applying high bias voltages.

On the contrary, too high bias voltages could temporarily disable the device ability to switch from HRS into the LRS. Here, the established filament suffered serious damage, which did not allow its reformation during a standard voltage sweep from 0 V to V_{min}. This assumption was supported by the fact that the device state set by an erase voltage of ±12 V exhibited a significantly lower conductivity than the HRS. This state is denoted as Super Off State. However, sweeping the bias voltage steadily from a relatively high V_E towards 0 V provided enough time for the filament reformation and allowed a continuous transition from HRS into LRS by sweeping along the NDR range. Reference curves measured before and after setting the device into the Super Off State showed that disabled switching behavior was only a temporarily and the Super Off state a reversible device state.

5.5 Influence of annealing

Temperature treatment was performed with a vacuum heating chamber right after finalizing the device fabrication. In this connection, this process is also denoted as preconditioning during which the substrate together with the memory elements was heated up to 100 °C under vacuum conditions ($p < 10^{-3}$ mbar) for 30 minutes.

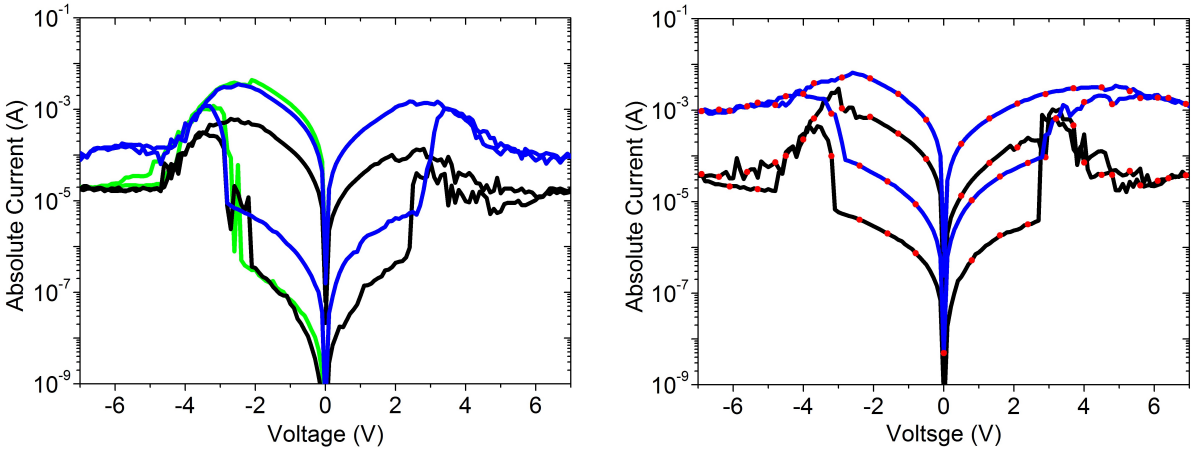
Two different variations of an ITO/Alq3/Ag device structure were investigated which exhibited a 150 nm and 300 nm thick Alq3 layer and are referred to as structure 1 and structure 2, respectively. Reference devices did not undergo a preconditioning, but were fabricated together with temperature treated devices. They were also characterized equally. Therefore, they exhibited identical device structures and the measured I/V curves are comparable.

Four sets of I/V measurements were performed consecutively for investigation. Each set consisted of three complete switching cycles where erase and write operations were performed alternately. First, the state of the memory element was erased by sweeping the bias voltage from 0 V to 7 V. Then, the device was switched into the LRS by a double sweep in the same bias voltage range. The bias voltage polarity was changed after each set of switching operations, whereby the first set was performed in the positive bias voltage range.

The first and the last performed double sweeps in the positive and negative bias voltage range were used for comparison of devices with a structure 1 and structure 2 configuration. Obtained device characteristics are illustrated in Figure 44 and 45 below.

The reference device with a structure 1 configuration showed an expected behavior. LRS and HRS read currents increased due to repeated resistance switching by about one order of magnitude. Threshold voltages of about −2.7 V and 2.5 V were not significantly affected due to the evolution of the device characteristics. A slight extension of the NDR can be observed in the positive bias voltage range in Figure 44a in which also an additional green curve (double sweep) is illustrated. This curve corresponds to the last set of switching operations performed in the negative bias voltage range and was measured immediately before the illustrated blue curve was obtained. It shows that the change in the erase region of the I/V curve takes place within one single switching cycle and the initially symmetric device characteristics actually evolved asymmetrically and finally again exhibited a symmetrical shape.

The temperature treated device showed comparable but more pronounced behavior. In order to compare the investigated devices, the focus was on the erase current at



(a) *Reference device* ***(b)*** *Preconditioned device*

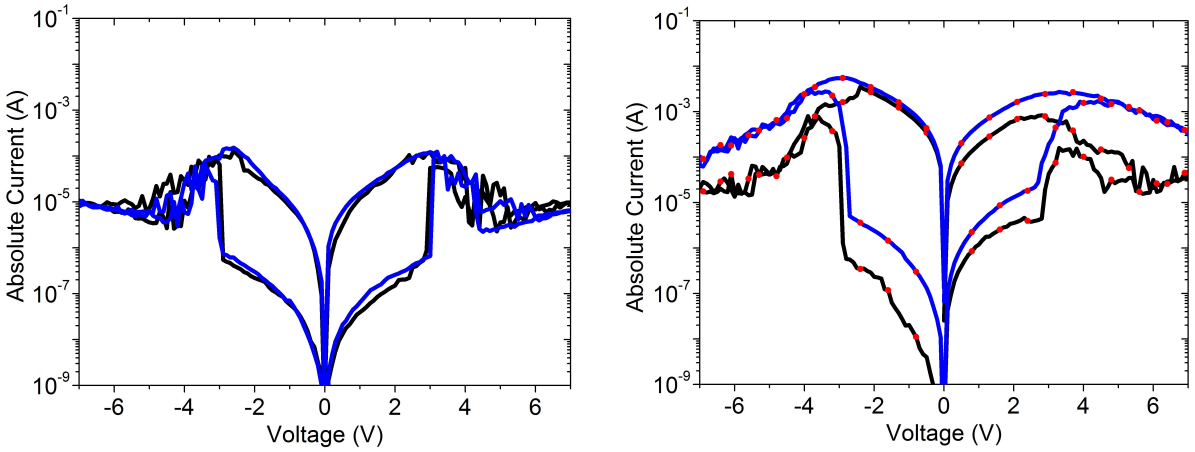
Figure 44: *Evolution of the I/V characteristics of (a) reference and (b) temperature treated structure 1 devices due to repeated switching. The first and the last measured double sweep in the corresponding bias voltage range is colored black and blue, respectively. Red dots indicate I/V curves of temperature treated devices. The green curve in Figure (a) was measured immediately before the blue one was obtained.*

$\pm 7\,\mathrm{V}$ first. The erase current is not influenced by the actual device state (LRS, IMS, HRS or Super Off) as long as local minima can be observed in the investigated bias voltage range what is the case considering the initially measured I/V curves. Erase currents of the temperature treated device were slightly increased in comparison to the reference device whose initially measured erase currents were about $2 \times 10^{-5}\,\mathrm{A}$. As a consequence, the current across the whole device area could be considered as equivalent, just as the device structure of both memory elements. Differences in the HRS read currents of about one order of magnitude were probably due to variations in the remaining parts of ruptured filaments which highly likely acted as a high conductive pathway and contribution correspondingly to the measured current. Furthermore, an accelerated evolution of the device characteristics could be observed, which could be reduced to temperature treatment. All read currents were increased by about one order of magnitude and again no influence on the threshold voltage could be observed. There were two characteristic features of the evolved device characteristics, namely:

The transition from HRS into LRS by sweeping the bias voltage from $0\,\mathrm{V}$ to V_{Erase} did not occur abruptly at a certain threshold voltage, but rather continuously by a number of small steps over voltage ranges from $-2.8\,\mathrm{V}$ to $-4.2\,\mathrm{V}$ and from $2.8\,\mathrm{V}$ to $4.5\,\mathrm{V}$. Furthermore, a substantial evolution of the NDR range took place, which resulted

in a current increase by more than one order of magnitude at the initially programmed erase voltage of ±7 V.

Similar behavior was observed for devices with a structure 2 configuration (see Figure 45) where the Alq3 layer thickness was doubled. In this case, no significant change of the reference device characteristics due to repeated resistance switching was observed. On the contrary, the temperature treated device showed an evolution of the device characteristics which was, however, less pronounced than compared to structure 1 devices. The slower evolution of the device characteristics could be related to the thicker Alq3 layer due to which material transport along the device requires more time and therefore more switching cycles.

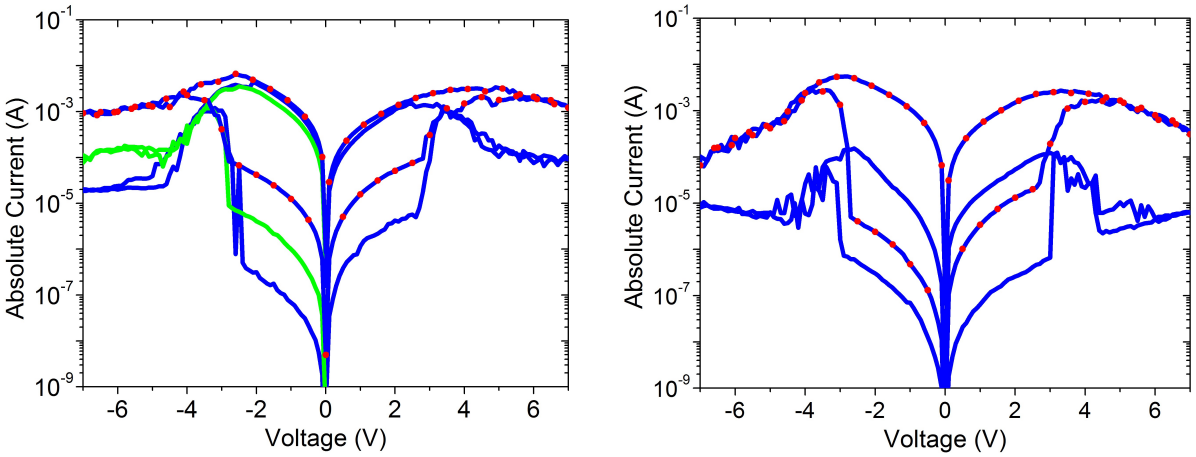


(a) *Reference device* ***(b)*** *Preconditioned device*

Figure 45: *Evolution of the I/V characteristics of reference and temperature treated structure 1 & 2 devices due to repeated switching. The first and last measured double sweep in the corresponding bias voltage range is colored black and blue, respectively. Red dots indicate I/V curves of temperature treated devices.*

Reference and temperature treated devices were compared with each other in Figure 46 in which each last double sweep in the positive and negative bias voltage range is illustrated. Preconditioning lead to an accelerated evolution of the device characteristics which resulted in an increase of the state defining read currents of states set by programming voltages of ±7 V. In this process, the NDR extended significantly until no local minimum could be observed and, following that, the programming current at ±7 V increased by at least one order of magnitude in comparison to reference devices. Asymmetric device characteristics were observed for both device structures. HRS read currents of preconditioned structure 2 devices differed by about one order of magnitude (see Figure 45b). Currents associated with local maxima were for all devices with ex-

ception of the structure 2 reference device around 5 mA. The deviation could again be explained by the thicker Alq3 layer due to which material transport along the filament required more time in order to provide enough material for extending the filament.



(a) Structure 1 *(b) Structure 2*

Figure 46: *Evolution of the I/V characteristic of a) reference and b) temperature treated structure 1 devices due to repeated switching. The first and last measured double sweep in the corresponding bias voltage range is colored black and blue, respectively. Red dots indicate I/V curves of temperature treated devices. The green curve in Figure 44a was measured immediately before the blue one.*

A possible explanation for this behavior is that due to temperature treatment more material of the top electrode diffused into the organic bulk. As a consequence, more material was provided for filament formation which lead to thicker filaments and/or to the formation of an additional one. Thicker filaments exhibited a lower electrical resistance and, therefore, carried a higher current. As a result, characteristic currents were increased and an evolution of the device characteristics took place, because the thicker filaments needed higher bias voltages to be ruptured.

5.5.1 Conclusion

Temperature treatment right after device fabrication influenced the I/V characteristics significantly and resulted in an accelerated evolution of the device characteristics. In this process, the NDR range started to extend and all characteristic currents in the same bias voltage range started to increase. Once the local minimum was shifted beyond the initially programmed erase voltage of ± 7 V, then V_E corresponded to the programming region of the device characteristics and erasing the device completely with the same

erase voltage was not possible any longer. The set HRS is therefore an IMS and the obtained on/off ratio had decreased (see Figure 46b). The accelerated change of I/V characteristics of temperature treated devices was supposed to originate from additional TE material which diffused into the organic bulk due to preconditioning and provided material for the extension of existing filaments and/or for the formation of additional ones.

5.6 Memory device comparison

This chapter deals with the comparison of the different hybrid organic/inorganic memory elements, which are based on the semiconducting Alq3 as separating material and which were already introduced in Chapter 5.2.1, 5.4.1, and 5.5. Beside variations in the Alq3 layer thickness of single layer devices with an Alq3 layer thickness of 150 nm and 300 nm, respectively, multilayer structures with incorporated aluminum core shell NPs as well as an additional PEDOT:PSS layer were used for comparison and are referred to as structure 1, structure 2, structure 3 and structure 4 in the following. Each Alq3 layer of memory devices, which exhibit a structure 3 and structure 4 configuration, is 30 nm thick. Al NPs were introduced by the deposition of a 15 nm thick aluminum intermediate layer. ITO and Ag were used as BE and TE electrode, respectively.

Devices with a structure 1 and structure 2 configuration were characterized by a double sweep in the bias voltage range from 0 V to ±7 V which was performed after the state of the device was erased at ±7 V. Structure 3 and structure 4 devices were switched by sweeping the bias voltage from 0 V to ±6.5 V. In order to switch the device into the LRS, the voltage sweep was stopped at the presumed local maximum. The results were without concerns comparable due to the fact that the local minimum could be observed during the erase operation. Switching by stopping the voltage sweep at the presumed local maximum leads to a LRS with lower conductance than compared to switching by a double sweep. However, the resulting deviation was comparable to the expected variation of the LRS read current, which can increase noticeably within a few switching cycles (see Chapter 5.5). Therefore, a detailed comparison of all four different device structures with respect to the LRS was not possible.

As shown in the previous chapters, characteristic properties (HRS, LRS, NDR range, V_{max}, V_{min}) and their corresponding currents vary significantly considering especially temperature treated devices. Therefore, a discussion of devices which underwent a preconditioning was excluded. As a consequence, the change of an evolving device characteristics could at least be reduced to a minimum and the influence of the device structure on the device characteristics can be elaborated and discussed.

The focus for device comparison was on the HRS and LRS read current at a bias voltage of ±1 V, the threshold voltage and the position of local maxima and minima, which define together the NDR range. Corresponding I/V curves and parameters are illustrated in Figure 47 and are listed in Table 4 for comparison, respectively. The only necessary condition for comparing different device structures was that the local

minimum of the corresponding voltage range could be observed while performing the erase operation and, consequently, the set device state did not correspond to a super off state. Hence, a state transition from HRS into LRS must be observed during the following I/V sweep. The super off state would be suitable in order to compare the currents across the whole device area of different device structures. However, damage to the organic semiconductor due to repeated switching and high bias voltages would decrease the corresponding current over time and was therefore considerable only with reservation. Furthermore, the focus was on the switching ability of the device and, therefore, the super off state was not of primarily interest.

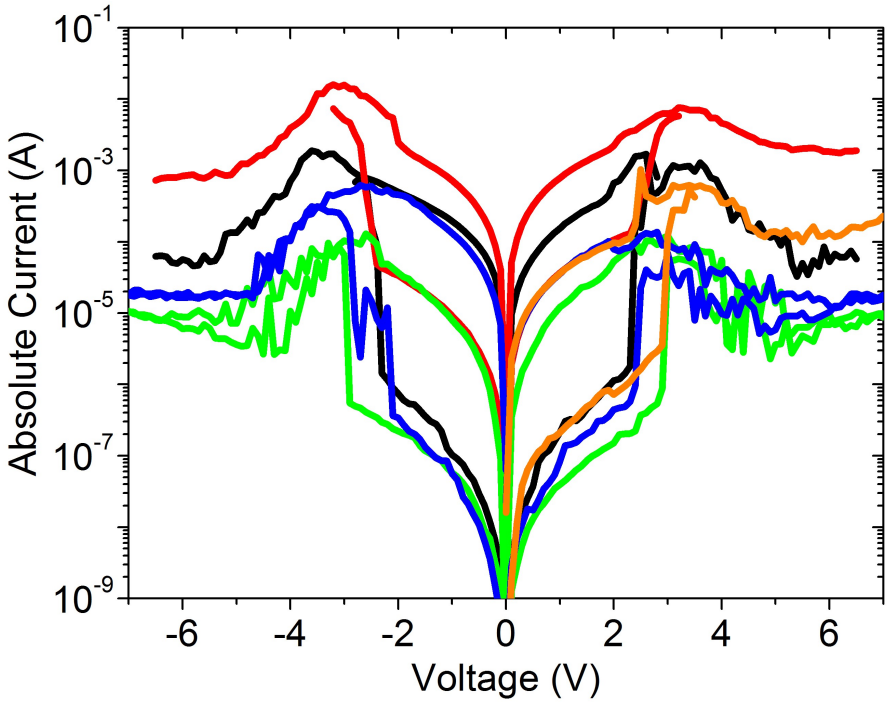


Figure 47: *I/V characteristics of devices with a structure 1, structure 2, structure 3 and structure 4 configuration are colored blue, green, red and black, respectively. Orange curves correspond also to a structure 3 device.*

The threshold voltage varied in the range from −3 V to −2.3 V and from 2.3 V to 3.0 V. However, no significant influence of the device structure could be obtained, although the overall Alq3 layer thickness differed by a factor of five, considering devices with a structure 2 and structure 3 configuration. A clear assignment of the NDR range was also not possible due to the fact that measured device characteristics exhibited either strong fluctuations or were relatively flat around the local minima. A rough estimate of the local maxima and minima resulted in NDR ranges which varied from 2 V to

Table 4: *Characteristic parameters of I/V curves illustrated in Figure 47. Absolute values of the HRS and LRS read currents as well as I_{max} of both bias voltage ranges are averaged arithmetically. Read operations are performed at $\pm 1\,\mathrm{V}$. If characteristic parameters are separated by a slash, than they correspond to the negative/positive bias voltage range and no average was calculated. The ratio of HRS and RLS is equal to the On/Off ratio. NDR range is calculated by the difference of V_{max} and V_{min}.*

Device structure	HRS [A]	LRS [A]	On/Off ratio [1]	V_T [V]	V_{max} [V]	I_{max} [A]	V_{min} [V]	NDR range [V]
ITO / Alq3 (150 nm) / Ag	7.0×10^{-8}	8.3×10^{-5}	1200	-2.8/2.4	-2.7/2.8	3.8×10^{-4}	-4.7/5.0	2.0/2.2
ITO / Alq3 (300 nm) / Ag	4.9×10^{-8}	1.0×10^{-5}	200	-3.0/3.0	-2.6/3.0	1.3×10^{-4}	-5.2/5.5	2.6/2.5
ITO / Alq3 / Al NPs / Alq3 / Ag	2.3×10^{-5}	7.6×10^{-4}	33	-2.4/2.4	-3.2/3.2	1.2×10^{-2}	-5.2/6.2	2.0/3.0
ITO / PEDOT:PSS / Alq3 / Al NPs / Alq3 / Ag	1.6×10^{-7}	1.8×10^{-4}	1100	-2.3/2.3	-3.6/2.6	1.8×10^{-3}	-5.8/5.4	2.2/2.8

3 V and must be considered as lower limit due to the fact that an evolution of the device characteristics can take place by repeated switching. Current fluctuations in the NDR range could be related to an established filament without stable rupturing region, because too few material is available within the organic bulk. The fluctuations disappeared with increasing number of switching operations while the LRS read current is started to increase (see Figure 44a in Chapter 5.5). This observation was in good agreement with proposed filament extension due to material transport from the TE and the resulting evolution of the I/V curves. Device characteristics which corresponded to a structure 3 configuration are colored red and orange respectively and exemplify how large variations can appear even considering one single device structure. In this case, the HRS of the one memory device corresponded to the LRS of the other structure 3 device configuration. Corresponding read current at 1 V belonged to 3.6×10^{-5} A. In combination with read currents of the upper LRS and lower HRS of 7.9×10^{-4} A and 2.1×10^{-7} A, respectively, the on/off ratios resulted in 20 and 170 at 1 V. Considering the orange curve instead of the red curve for device comparison, then the HRS and LRS read current varied in the range from 4.0×10^{-8} A to 2.1×10^{-7} A and from 1.2×10^{-5} A to 1.6×10^{-4} A. Hence, they were comparable and the device structure did not have a significant influence on the device characteristics. However, there was an influence on the evolution of the device characteristics, which was indeed affected by the device structure or, to be more general, by the overall layer thickness of the separation materials. This supports the filament thickening theory which relies on material transport from the TE due to repeatedly switching and preconditioning.

6 Summary and Conclusion

Emerging new technologies associated with Industry 4.0, Internet of Things and Smart Environments require memory technologies which can be fabricated cost effectively on virtually any substrate, are non-volatile and exhibit data retention comparable to archival systems. Especially in the low price segment, organic memory technologies have the potential to meet such high demands. However, a detailed understanding of the underlying mechanisms is essential for the device performance optimization. Within this thesis, the main focus was put on the investigation of the underlying physical mechanisms responsible for reversible and unipolar resistance switching of non-volatile and two-terminal hybrid organic/inorganic memory devices.

Memory elements with and without incorporated aluminum oxide shell NPs were used to study proposed switching mechanisms based on charge trapping and filament formation, respectively. For this purpose, device characterization was performed by I/V measurements due to which the state of the investigated device was switched repeatedly. In order to achieve an optimal comparability of measured I/V characteristics, switching by voltage sweeps was used which, however, was much more time-consuming compared to switching by voltage pulses. Programmed device states were verified by reading operations. Thereby, clearly distinguishable intermediate states were observed between the limiting LRS and HRS boundary states. It became apparent that incorporated aluminum oxide shell NPs are not necessary for the observation of uniplar and reversible resistance switching. Hence, they could be omitted and the memory device structure could be simplified.

Long term behavior is with regard to potential memory applications of significant importance. In order to investigate this issue, two different approaches were chosen and the obtained results were combined to an overall picture. About 1800 switching operations were performed and in this process a continuous increase of read, write and erase currents was observed whereby the HRS read and the erase current were more affected. As a consequence, write and erase currents equalized towards the end of the measurement series. HRS and LRS read currents showed equivalent behavior. Addi-

tionally, also single distinct current increases could be observed. Similar results were also obtained by switching by voltage sweeps. In this process, an extension of the NDR range was observed. Such behavior was also denoted as evolution, proceeded faster in the positive bias voltage range and resulted in an asymmetric device characteristic. As a consequence, writing operations performed at equal bias voltage amplitudes, but with inverted polarity, wrote clearly distinguishable device states. However, HRSs programmed in both erase voltage regions were equivalent. This behavior also explained the equalization of the characteristic currents due to the fact that the programming voltages were kept constant while an evolution of the device characteristic took place. Furthermore, it was observed that in case of an extended NDR the threshold voltage increased with increasing resistivity of the corresponding IMS. Such behavior could satisfactorily be explained by mechanisms based on filamentary conduction. We strongly believe that, I/V measurements cause material transport from the top electrode along the filament and enlarges its cross section. Consequently, the resistance is reduced and the device current increases correspondingly. Thicker filaments also require more power to be ruptured, what could be related to the extension of the NDR ranges. Single steplike current increases could also be explained under the assumption that either additional filament are formed or, more probably, the switching region is influenced by the material transport along the filament.

In order to verify this assumption, supplementary measurements were performed. For this purpose, memory elements were temperature treated (preconditioned) under vacuum at 100 °C for 30 min right after device fabrication. The intention was to trigger diffusion processes of top electrode material into the bulk. Subsequently, the device state was switched repeatedly by I/V sweeps which showed an accelerated and much more pronounced evolution of the device characteristics. It is highly likely that the additionally provided material let to an expansion of the filament and influenced the switching region as well.

State transitions from HRS into LRS were forced within the read region by applying the corresponding bias voltage for an adequate long period. The delay of the switching process increased disproportionally to the decrease of the applied sub threshold bias voltage amplitude and ranged from just a few seconds to a couple of minutes. Such writing processes were denoted as sub-threshold switching with which the threshold voltage could be reduced up 20 %. This observation was also in agreement with proposed switching mechanisms based on filament formation which relies on migration processes in inhomogeneous electric fields.

Furthermore, the influence of relatively high erase voltages on functioning memory elements was investigated. The erased device exhibited a higher resistance than compared to the HRS and no abrupt switching effect could be observed during performance of the first part of a double sweep. However, the switching ability was restored by sweeping the applied bias voltage along the NDR range back to 0 V. During this process, the device performed a continuous transition from HRS into LRS and afterwards showed a normal switching behavior again. This phenomenon could also be explained by filamentary conduction. Here, high erase voltages caused severe damage to the filament and the period required for sweeping the bias from 0 V to V_{min} was not sufficient long enough to reform the filament which, however, was achieved during ramping it down to 0 V.

Device initialization provided strong evidence for filamentary conduction. The application of relatively high bias voltages on device structures with an insulator as separating material caused a short circuit which could be removed afterwards by Joule heating. Subsequently, unipolar resistance switching was possible. Similar behavior could be observed with an OLED device structure. The device showed unipolar resistance switching after the application of high erase voltages of 18 V. Interestingly, no electroluminescence took place at bias voltages around V_{max} although the corresponding current was significantly higher than compared to bias voltages at which emission of green light was observed. This aspect is also an strong evidence for filamentary conduction and contradicts possible mechanism based on charge transport.

No distinct influence of the device structure on the device characteristics could be observed. However, the threshold voltage must be considered apart from minor variations as independent of the device structure. Therefore, we suggest that the primary focus of further investigations should be on the investigation of abrupt state transition at the threshold voltage. Especially, the asymmetric evolution of the device characteristics may offer a deeper insight into the underlying physical mechanisms. Due to its dependency on the bias voltage polarity, we assume that memristor like behavior as a result of electromigration must also be considered for a complete description of the investigate two-terminal, hybrid organic/inorganic memory devices.

Organic memory elements carry great potential due to cost effective high volume production by wetchemical fabrication processes. Furthermore, an over several orders of magnitude continuously tunable electrical resistance enables hardware based implementation of designed neuromorphic networks for e.g. smart sensor applications and non-volatile resistive photo-switches for flexible image detector arrays [67]. An easy realization of a crossbar memory array is possible by using diodes instead of transistors as selective elements. In this way, the problem of parasitic currents can also be encountered and, moreover, the highest possible integration density of $4\,F^2$ can be achieved.[65]

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