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Best Practice for Dynamic Analysis by Laser Stimulation

MASTER'S THESIS

to achieve the university degree of

Master of Science

Master's degree programme: Electrical Engineering

submitted to

Graz University of Technology

Supervisor

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Institute for Electronics - IFE

Graz, March 2015

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Thanks

My gratitude goes out to my parents Albert and Rita Promberger who supported me throughout my studies and were always excited about my academic progress. My sister, Karoline Promberger, who gave me the best advice I could ever get before starting my studies: When I was uncertain about beginning my studies in the first place, she just told me that I am responsible for my own and I should take a shot at it if I wanted to. Prof. Dipl.-Ing. Dr.techn. Peter Söser from the department of electronics at the TU Graz for his valuable inputs during our conversations and giving me instructions and tips regarding the contents of this thesis. From the company ams AG Albert Scheucher who was my supervisor and offered me to write my thesis about the subject of DALS and was always interested and of great guidance while working on this topic. Klaus-Peter Tschernay for sponsoring my thesis out of his department. Gerhard Losinschek, Franz Renz, Patrick Dionis, Christian Mautner and Ewald Lamprecht for their fruitful discussions and inputs during the follow up meetings and every time we had a conversation regarding my topic. Anderson Singulani for his useful suggestions regarding the FEM based simulations. Thomas Haber for the FIB preparations of my experiment samples. Paolo Grassi from Sector Technologies who provided useful details regarding the tester equipment and Michael Fels from Hamamatsu Photonics Germany for answering my questions regarding the laser scanning microscope. Not to mention all my friends and study colleagues for their interest in my work and late night talks.

Abstract

Defect localization in integrated circuits is a very important task in failure analysis. There exist multiple ways of how defects can alternate a device's behavior and there are manifold locations in an integrated circuit where defects can be physically located. Failure localization itself should ideally lead to the exact location of the original defect within a very short time and at high precision. Furthermore defective parts are very valuable as they also can be used to identify possible weaknesses of a device and must not be damaged during the analysis. The DALS technique makes use of the most available analysis tools in a failure analysis laboratory and combines the above mentioned desires into one analysis routine. The thesis will cover an experimental approach about the possible influence of a continuous wave laser at $\lambda = 1300\,nm$ and limited power of $P = 100\,mW$ on the operation of mixed signal devices and simple test structures. In correlation with simulation and analysis results a best use approach will be suggested to reduce the overall analysis time and to increase the meaningfulness of the analysis itself. DALS will be used to detect soft defects in integrated circuits which cover timing failures, leakage currents, shifted device parameters and varying resistances in contacts, vias or signal lines. Furthermore the results and findings of this work will be compared with the related work from other researchers.

Abstrakt

Die Fehlerlokalisation in integrierten Schaltungen ist ein Hauptbestandteil der Fehleranalyse und trägt bei jedem Halbleiterhersteller dazu bei das *Null-Fehler-Geschäftsmodell* zu ermöglichen. Zu den unzählbar möglichen Defektstellen aus der Produktion, dem Design oder dem Layout eines Bauteils, existieren mehrere Möglichkeiten wie das gewünschte Betriebsverhalten negativ beeinflusst werden kann. Mit Hilfe geeigneter Analysetechniken zur Fehlerlokalisation, soll der Defekt binnen kürzester Zeit örtlich am Bauteil identifiziert werden. Die dabei verwendete Analysetechnik selbst soll das Bauteil möglichst nicht beschädigen, da dieses in vielerlei Hinsicht von großem Wert für die Aufklärung eines einzelnen Vorfalls, oder der Identifikation eines generellen Bauteil-Problems ist. Die DALS Analyse-Technik erfüllt genau die genannten Anforderungen, wobei ausschließlich Standardgeräte aus einem Fehleranalyselabor verwendet werden. In der folgenden Darstellung wird daher in aufeinander aufbauenden Experimenten der Einfluss eines Laserrastermikroskops für eine Wellenlänge von $\lambda = 1300\,nm$ und einer begrenzten Leistung von $P = 100\,mW$ auf den Betrieb eines Mixed-Signal-IC's untersucht. DALS selbst wird in integrierten Schaltungen dazu verwendet so-genannte *Soft-Defects* zu identifizieren worunter fehlerhafte Leckströme, Zeitsignale, Bauteil-Parameter und über Temperatur veränderbare Widerstände in Vias oder Kontaktierungen und Leitungen zusammengefasst werden. Die Ergebnisse der Experimente werden anschließend anhand von Simulationen beziehungsweise durch den Vergleich mit weiterführender Literatur diskutiert und zu einer Best-Practice Analyse zusammengefasst, welche es dem Anwender oder der Anwenderin ermöglichen soll die bestmöglichen Resultate in kürzester Zeit mit DALS zu erreichen.

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1 Introduction

Characterization and localization of defects from an integrated circuit can be a highly challenging task while a simple pass-fail evaluation of a device might be quite easy. In order to decrease the failure analysis time while increasing the failure detection rate we have been working out a failure analysis method by the use of a beam based failure analysis technique. Under certain circumstances it is possible to create a pass-to-fail or fail-to-pass behavior due to the local and also in size limited stimulation of a laser beam. During our analysis we increase the amount of information about a possible defect in comparison to other known analysis methods. At the same time we are reappraising the basic principles of laser influenced defect localization with a main focus on the absorption and transmission of laser light, thermal activation as well as photo current generation. With this knowledge we will clarify which failures might be detectable by the use of our proposed setup as well as presenting our best use setup parameters. During this whole process we will even be able to improve our experience with the use of other available failure analysis techniques for effectiveness and usefulness comparison purpose.

We will prove that active beam based failure techniques such as **Best Practice for Dynamic Analysis by Laser Stimulation** are helpful to recover multiple failure types during one evaluation run due to the combination of functional testing in the analog and digital regime of the integrated circuit as well as high accuracy current, voltage and timing delay measurements. Together with all the possible production faults like opens, shorts, resistive bridges or floating nodes, we will be able to pinpoint possible design or layout weaknesses due to the high accuracy observation of timing variations and laser influenced resistance changes. With the local excitation of the laser we will even be able to limit the possible failure area on the IC which will lead to a much faster failure correlation in the schematics of the observed integrated circuit. The temperature dependency of some defects which should mainly cause the pass-to-fail or fail-to-pass behavior, is furthermore

investigated. It is checked if thermal material expansion might be useful in the description of fault behavior and a detailed overview of the expected resistance change and temperature influence of the laser is given. We will also check if the supposed defects can be artificially generated and will analyze how frequently those defects are monitored during production and occur in field return samples.

Our analysis will summarize the do's and dont's for beam based laser analysis techniques. In the best case the analysis will show a clear defect spot caused by the influence of the laser on the IC if our proposed setup will be used. We will show the most useful setup parameters for all the used measurement components in our examples and confirm our observation during multiple experiments and simulations. Within our experiments we will show the device specific behavior depending on:

- Test Setup
- Supply Voltage/Current
- Test Pattern Type/Speed
- Temperature
- Laser Scan Area
- Laser Scan Direction
- Laser Power
- Magnification Lenses
- Scan and Laser Synchronization

The worst case results will be useful to reveal where the proposed analysis method is not useful. They will also cover what might have gone wrong during our experiments. These clear descriptions will lead to an easy to use test setup which is created to be used for a very simple but powerful failure detection and evaluation. The easy to use guide is also designed to create interest in the use of beam based defect detection systems and it will be not limited to just work with our specific test equipment.

All our results will be achieved by tests with simple test structures and suitable test devices which will reflect the appearing defects in the day to day business of semiconductor production. All these used devices will show some kind of temperature related behavior whether they where caused due to a failure in the production, a poor design or layout, or due to artificial failure implantation. The literature research will present the findings from related work and this information will be used to further improve and

validate our analysis technique. Additionally we got in correspondence with the setups manufacturers to fully understand all the used components of the measurement setup and to minimize measurement failures. The experimental results will also be correlated with simplified and suitable simulations, created with finite element simulation tools, to evaluate the correctness and validity of our findings. All our experiments will be created to match defects which will be observable in the day to day work and won't show any abstract behavior.

In the first chapter we will give a short theoretical background with some recommended literature of the basic working principles. Furthermore we will enlighten the most common defect types in an integrated circuit. Then we will carry on by introducing already known active and passive beam based defect localization methods. Afterwards we will take a look at non beam based defect localization techniques and show how the combination of the presented methods might be helpful for detecting IC failures. We will also introduce the basic principles of functional test pattern generation for dynamic analysis and clarify which method might be useful under certain circumstances. In the section experiments we will describe our results and conclusions up from scratch. An overview for necessary preparations for the DALS analysis will reveal which hardware is needed for a simple but highly effective test setup. Even the necessary preparations for the functional testing of the IC which might include some device processing in advance of the measurements will be discussed. We won't hesitate to inform you about the possible difficulties during the testing and will summarize the occurring defects. All this information will be furthermore collected in a best practice guideline which will also be provided in a simple process flow diagram.

2 Background

In order to fully understand the effects which will occur during our analysis we need to make ourself familiar with the fundamental effects between light and matter as well as the principles of failure evaluation on IC's. Therefore we will first take a look at the principal model of atoms. After that, we will deal with the basic principles of laser light and will see how light affects matter based on the properties of the material and the laser light. Furthermore we conclude our introduction with the basic fault models in integrated circuits as well as possible detection methods and will show the correspondence to the fundamental effects. We will keep it as simple and sharp as possible and will provide proper literature for further reading and more detailed information for interested readers.

2.1 Atom Structure

An atom is the basic unit of matter and basically consists of a nucleus which is built up of positively charged protons and neutrons which have no charge. This nucleus is surrounded by negatively charged electrons which move around the nucleus at fixed paths. These fixed paths are called orbitals. This postulate has been made by Niels Bohr[1] due to the experience from the scattering experiments made by Ernest Rutherford[2]. For simplicity, we will take a look at the hydrogen atom which consists of one proton and one electron. The Coulomb force acts between the proton and the electron and is an attractive force between both particles whereas the centrifugal force acts on the electron into the opposite direction as the Coulomb force.

[1] Niels Henrik David Bohr (1885-1962) was a Danish physicist who worked out the todays understanding and basic configuration of the atom structure as well as quantum mechanics.

[2] Ernest Rutherford (1871-1927) is known to be the father of nuclear physics. He discovered the Proton as well as the particle scattering due to the condensed atom nucleus.

This approach leads to the solution that there only exist fixed energy levels for the electron which lead to the following equations:

$$E_n = -\frac{1}{2}\frac{e^2}{a_0}\frac{1}{n} \tag{2.1}$$

where

n: is the quantum number which labels the orbit $n = 1, 2, 3, \ldots$

and

$$a_0 = \frac{\hbar}{me^2} \tag{2.2}$$

where

h: is Planck's constant $h = 6.62606957$ E-34 Js
$\hbar$: is the reduced Planck constant $\hbar = \frac{h}{2\pi} = 1.054571726$ E-34 Js
m_e: is the effective electron mass $m_e = 9.10938291$ E-31 kg
e: is the elementary charge $e = 1.60217657$ E-19 C
a_0: is Bohrs atom radius

The full derivation of this context can be reviewed in *Physik der Halbleiterbauelemente* by Thuselt, 2011. As we can observe, the solution from 2.1 for given n gives us only quantized energy levels for the observed electron in the hydrogen atom. If an electron changes it's state from one energy level to another, the excess energy must be conserved due to the law of energy conservation. The law of energy conservation states, that energy itself cannot be annihilated but it can change its form (e.g. kinetic energy to potential energy). For this reason we will take a look at the particle-wave duality of light. Within interference experiments from Thomas Young[3] (double slit experiment) there has been shown, that light is behaving as a wave particle. The photoelectric effect which was recovered by Heinrich Hertz[4] and Philip Lenard[5] has shown additionally that light can also act as a particle. Within the photoelectric effect, free electrons are generated by shining light of a specific wavelength on a metal surface.

[3]Thomas Young (1773-1829) is known to establish the wave theory of light which he has demonstrated in his famous double-slit experiments.

[4]Heinrich Rudolf Hertz (1857-1894) was the first scientist who proved the existence of electromagnetic waves.

[5]Philipp Eduard Anton von Lenard (1862-1947) did his comprehensive work on cathode rays.

This observations have been summarized by Albert Einstein[6] who showed the connection between the wavelength of light and it's representative energy through the following equation:

$$E = h\nu = h\frac{c}{\lambda} \tag{2.3}$$

where

c: is the speed of light $c = 299792458\,m/s$
ν: is the frequency of the used light source
λ: is the wavelength of the used light source $\lambda = \frac{c}{\nu}$

Using the introduced equation 2.3 it is very simple to calculate the representative energy of a photon emitted by a monochromatic laser light at given wavelengths λ as we will use it further on in our experiments.

wavelength nm	energy eV
800	1.550
1064	1.165
1300	0.954

Table 2.1: photon energies at given wavelengths λ

In table 2.1 we are introducing the energy levels in eV which differ slightly from equation 2.3 due to the normalization with the elementary charge which is a much more common way to describe energy levels in atom physics. From a more detailed point of view we would have to take a look at quantum mechanics, because the probability to actually observe an electron at a specific point in space is described due to a probability density function which results from the solution of the Schrödinger[7] equation

$$\hat{H}\psi(r) = E\psi(r) \tag{2.4}$$

[6] Albert Einstein (1879-1955) is most commonly known due to his formulation of the mass-energy equivalence formula. He also did extensive research on quantum mechanics and also stated the general relativity theory.

[7] Erwin Schrödinger (1887-1961) is known for the formulation of the Schrödinger equation as well as his work regarding quantum mechanics.

where

$\hat{H}$: is the Hamilton operator
$\psi(r)$: is the wave function of the electron
E: is the energy of the electron

The probability to find a quantum-mechanical particle at a specific point in space would be therefore given by

$$\rho(r) \propto |\psi(r)|^2 \tag{2.5}$$

where

$\rho(r)$: is the probability density function

Interested readers in solving the Schrödinger equation 2.4 might take a look at a simple example called *particle in a box* and the *wave equation*. For our observations we will stick to the basics of Bohr's atom model which regard fixed energy levels (orbitals) for electrons in an atom and continue with the interactions of light and matter.

2.2 Light and Matter

The previous denoted energy conservation problem can be easily resolved due to the interaction of light and matter which is also represented in figure 2.1. If a light particle also called *photon* excites an electron from a low energy state into a high energy state, the process is called *absorption* because the photons energy is absorbed by the electron. If an electron changes its state from a high energy state to a low energy state, the surplus energy will be conserved by emitting a photon. This process is called *spontaneous emission*. Due to equation 2.3 the energy of the photon and therefore its representative wavelength and frequency will be defined due to:

$$E_{photon} = h\nu = E_1 - E_2$$

The third possible interaction of light and matter can be observed if a photon stimulates an electron from a high energy state into a low energy state whilst emitting a photon of the same wavelength and phase as the incoming photon. This process is called *stimulated emission* and is used for example to create monochromatic laser light.

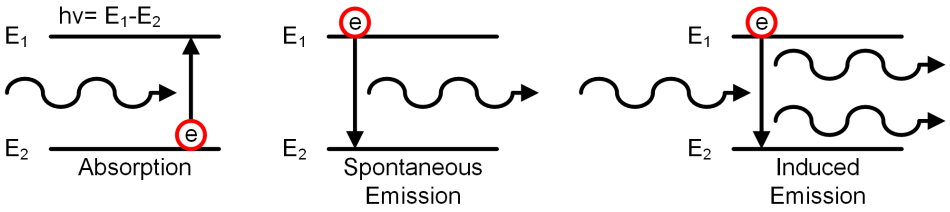

Figure 2.1: Light Interaction

During our observations with *DALS* we will get in contact with each of the three mentioned interaction processes. *Absorption* will be useful for active beam based failure analysis where we will also make use of *stimulated emission* whilst stimulating the DUT with a $\lambda = 1300\,nm$ laser. *Spontaneous emission* will be used for passive beam based failure analysis. We will enlighten the use of these methods further on in the upcoming chapters.

Up until now we have made our observations only for the hydrogen atom, but the same concept holds for any kind of matter. Furthermore we have to make ourself familiar with the band model. Due to the interaction of multiple electrons with each other and the crystal structure of matter, the energy bands from Bohr's atom model won't be defined quite sharply but will smear out. Due to the famous relation of de Broglie[8] and the observations from Arthur Compton[9] it is known that an electron has a representative matter wave which is described by the equation

$$p = mv = \frac{h}{\lambda} = \hbar k \tag{2.6}$$

where

p: is the impulse
m: is the mass
v: is the velocity
k: is the wave vector $|k| = \frac{2\pi}{\lambda}$

This relation can be furthermore used to calculate the kinetic energy of an observed particle.

$$E = \frac{mv^2}{2} = \frac{p^2}{2m} = \frac{\hbar^2 k^2}{2m} \tag{2.7}$$

[8]Louis-Victor Pierre de Broglie (1892-1987) has made fundamental contributions to the quantum theory as it is known nowadays. He stated that all mater has wave properties.

[9]Arthur Holly Compton (1892-1962) observed the scattering of alpha particles on graphite.

From this equation it can be derived that if an electron changes its energy state from a low energy state to a high energy state, or vice versa, the momentum of the electron needs to be conserved. Typically and without influence due to any possible energy source, an atom will always inhabit the lowest possible energy state. Therefore the band with the highest energy which is inhabited by an electron is called the valence band. The next possible band which has a higher energy state than the valence band will be called conduction band and the difference between both energy bands is called band gap. As for an example, the band gap of pure Silicon is about the size of $E \approx 1.1\,eV$. Due to the interference phenomenas of matter waves (constructive or destructive interference) it is possible, that the energy state in the single atom bands depend on the wave vector k as it can be seen in the schematic in figure 2.2. For this reason we have to distinguish two different band gaps:

- direct band gaps
  The maximum energy state of the valence band and the minimum energy state in the conduction band are located at the same wave vector k.
- indirect band gaps
  The wave vector k differs for the maximum energy state in the valence band and the conduction band.

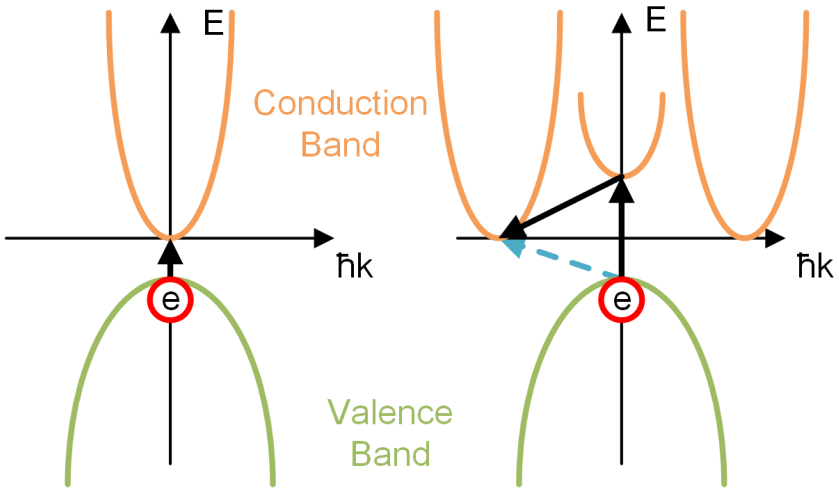

Figure 2.2: Energy Bands

If the observed material has an indirect band gap, as it is the case for silicon, the difference in the momentum is conserved due to lattice vibrations of the crystal which are known as *phonons*. Phonons are quasi particles which can be interpreted as the lattice vibrations due to thermal excitation or acoustic modes. If an electron of a silicon crystal is being excited due to the absorption of a photon from the valence band into the conduction band, the difference in momentum will have to be conserved due to phonons. The momentum conversion due to phonons is very well described in *Solid State Physics* by Grosso and Parravicini, 2003. Additionally, if the energy of a photon is not sufficient to excite an electron from the valence band into the conduction band, the surplus energy can also be conserved due to phonons which can lead to additional lattice vibration and thermal excitation. As it already has been derived, the energy for a light source with a wavelength of $\lambda = 1300\,nm$ is $E = 0.954\,eV$ and the average band gap of silicon is about the size of $E \approx 1.1\,eV$. At the first glance, with a light source of $\lambda = 1300nm$ only thermal excitation of the silicon crystal will be possible, but there also exists phonon assisted absorption.

This process has been supposed by A. Glowacki and Boit, 2005 where they described a small measurable current produced in a p-n junction of a test structure whilst stimulated by a $\lambda = 1300\,nm$ wavelength laser beam. Noffsinger et al., 2012 give a more detailed explanation for the so called *intraband light absorption* which describes phonon assisted processes for indirect band gap semiconductors. The model which is used most of the time to mathematically describe the electron-phonon interaction is the configuration coordinate model. Amato, 2002 states that the phonon assisted absorption can be influenced in two ways. The absorption of a phonon during thermal laser stimulation can cause the band gap to narrow down as the conduction band energy is lowered. Whereas during phonon emission the conduction band energy is increased and therefore the band gap is broadened. This behavior is used for absorption enhancement in amorphous Si solar photo voltaic cells as Kim and Kaviany, 2010 are mentioning in their work. Due to the additional momentum of the phonons, the absorption process itself can be nearly interpreted as in a direct band gap semiconductor. Moreover the phonon interaction dominates the absorption behavior of the used crystal in comparison to other thermal related effects.

Handbook of Optics from Bass et al., 1995 and *Solid State Physics - Optical Properties* from Dresselhaus, 2001 give a more detailed overview of the above described happenings.

It is mentioned that the phonon energies are usually very small $E_g \leq 0.050\,eV$ and that the absorption coefficient can change by several powers of 10 over the whole absorption spectrum. Furthermore the absorption or emission of phonons can occur due to several processes which increases the difficulty of correct observation and outcome prediction. There exist

- Transverse Acoustic - TA
- Longitudinal Acoustic - LA
- Transverse Optic - TO
- Longitudinal Optic - LO

phonons which influence the fundamental absorption edge and therefore the band gap of the used material. In *Solid State Physics - Optical Properties* the influence of temperature on phonons is given. Cite: *At low temperatures, the phonon emission process dominates because there are so few phonons available for the absorption process. On the other hand, phonon emission does not depend upon the availability of phonons since the emission process itself generates phonons; for this reason the phonon emission process is relatively insensitive to temperature.* In contrast to phonons, the band gap of the used material is temperature dependent due to the thermal expansion and contraction of the lattice which can be calculated due to simplified equations from empirical fits

$$E_g(T) = 1.165 - 2.84\ T\ \text{E-04}\,eV \quad \ldots \text{Silicon} \tag{2.8}$$

$$E_g(T) = 0.742 - 3.90\ T\ \text{E-04}\,eV \quad \ldots \text{Germanium} \tag{2.9}$$

where

T: is the temperature $T\ in\ K$

Furthermore it is very simple to calculate the necessary photon energy for a phonon assisted absorption process as it is written in equation 2.10.

$$\hbar\omega = E_f - E_i \pm \hbar\omega_p \tag{2.10}$$

where

E_f: is the energy in the final state
E_i: is the energy in the initial state
ω: is the circular frequency of the involved photon
ω_p: is the circular frequency of the involved phonon

The $\pm$ sign in equation 2.10 is an abbreviation for

$$\alpha_{abs}(\omega) = C_a \frac{\left(\hbar\omega - E_g + \hbar\omega_p\right)^2}{exp\left(\frac{\hbar\omega_p}{k_B T}\right) - 1} \tag{2.11}$$

With this knowledge of light and matter interactions as well as the law of energy conservation one might ask where this interactions might occur within an observed piece of material. An incoming light ray might not interact with an electron in the first layer of atoms of a material structure but will travel through the material up until a certain point. The absorption of light can be very easily observed if a light ray with the intensity of I_0 passes through a probe of a specific thickness d as it is shown in *Laser - Bauformen, Strahlführung, Anwendungen*, chapter 2 by J. Eichler and H. J. Eichler, 2010. Due to the absorption of light, the intensity of the light wave will be reduced according to the properties of the probe's material and the wavelength of the light. This process has been described due to the Beer-Lambert law[10] of absorption.

$$I(x) = I_0 e^{-\alpha x} \tag{2.12}$$

where

α: is the absorption coefficient of the material
x: is the penetration depth of the light wave

The following table 2.2 is showing some typical absorption coefficients for some pure metals and for silicon at given wavelengths which might occur during the fabrication of a typical integrated circuit. As one can easily observe, the absorption coefficient at the given wavelength for metals is much higher than for silicon. This data has been looked up at Honsberg and Bowden, 2014 and Polyanskiy, 2014. The derivation start of equation 2.12, as well as the decrease of the intensity of a light ray while passing through an arbitrary material, can be seen in figure 2.3. The amount of absorption is strongly dependent of the material's characteristics just like the density of the absorbing atoms or molecules as well as the wavelength of the light wave.

[10]Named after August Beer (1825-1863) who is most commonly known for is work on absorption of light and Johann Heinrich Lambert (1728-1777) who has proven the irrationality of π.

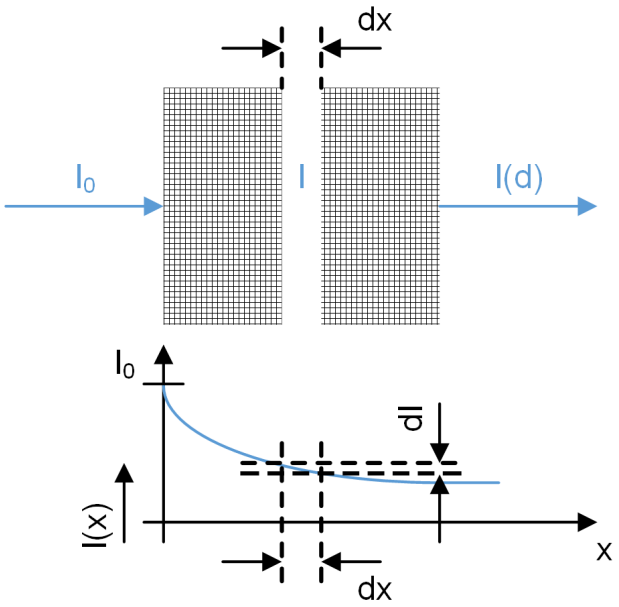

Figure 2.3: Light Absorption

wavelength λ	$800\,nm$	$1064\,nm$	$1300\,nm$
absorption coefficient	α_{800} $1/cm$	α_{1064} $1/cm$	α_{1300} $1/cm$
Aluminium	1.299 E+06	1.180 E+06	1.217 E+06
Copper	7.859 E+05	8.345 E+05	8.432 E+05
Silicon	8.500 E+02	1.110 E+01	4.500 E-05
Tungsten	4.466 E+05	4.423 E+05	4.197 E+05

Table 2.2: Absorption Coefficients for Different Materials and Wavelengths

The absorption coefficient of silicon for a wavelength of $\lambda = 1300\,nm$ is around $\lambda = 4.500\text{E-}05\,1/cm$ and given in table 2.2 which is a very small value. In other words, if we want to reduce the intensity of a light ray by $\frac{1}{10}$ of its original value, the silicon probe where the light has to pass through must be about

$$x = -\frac{\ln\left(\frac{9}{10}\right)}{\alpha} = -\frac{\ln\left(\frac{9}{10}\right)}{4.5E-05} = 2.34\ \text{E+01}\,m$$

thick. For IC production applications this value is far beyond typical values for silicon wafers, therefore at the observed wavelength, silicon will be nearly transparent. For further information figure 2.4 is showing the absorption coefficient α of pure silicon in dependence of the wavelength λ and has been looked up at Honsberg and Bowden, 2014. Furthermore we can carry

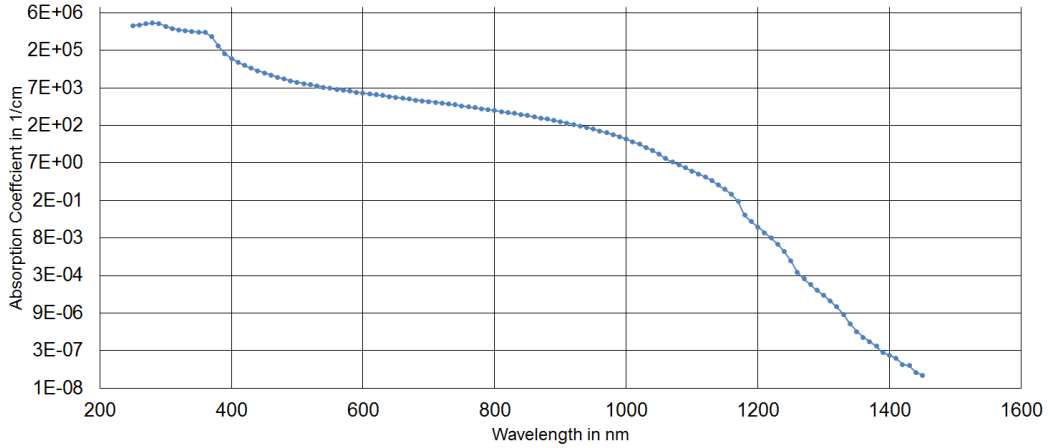

Figure 2.4: Absorption Coefficient of Silicon

out the same calculation for the given absorption coefficients from table 2.2 and will receive the absorption depth values given in table 2.3. Out of this simple calculation we can clearly observe the strong changing absorption depth of silicon in dependence of the used wavelength. The absorption depth even changes by multiple powers of ten! Therefore we will observe during our measurements, that with the use of a $\lambda = 1300\,nm$ wavelength light source, we won't observe any stimulation of the integrated circuit if we aren't able to focus the light source on a structure with a much higher absorption coefficient.

wavelength λ depth x	800 nm m	1064 nm m	1300 nm m
Aluminium	8.111 E-10	8.929 E-10	8.657 E-10
Copper	1.341 E-09	1.263 E-09	1.250 E-09
Silicon	1.240 E-06	9.492 E-05	2.341 E+01
Tungsten	2.359 E-09	2.382 E-09	2.510 E-09

Table 2.3: Absorption Depth for Different Materials and Wavelengths

2.3 Laser Light

Laser is an acronym and stands for *Light Amplification by Stimulated Emission of Radiation*. There exist various applications as in industry, medicine and science and their function has been described in many publications and books such as in *Laser - Bauformen, Strahlführung, Anwendungen* by J. Eichler and H. J. Eichler, 2010, *Laser Material Processing* from Steen, Watkins, and Maumder, 2010 as well as in *Laser Heating Applications - Analytical Modeling* by Yilbas, 2012.

The main observables to describe a laser are its wavelength (m), the power (mW), the pulse energy (J) as well as the beam diameter (spot size) and the beam profile (spatial intensity distribution).

The working principle of a laser is simply based on *spontaneous* as well as *stimulated emission*. The only difference between both emission types is, that during the spontaneous emission the generated photon can be emitted into any possible direction. On the other hand, if we are observing stimulated photon emission, the emitted photon will travel into the same direction as the photon which has stimulated the emission. The emitted photon will even inherit the same frequency ($\nu = c/\lambda$) and phase of the incoming photon. As we can now picture in our mind, absorption processes might even occur at the same time than the discussed emission! To achieve an amplification of the desired light ray, more electrons must be stimulated into the conduction band, than there are electrons in the valence band which is also known as to create a *population inversion*. The underlying stimulation process is generally known as *optical pumping*.

Optical pumping can be achieved due to the following excitation techniques:

- electron impact ionization: noble gas ion lasers
- chemical reactions: hydrogen fluoride lasers
- gas dynamic reactions: CO_2 lasers
- light: not as common as other techniques

To increase the probability of stimulated emission and to furthermore create population inversion, the laser must be built out of an active material. If the amplification factor of the used material is very high or the length along the propagation direction is long, it might be sufficient for photons to pass once through the material. In practice often a combination of mirrors and active material is used as it is showed in figure 2.5 because the amplification capability of a specific material and the physical construction size is often limited. Due to the reflectance of the mirrors and their proper arrangement it is possible to control the amount of photons which are emitted out of the active material. One mirror is designed to have a reflectance of nearly 100 % whereas the second mirror will have a lower reflectance. The reflectance ρ

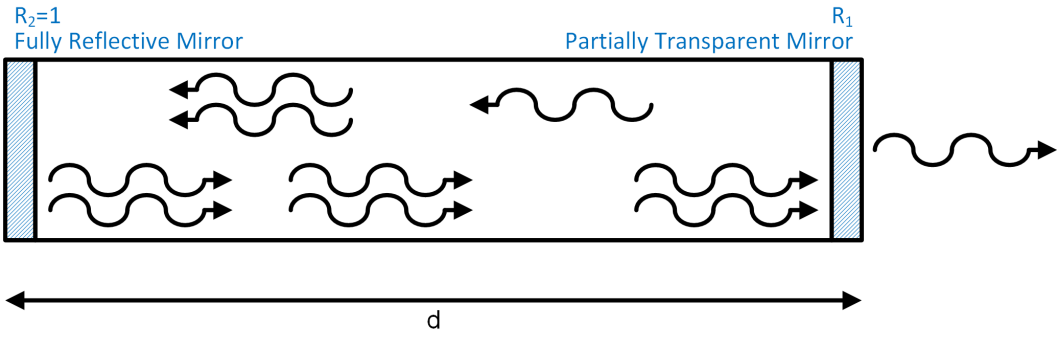

Figure 2.5: Laser Structure

and transmittance τ factors of a material describe the amount of photons which are able to pass through a material. Both factors are highly dependable on the wavelength as well as the polarization direction of the observed light. If the reflectance is at 100%, no photon will be able to pass through the material, which is a desired effect for common mirrors. The transmittance factor of a material describes the ability of a photon to pass through the material and is linked to material absorption α by

$$\alpha = 2 - \log(\tau[\%]) \tag{2.13}$$

wavelength λ	800 nm %	1064 nm %	1300 nm %
Aluminium	86.819	94.749	96.777
Copper	96.902	97.078	97.148
Silicon	32.940	31.625	30.882
Tungsten	50.429	60.267	64.873

Table 2.4: Reflectance Factors for Different Materials and Wavelengths

which is also represented in figure 2.6. For optical lenses it is desired to gain a transmittance factor of 100% in order to increase the observability of a given object and to reduce unwanted effects just as reflection and absorption.

$$\rho + \tau = 1 \tag{2.14}$$

Table 2.4 is showing reflection factors for some common materials in IC

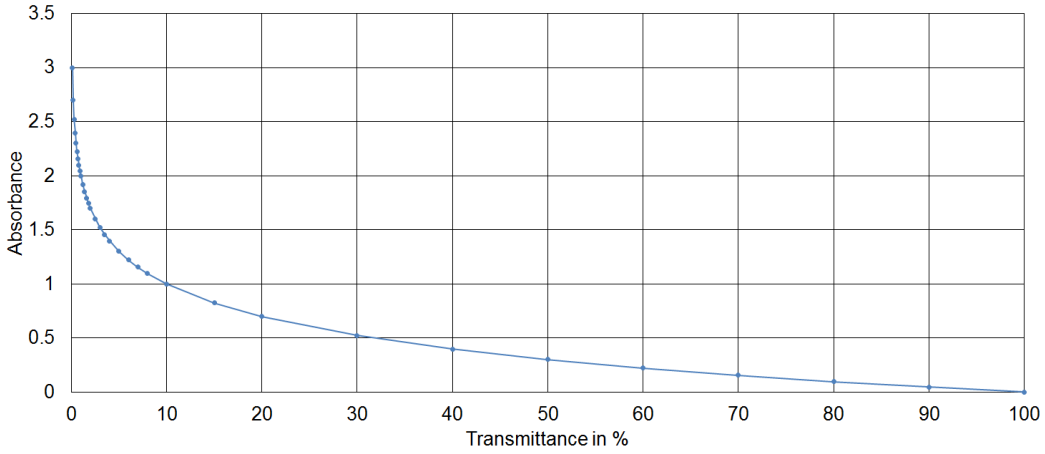

Figure 2.6: Transmittance and Absorption Correlation

production and have been looked up at Polyanskiy, 2014. Up until now we have described the emission process just for static energy levels where the wavelength of the emitted photon is described by equation 2.3 and therefore dependent on the energies of the valence band E_1 and conduction band E_2. In practice, the energy levels of the valence and conduction band will not be defined sharply, but will smear out a little bit.

This uncertainty is called *line broadening* and will lead to the creation of a wavelength spectrum which is an undesired effect for monochromatic laser light. Due to several broadening effects, the waveform spectrum is often described by common known distributions at it is shown in figure 2.7.

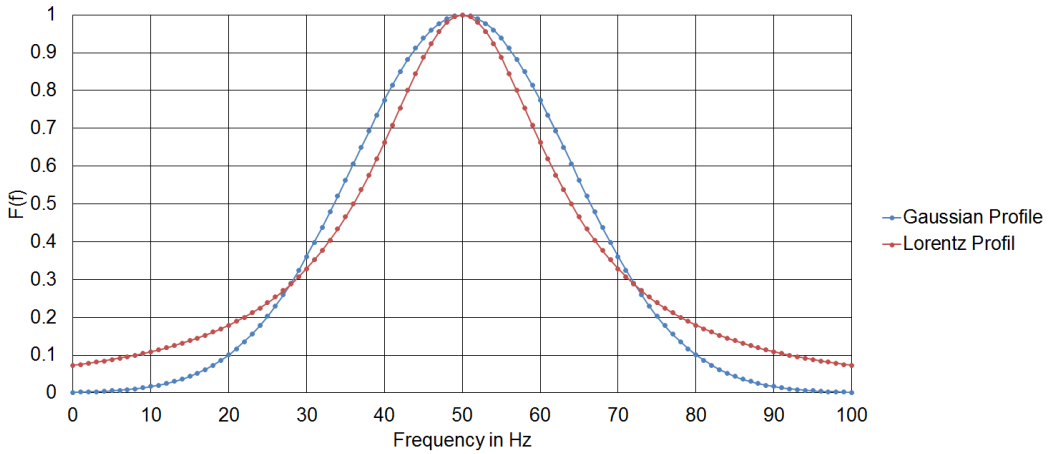

Figure 2.7: Wavelength Uncertainty - Distribution Example

If an electron is being excited into a higher energy band than the valence band it will inhabit the new energy level for a specific lifetime. This material specific lifetimes can be used to describe the natural line widths which form a *Lorenz profile* like it is shown in figure 2.7. In comparison to the following line broadening processes the influence of natural line width broadening can be neglected most of the time.

- homogeneous line broadening
  - atom and molecule collisions
    The half life time will be alternating due to scattering events of electrons and molecules. The half life time can be calculated due to the mean free time, where no collision of atoms and molecules occur.
  - lattice vibrations
    Thermal excitement and phonon interactions in the active material will cause a Lorenz distribution shaped line width profile.

- inhomogeneous line broadening
  - Doppler broadening
    Not all atoms and molecules will have the same velocity and propagation direction during the introduced absorption and emission processes. Therefore the *doppler effect* will lead to additional line broadening.
  - Stark effect
    With the presence of an external electric field the absorption and emission processes will be alternated.

The introduced line broadening effects will occur in most of the commercially available lasers and therefore it is mandatory to select the proper product for the desired application. Furthermore the laser beam profile will have a huge impact on the application. As it is known from geometric optics, light is spreading out linearly in bundles but it is also common to describe the locomotion of a light ray with the interpretation of spherical waves. Both cases are nevertheless not directly applicable for laser light. Figure 2.8

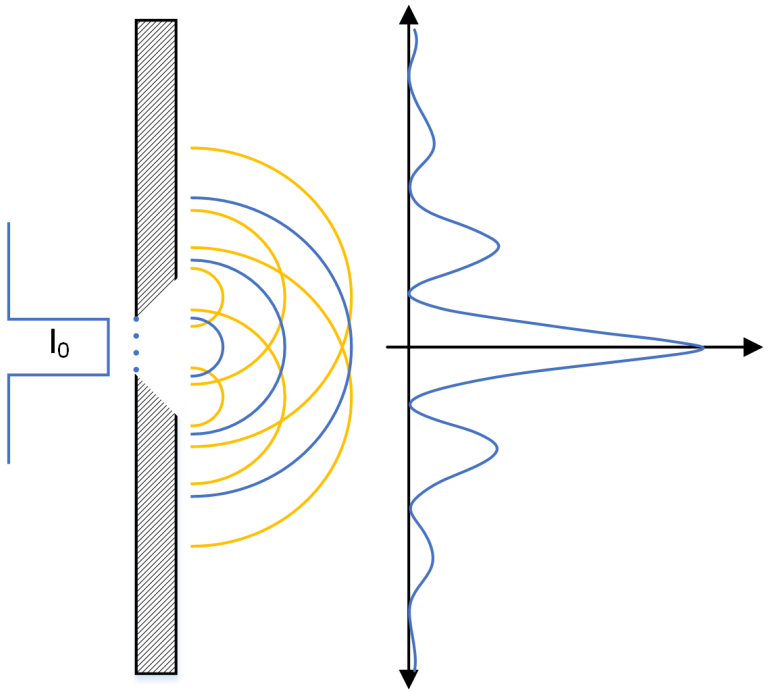

Figure 2.8: Diffraction Principle

is representing the occurring effects as it is described with *Hyugens principle*.

Within this principle a plane wave, which might be emitted by a laser light source, is diffracted at an aperture and at the same time spatially limited due to the diameter of the aperture. Observations tell us, that the originally flat top profile from the laser light is then changed due to diffraction at the aperture to a Gaussian distribution profile. Even if the original light profile follows another distribution like a Gaussian or a Normal profile, the resulting distribution will be Gaussian profile. This behavior can be explained due to additive and extinctive spherical waves which emerge at the virtual axis of the aperture as it is shown in figure 2.8 and sum up at a detector. The occurring profile minimums depend on the lights wavelength, as well as the diameter of the aperture and can be described due to

$$\sin(\theta) = \frac{k\lambda}{d} \tag{2.15}$$

where

λ: is the wavelength of the light
d: is the diameter of the aperture
k: follows $k = \pm 1, \pm 2, \ldots$
θ: is the angle with respect to the incoming plane wave and the center of the aperture (*divergence angle*)

Equation 2.15 shows, that due to the path difference of the spherical waves multiple minimums can be created at a detector. This property makes it very difficult to determine the radius of the light beam. Even absorption and transmission processes will be much harder to describe, as we will observe in further chapters.

ISO 11146 states, that the beam width is defined as the $1/e^2$ point of the second moment of intensity. In other words it describes the point where the intensity of the ground mode of the light wave reaches the intensity of $I_{w0} = \frac{I_{max}}{e^2}$ as it is shown in figure 2.9 and in equation 2.16 where $I \sim |E|^2$ and E states the solution of the *wave equation* which has been mentioned for the solution of equation 2.4.

$$\frac{I}{I_{max}} = e^{\left(\frac{-2r^2}{w(z)^2}\right)} \tag{2.16}$$

where

$w(z)$: is the beam radius of a Gaussian profile shaped laser light beam in dependence of the propagation direction length
I_{max}: is the maximum intensity of the laser light beam

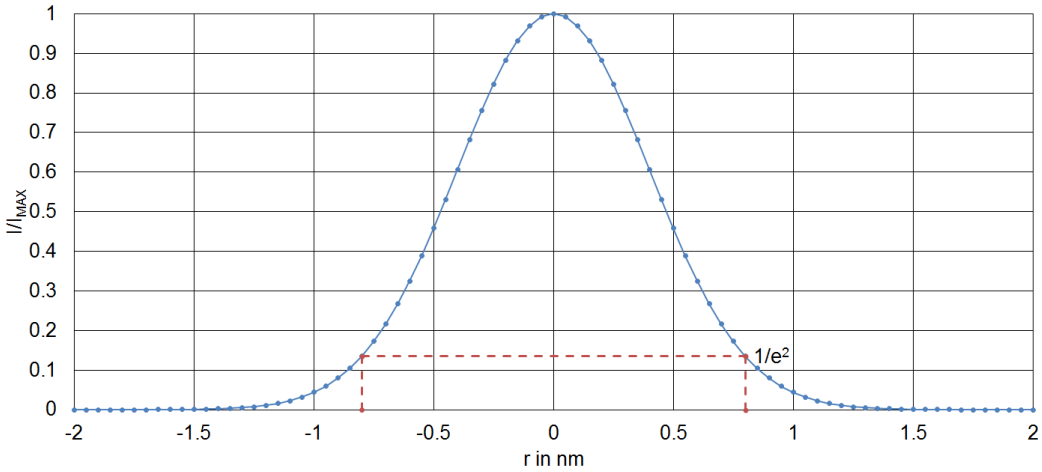

Figure 2.9: Beam Width

This definition is sometimes very hard to work with in practice because of ambient light distortion or distortion resulting from CCD-based beam width measurement systems but it is the most common one. With this definition we can easily calculate the laser power because it results out of the integration from equation 2.16 over the beam area

$$P = \int I d\Gamma = \frac{\pi w(z)^2 I(z)}{2} \tag{2.17}$$

It is also possible to describe the beam width according to its propagation direction as it can be seen in figure 2.10. For a Gaussian beam which results due to diffraction limits, the beam radius w_0 can be described at the point, where the beam radius decreases by the factor of $\sqrt{2}$ which also results in the definition of the *Rayleigh Range* z_r and the *focal length* $b = 2z_r$.

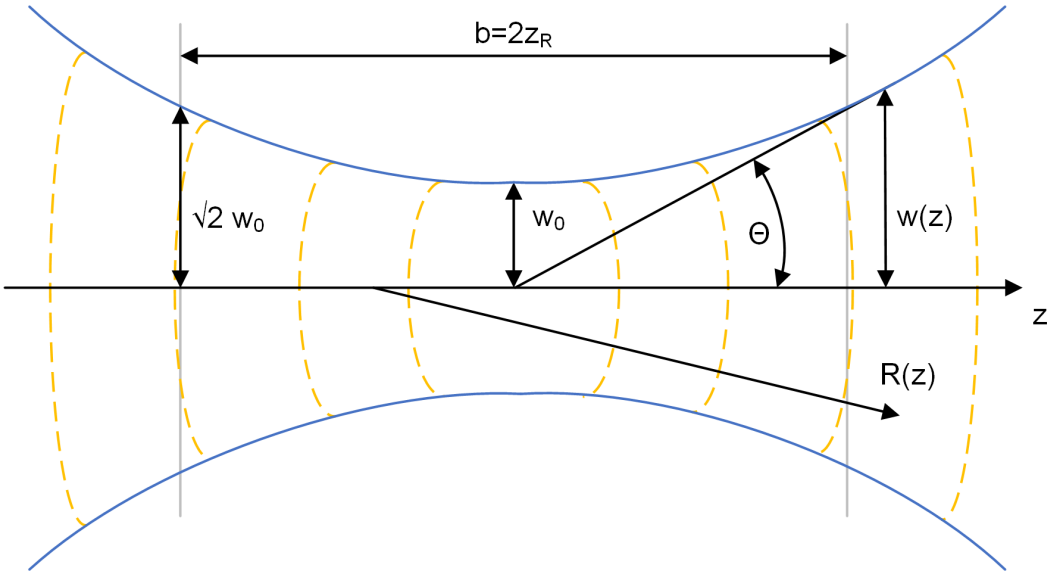

Figure 2.10: Beam Width in Radiation Direction

$$w_0 = \sqrt{\frac{z_r \lambda}{\pi}} \rightarrow z_r = \frac{w_0^2 \pi}{\lambda} \tag{2.18}$$

Equation 2.19 can be furthermore used to calculate the beam radius in dependence of the propagation direction z

$$w(z) = w_0 \sqrt{1 + \left(\frac{z}{z_r}\right)^2} \tag{2.19}$$

and equation 2.20

$$\theta = \frac{w_0}{z_r} = \frac{\lambda}{\pi w_0} \tag{2.20}$$

approximately states the angle of divergence for the laser beam. The beam radius w_0 and the Rayleigh Range z_r are most commonly used to describe the properties of a laser.

For laser stimulation techniques as we are going to describe in this work, it is also most common to use lenses to alternate the focal point of a laser in order to increase the accuracy of the measurement method as well as to decrease the size of the stimulated area due to the beam waist w_0. The basic laws of geometrical optics can be used to approximately describe the beams behavior as it can be seen in equations 2.21, 2.22 and figure 2.11 if diffraction processes are neglected.

$$\frac{1}{f} = \frac{1}{b} - \frac{1}{g} \tag{2.21}$$

where

f: is the focal length measured from the virtual axis of the lens
The focal length will be the same for the left and right hand side of the used lens if the space surrounding the lens itself is made up from the same material (e.g. air).
b: is the image distance measured from the virtual axis of the lens
g: is the object distance measured from the virtual axis of the lens

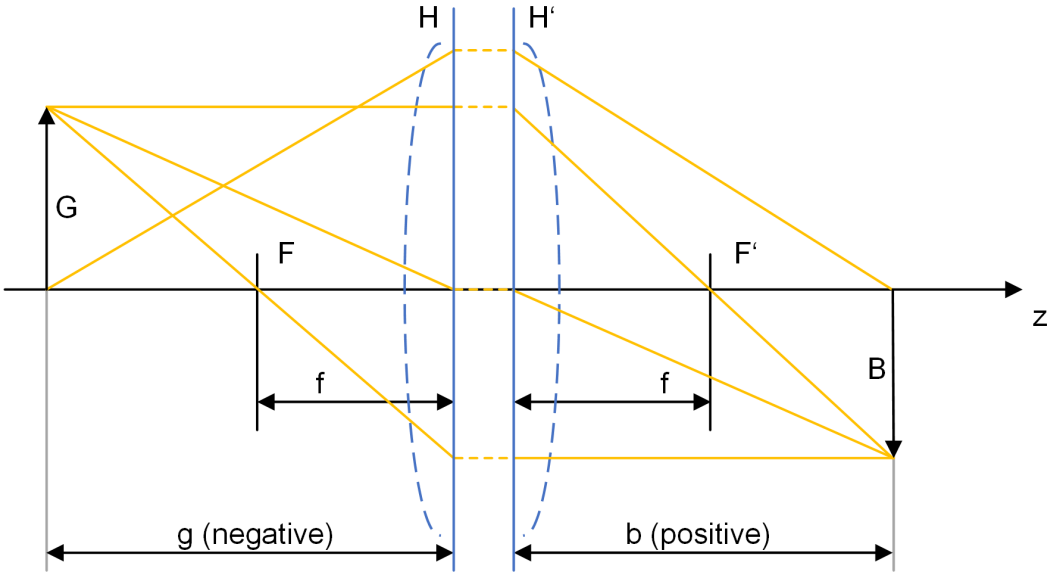

Figure 2.11: Geometrical Optics

$$\beta = \frac{B}{G} = \frac{b}{g} \tag{2.22}$$

where

β: is the image scale
B: is the image height
G: is the object height

Lens manufacturers often tend to describe the properties of their products and the corresponding calculations of light beams in an even more practical way like it is noted in the following list and summarized from the product portfolio of *Mitutoyo*[11].

- numerical aperture - NA
  The numerical describes the optical resolution capability of a lens. It is correlated to the resolving power, the luminosity (transmittance) as well as the depth of field. The higher the numerical aperture is, the more details will be observable under controlled conditions.

  $$NA = n \sin(\theta) \tag{2.23}$$

  where

  n: is the refraction index (e.g. for air: $n = 1$)
  θ: is the angle of divergence
  NA: is the numerical aperture

- Spot Diameter
  Due to the properties of the lens, the original beam waist and focal length will be alternated. The spot diameter therefore states the resulting beam waist of finite size. Summarizing there exist two ways of calculating the resulting beam waist. The first one is quite simple and should not be used for laser application purposes but it gives a clue about what beam waist is about to being expected.

  $$w_0 = 1.22 \frac{\lambda}{NA} \tag{2.24}$$

  If the beam waist is again calculated due to the intensity distribution and the radius where the intensity distribution reaches $1/e^2$ of its peak value, it is possible to use the simplified equation.

  $$w_0 = \frac{4\lambda f}{\pi D} \tag{2.25}$$

[11] `http://www.mitutoyo.com`

- Pupil Diameter - D
  Describes the maximum beam waist of a light bundle which is able to enter the lens without spatial limitations. See figure 2.12.

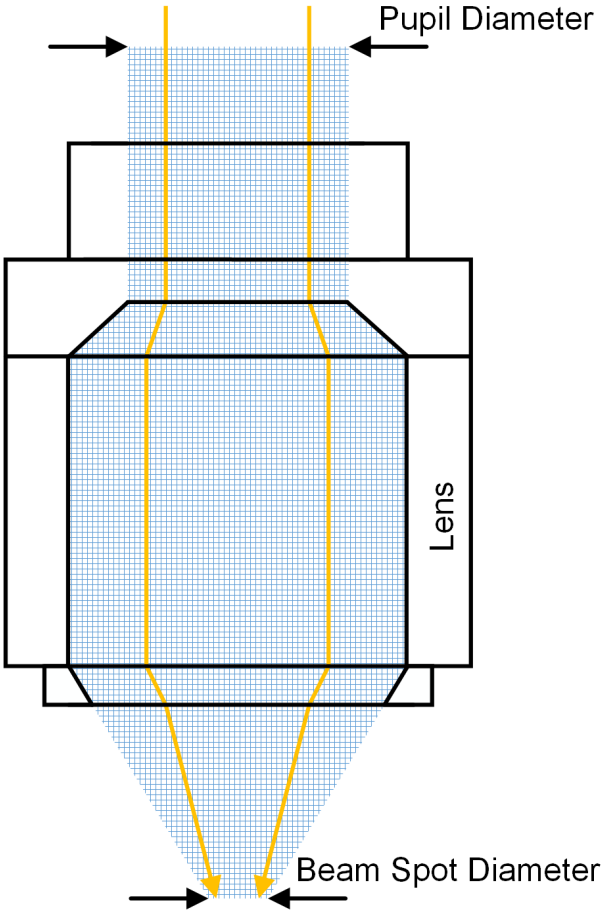

Figure 2.12: Pupil and Spot Diameter of a Lens

- resolving power - R
  Describes the smallest space between two juxtaposed structures

$$R = \frac{\lambda}{2NA} \tag{2.26}$$

- Working Distance - WD
  The distance between the lens and the observed object, when the object is in focus.

- Depth of Field - *DOF*
  Describes the allowed variation of the focal length, where the object still appears to be focused and the observed image still leads to an acceptable result.

For failure detection purposes in IC production the desired behavior for optical beam based failure detection techniques is quite simple and can be summarized by the following items:

- Laser Light Source
  - The spatial intensity distribution of the laser should show a flat top profile with no diffraction effects.
  - A small beam waist leads to a punctual stimulation of the IC which decreases the size of the stimulated area and therefore increases the precision of failure localization.
  - Monochromatic laser light with negligible broadening effects and thus a single wavelength light creates a continuous stimulation source with constant energy.
  - The wavelength must be chosen in a way, that only active areas (p-n doped regions) of the IC are stimulated.
- Optical Lenses
  - Optical lenses should have a transmittance of 100 % to make advantage of the full laser light intensity.
  - Multiple lenses with different magnification sizes are preferred in order to decrease analysis time and increase detail of the analysis.

These proposed properties can de facto not be realized under normal operating conditions. The spot size of the used light source will always be dependent of the used magnification lens and the spatial intensity distribution will also follow most probably a Gaussian distribution profile. Additional influences from the test setup might be the limited transmittance of the used lens as well as ambient temperature and light influence, as well as dust particles from the surrounding area of the test setup. Furthermore the output of an optical system clearly depends on the user who needs to adjust the working distance properly to get a focused image of the observed area.

3 Defect Localization

Defect localization is one of the most challenging tasks in semiconductor production. There exists a vast kind of possible faults and defect locations resulting from bad design, a bad layout or simple production variations as well as electrical over stress in the application. A defect in a circuit which might be represented by a short, open or floating contact and can lead to several errors in the IC, which may be only recovered if the IC is in a specific working or load condition or if a certain logic combination is applied to its inputs. Therefore with increasing number of inputs and complexity of the IC itself the difficulty for failure detection, localization and characterization increases exponentially. Just as Chunlei, L. Zhai, Motohiko, Liu, et al., 2009 and Chunlei, Motohiko, et al., 2011 have mentioned in their papers, a simple failure analysis process consists of the main steps which are shown in figure 3.1.

The goal of each IC manufacturer is to deliver products at a failure rate of almost zero parts per million. Failures are not said to be non existent in the field but most commonly the first step in failure analysis is to check whether the application in which the integrated circuit is working has been properly set up. If this first failure analysis step has been made, the defective device needs to be checked in a reduced test environment. This test environment should ensure that

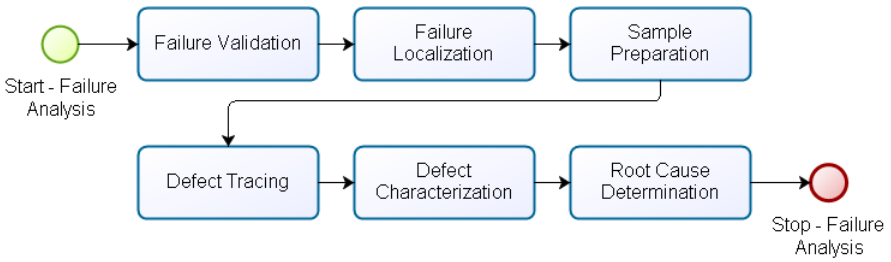

Figure 3.1: Main Steps in Failure Analysis

- all device specifications are met (supply voltage, frequency, operating temperature, loads)
- all registers and test modes are accessible
- all functions of the product are testable
- ambient influences are reduced to a minimum level
- the customers needs are reflected within the test

As this item list is already indicating, the verification of a defect is heavily dependent of a proper test setup. The best test setup in the world must not necessarily ensure that the full functionality of a device can be confirmed since we do not know something about the internal states of the device. For this reason there exist two main items in the design for testability which must be considered under each condition

- Controllability
  As the name already indicates, the controllability describes the access to a specific node at runtime and the possibility to externally set up a nodes value. The node must not directly be accessible, as it can also be sufficient to have access in a serialized kind of way.
- Observability
  The observability expresses the possibility to monitor a value of a node at runtime without changing its actual value. Again the node must not directly be accessible, but for analog logic it is more or less essential, since there would have to be an ADC included in the realization for serial data extraction. An analog test bus is also very hard to realize due to the losses and signal alternations on the test bus.

There exist multiple ways of how to increase the controllability and observability within the development phase of a product. The controllability of a product will ensure that the device can be put in a specific state of operation and the observability will guarantee that all nodes and logic gate outputs can be monitored without repercussion. Summarizing this abilities the goal of a functional test would lead to clear pass or fail result of the device. Creating pass fail events and detecting their threshold of occurrence is next to simply detecting a fault, the main goal in failure analysis. As the following section will show, defects can be dependent of several device parameters and are often very hard to stimulate due to their small range of stimulation.

3.1 Defect Types

First of all, it might be useful to differentiate between the following definitions. A defect is used to be called the difference between the desired design and the actual hardware which has been produced. An error is an effect which results from a defect and can be represented by a wrong output signal. Slight alterations of the output signal like timing or amplitude variations might not be easily detectable since they don't necessarily have to lead to a malfunction, but they represent an undesired behavior of the device. From a model based point of view a defect can be represented on a more abstracted level as a fault. A fault leads to a predictable outcome which creates the opportunity for the simulation of specific states in a defective device and comparison against real device behavior. A defect can be dependent of several operating parameters which can be

- Voltage
- Current
- Frequency
- Temperature
- Humidity
- Ambient Light

In order to be able to keep track of all possible dependencies and outcomes of device simulations and measurements *Shmoo*-plots are used to characterize the device behavior. The term Shmoo itself is a fictional word and originates from a comic figure which quite obviously has nothing to do with the electrical test of an IC. Shmoo plots can be one- or multi-dimensional graphical representations of device specific parameters and represent the pass/fail behavior of a device as well as the pass/fail threshold. Figure 3.2 is representing a two dimensional pass/fail outcome of a fictional but possible device stimulation with dependency of the supply voltage (y-axis) and the operating frequency (x-axis). This simple diagram is clearly showing the devices behavior on the possible input variables and its range of operation. For further defect analysis it is mandatory to operate the device in the region where the pass/fail threshold can be observed, because in this operation mode the device will show most probably an unstable and noticeable state change and will react very sensitive on external stimulation techniques.

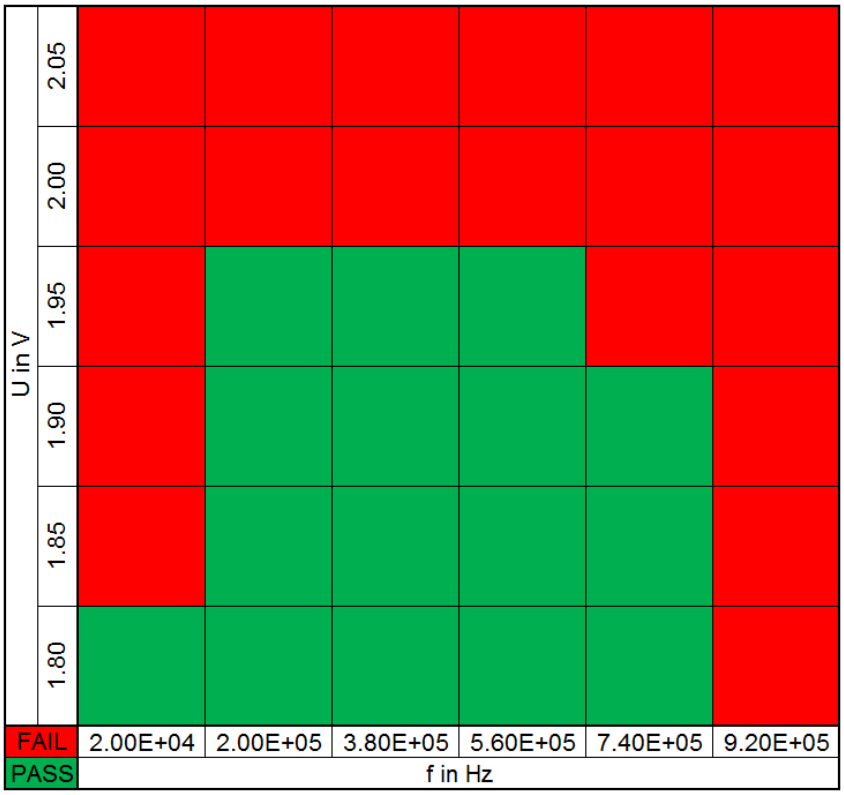

Figure 3.2: Shmoo Plot Example

The following fault models will give a basic overview about how defects are treated during the introduced failure analysis process.

3.1.1 Stuck At Fault

A stuck at fault is represented due to a contact which is fixed at a specific logic state. This might be V_{ss}, V_{dd} or even some other potential used in the device's logic. In failure analysis the term *Stuck At Zero* states that the contact potential is *LOW* which means that the contacts potential might be fixed to *GND* while *Stuck at One* implies the logic state *HIGH* which might be V_{dd}. Just as an example an *AND*-gate with two inputs and one output as it is shown in figure 3.3 has $N = 3$ fault sites which can be affected at once or at the same time and lead to $2^N = 2^3 = 8$ possible failure combinations.

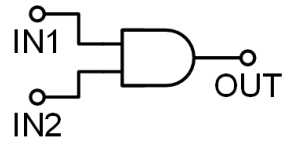

Figure 3.3: AND gate Example

If all fault sites are physically observable from the affected gate, the presented example might be easy to cope with, but in a complex IC with high logic depth it is very complicated to make all the nodes of a single gate observable. Nevertheless, due to the defined states in the *Stuck At Faults* this method is the most used and preferred analysis method and there exist a huge variety of analysis tools. Almost each functional analysis tool and test pattern generator is based on *Stuck At Faults* which use some kind of backtrace algorithms in order to verify faults in the scan chain path of IC's. Backtrace algorithms make use of known node states and the implemented logic function. By fixing a node state, e.g. with stuck at one, it is possible to identify the remaining states of the the in-, and outputs by interpreting the logic function. The goal is to generate custom stimulation algorithms, which can activate the fault of the device with a minimum set of input combinations.

3.1.2 Stuck Open and Short Faults

Apart from the presented *Stuck At Faults*, defects can be modeled in dependency of their physical configuration. These defects might originate in production due to a misaligned setup in the lithography or during improper chemical or mechanical production steps. The result will be misplaced metal paths which can either cause *shorts* or *opens*. *Shorts* lead to a static connection to a specific potential in the IC with negligible losses over the connecting path and will generally cause additional load. This additional load or current can be easily monitored by suitable current or voltage measurements at the input pins of the device. Even if the fault just causes a race condition between two gates for a very short time, a limited increase of current consumption will be noticeable. *Opens* result in a more complex failure situation.

The potential of one side of the open contact will be defined well, whereas the other side of the open contact must not necessarily be defined properly. This leads to a more or less unpredictable behavior which is strongly dependent on the defects characteristics.

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{3.1}$$

where

d: is the width of the open contact
A: is the cross sectional area of the open contact
ε_0: permittivity of vacuum $\varepsilon_0 = 8.854$ E-12 F/m
ε_r: relative permittivity

For simplicity it is common to use the known equation 3.1. We can clearly observe that the capacitance of an open contact will depend on the width and cross sectional area of the open, as well as the relative permittivity of the material in between the two conductors just like for parallel plate capacitors. The coupling material is influenced by the time when the fault will be created in the production process. It is imaginable that the coupling material consists of air, silicon oxide, nitride or other materials used in semiconductor fabrication. Nevertheless, what all these coupling materials will have in common is, that the resulting impedance is dependent on the operating frequency of the open contact as it can be observed in equation 3.2.

$$X_C = \frac{1}{j\omega C} \tag{3.2}$$

where

j: is the imaginary unit
ω: is the circular frequency $\omega = 2\pi f$
C: is the coupling capacitance

Furthermore the capacitance will cause an additional load, which will vary according to the charging and discharging of the capacitor. If an open contact is situated for instance at a clock path which operates at very high frequency and the width of the open contact is narrow, the parasitic coupling capacitance will be very low, but due to the high operating frequency the over all impedance will be very low too. For this combination, the open contact conductor will be defined very well for high frequencies and very poor for low frequencies. Just think of a resistive network and the

resulting voltage divider in this situation. Furthermore temperature is a highly influencing factor on open contacts. Temperature is able to cause material aging, thermal expansion and resistive changes. It is quite obvious that temperature can be used to *heal* a local open contact due to material expansion. This is the foundation for temperature dependent faults in integrated circuits which is a challenging task in failure analysis because a fault might only occur in between a certain temperature-range. For this reason it is most common to create Shmoo-plots for the device sensitive parameters. There is also the option for a *floating node* which is a special form of an *open contact*. The floating node is generally located at the gate of a transistor. The potential of the floating contact will be defined over parasitic capacitances and will cause, depending on its actual potential, the affected transistor to switch on or off. This failure behavior can again be easily monitored by measuring the current consumption of the device. If the region with the affected transistor is powered on, a short increase in the current consumption will be detectable. It has been shown in laboratory measurements, that simple dc-voltage and voltage sweep measurements are a powerful tool to reveal open contacts and floating nodes as it will be shown in the experiments chapter. Furthermore floating nodes are very sensible against ambient light. If light is shown on a floating node, the absorbed energy from the light might be sufficient to define the nodes potential.

3.1.3 Bridging Faults

Bridging faults are a special form of *shorts* with the difference that the resistance of the unintended connections due to metal or poly contacts are not negligible. They can also be interpreted as an unwanted connection between two signal lines, which can cause cross talk or even the determination of a static potential. According to the temperature coefficient of the resistive connection, these defects are able to show an increase or decrease of resistance according to temperature change.

Material	Temperature coefficient $1/K$
Aluminium	4.00 E-3
Copper	3.93 E-3
Gold	3.70 E-3
Tungsten	4.40 E-3
Germanium	−48 E-3
Silicon	−75 E-3

Table 3.1: Temperature Coefficients for Different Materials.

Basically the resistance of a material at a specific temperature can be calculated due to the simplified equation:

$$R_\theta = R_0 \left(1 + \alpha \Delta\vartheta\right) \tag{3.3}$$

where

$\Delta\vartheta$: is the temperature change from the reference
α: is the temperature coefficient
R_0: is the reference resistance
R_ϑ: is the resulting resistance at the observed temperature

which can be used for temperatures below $100\,^\circ C$. The temperature coefficients from table 3.1 have been looked up at Wikipedia[1]. There exist multiple scenarios in which a bridging fault might be interpreted as a short or a just as an additional resistance in a circuit. If there exists an additional unwanted resistive path between V_{dd} and V_{ss} or between any other supply voltage from the circuit to the reference potential, an additional current will be drawn, which may cause the device to heat up and probably change its fault model. If the bridging fault is located at a clock buffer, it is possible to cause timing variations $\tau = RC = L/R$ in the circuit which might even cause the device to fail in operation. During basic continuity or leakage measurements, bridging faults are very likely to be detected due to the increased current consumption or the dependence on temperature. A continuity test is used to check the proper contact to the DUT and additionally the protective circuit on the input,- or output pin if available. For this reason the supply pins V_{dd} and V_{ss} are fixed to GND while either the voltage is

[1] `http://de.wikipedia.org/wiki/Temperaturkoeffizient` from 11/3/2014

sweeped from $-V_{dd} \leq V_{pin} \leq V_{dd}$ or a constant current with $I = \pm I_{cont}$ is sinked at the observed pin. If the pin is shorted to V_{ss} or V_{dd} no voltage drop will be measurable according to the used bias direction, whereas at an open contact, the measured voltage will reach its maximum level. As the protective circuit of an in,- or output pin can be interpreted as a simple diode to V_{dd} or V_{ss}, also the diode characteristics can be monitored at the same time if no open or short is present.

3.1.4 Functional Behavioral Faults

As the name indicates, *Function Behavioral Faults* represent a huge variety of possible defects in IC production. They all have in common that their occurrence depends on analog parameters just as voltage, load (current), frequency, temperature and light or even test patterns. A specific operating condition will cause an error which might only be activated during the application of a specific logic input configuration resulting from a test pattern or due to a specific operating state. This behavior is summarized within the so called *soft defects* as Burmer, Brillert, and Qian, 2007 and Jr., 2011 point out in their work. They state that the physical reason can either be:

- leakage currents
- gate oxide defects
- shifted transistor parameters
- timing marginalities
- increased resistances in contacts, vias or signal lines

Due to the huge variety of *soft defects* they are very hard to cope with because a typical pass/fail behavior can depend on several parameters. Even self heating of the device can contribute to change the output behavior. Another typical error resulting from a soft defect originates from the *Seebeck effect*, see *Principles of Electronic Materials and Devices* from Kasap, 2006 for further reading. When two different metals or semiconductors of different temperature are in direct contact with each other, it is possible that their difference in *Seebeck-Potential* causes a *Seebeck-Voltage* which occurs as an additional voltage source in the circuit and is able to change the devices state. The interconnection between tungsten and poly-silicon is one of the highest possible Seebeck voltage sources in an integrated circuit.

Material	Seebeck coefficient $\mu V/K$
Silicon	435
Germanium	325
Gold, Silver, Copper	1.5
Tungsten	2.5
Aluminium	−1.5

Table 3.2: Seebeck Coefficients for Different Materials

The Seebeck voltage can be calculated with the following equation

$$\Delta U = (S_1 - S_2)\Delta T \tag{3.4}$$

where

ΔU: denotes the Seebeck voltage
S_i: represents the Seebeck coefficient of the materials
ΔT: is the Temperature difference between the materials

and the use of the coefficients shown in table 3.2 which have been looked up at Wikipedia[2] and crosschecked with Kasap, 2006.

Soft defects are going to be one of the main focus points in this work as they represent a category which are sensitive to temperature influence and therefore most likely to be detected with *DALS*.

3.1.5 Delay Faults

Each logic gate in an integrated circuit has it's own time delay. As an example figure 3.4 is showing the basic operating principle of a simple inverter. Time delay will be caused by the parasitic capacitances at the input and output of the inverter and the known issue that the channels in the p- and n-MOS transistors won't be built up or broken down instantly, because of the limited charge travel velocity linked with the resistivity of the diffusion channels. Additional defects might not cause a direct malfunction of the presented inverter, but alternate the time delay of the gate.

[2] `http://en.wikipedia.org/wiki/Seebeck_coefficient` from 11/3/2014

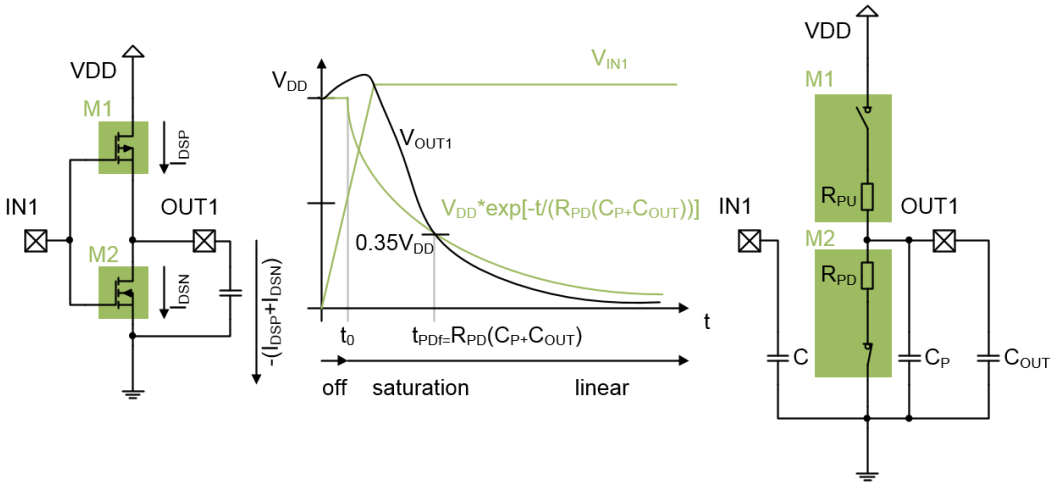

Figure 3.4: Time Delay at an Inverter

As every integrated circuit has a much deeper logic depth than the presented inverter and is operating at a specific clock rate, time delay faults of single gates can sum up and cause a malfunction of the device in total. Also adding probe pads for the input or output of specific gates can cause the presented errors because each additional constructed pad is supposed to have a capacitance of $C \approx 50\,pF$ or more regarding how and where the probe pad was set up. Also probing itself and measuring the time delay with an oscilloscope will cause an alternation of the gate's behavior because almost no measurement can be made reaction less. Time delay faults are therefore very hard to cope with and are most probably detected by the use of scan chains in combination with function based tests and other methods out of design for testability.

3.1.6 Redundant Faults

Defects might also be represented due to multiple fault models. A weak bridging fault can have the same behavior as an open contact fault, or a heavy bridging fault might equal a short. For stuck at faults it is also possible to originate from different device logics, as it can be seen in figure 3.5. Despite the fact that a stuck at one fault is present on the input of the *NAND*-gate of the circuit presented on the left hand side of the figure, the logic function will not be changed.

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

Table 3.3: Redundant Fault - Karnaugh Diagram

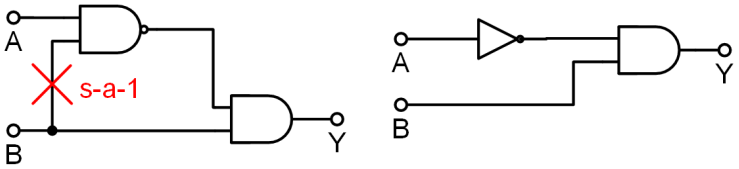

Figure 3.5: Redundant Fault Example

Furthermore the same circuit can be synthesized to the circuit presented on the right hand side of the same figure. For this reason a simple *Karnaugh* diagram presented in table 3.3 shows the intended circuit logic function which makes the behavior quite obvious. This simple example is demonstrating that the error at the output of a functional area must not necessarily directly correlate with a chosen fault model. We will have to introduce another analysis process which creates the ability for suitable defect localization.

3.1.7 Intermittent Faults

Intermittent Faults are very hard to characterize as they occur almost every time in an unpredictable pattern and only if specific circumstances are met. They clearly have to be differentiated between functional behavioral faults since they also can have some kind of reset mechanism of the error during their occurrence. This faults form some kind of unknown and unpredictable behavior and have been under investigation by Contant, Lafortune, and Teneketzis, 2004. They present in their work a methodology to describe the behavior of intermittent faults by the creation of four different events.

By combination of these events which include cite:

- the certainty that a fault is present at a specific state
- the certainty that a fault is absent after a reset event
- the probability that a fault is present after several cycles after his first occurrence
- the probability of how often a fault has been reseted in successively cycles

they form evolution diagrams which present the probabilities of all possible event paths. In IC production this behavioral model might seem a bit to complicated at the first glance but in reality they were able to create quite useful outputs due to the use of statistical methods.

3.1.8 Initialization Faults

Testing devices is often a highly time demanding task and the factor of time is directly linked to the factor of costs in IC production. In order to decrease test costs, test time is a valuable factor which is optimized to a very high level. This optimization might lead to an unwanted faulty initialization state of the DUT resulting from an unnoticed or underrated settling time of a signal. This simple initialization fault principle can be also met by certain faults at the input pins of a functional area of the device under test as it is shown in figure 3.6. Let's assume, the main task is to reset the output of the given circuit to zero. For this reason the input A will have to be set to *HIGH* as it is shown in table 3.4. If the input A is set to be stuck at zero due to a possible defect, the output Y won't be set to zero and will therefore lack an initialization fault.

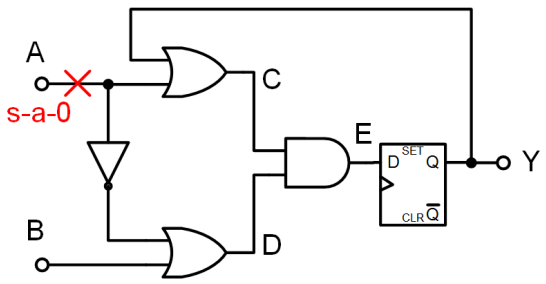

Figure 3.6: Initialization Fault Example

A	B	C	D	E	Yi-1	Y
set to zero						
1	0	1	0	0	0	0
1	0	1	0	0	1	0
set to one						
1	1	1	1	1	0	1
1	1	1	1	1	1	1
initialization fault						
0	0	0	1	0	0	0
0	1	0	1	0	0	0
0	0	1	1	1	1	1
0	1	1	1	1	1	1

Table 3.4: Initialization Fault - Karnaugh Diagram

The same result can be observed in table 3.4. Initialization faults are often an underestimated source of errors and lead to a very time consuming failure analysis. Resistive, capacitive as well as inductive loading is a heavily underestimated error source in failure analysis. During the experiments of this thesis, very basic faults in the lab setup lead to false failure predictions. Oscilloscopes, voltmeters, ammeters and other laboratory equipment (wiring) which are used to monitor the inputs and outputs of an IC don't have ideal characteristics in terms of their desired impedance. This can lead to an unwanted load of the device and therefore into an alteration of the operating condition. For high accuracy measurements it is therefore mandatory to known the load behavior of the port, gate or signal line.

3.1.9 Defect Preparation

Most of the time defects are not directly observable by monitoring the output of specific gates or signal lines. The error caused by the defect will rather shift through the logic of the device until they cause an observable malfunction. As scan design and scan patterns are a highly effective combination in design for testability, it is possible that a pattern fault will not directly reveal the malicious gate. Even the todays simulation tools from the known schematic and design editors are limited in their function as

they cannot predict real production variations of a device. For this reason it is common practice to artificially insert defects into fully functioning devices and observe afterwards the implanted errors. The most used tool for such alterations is a *Focused Ion Beam system* or short *FIB*. A FIB system combines the abilities of both imaging and material deposition or removal. *Focused Ion Beam Systems: Basics and Applications* from Yao, 2007 gives a great overview about the field of application as well as the capabilities of a FIB system. The basic schematic from figure 3.7 gives an easy overview of the components of a FIB. It basically consists of an ion and an electron beam source. The beams are furthermore focused and aligned due to apertures and an electric field which also causes the acceleration of the particles. As

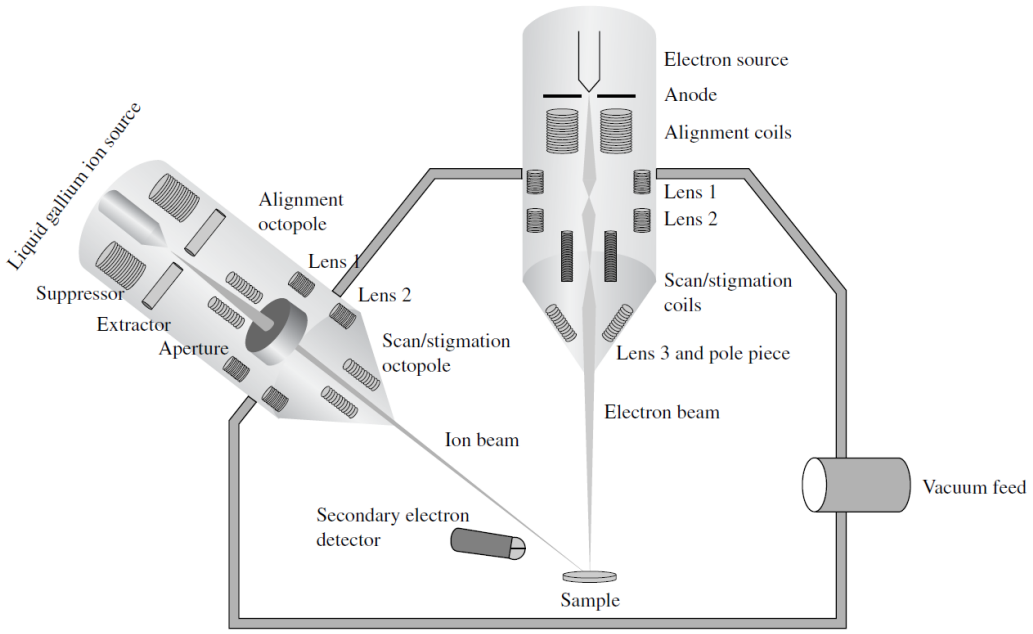

Figure 3.7: Focused Ion Beam Schematic Diagram from Yao, 2007

the energy of a particle is linked to its velocity and its relative mass by equation 2.7 the velocity and the mass will mainly influence the interaction with the focused material. By proper adjustment of the acceleration voltage, ion source, ion dosage, beam width and dwell time, particles can either be placed or removed from the focused material.

Figure 3.8 is showing an example for particle deposition and removal at a sample structure. The possibilities for device preparations are sheer infinite

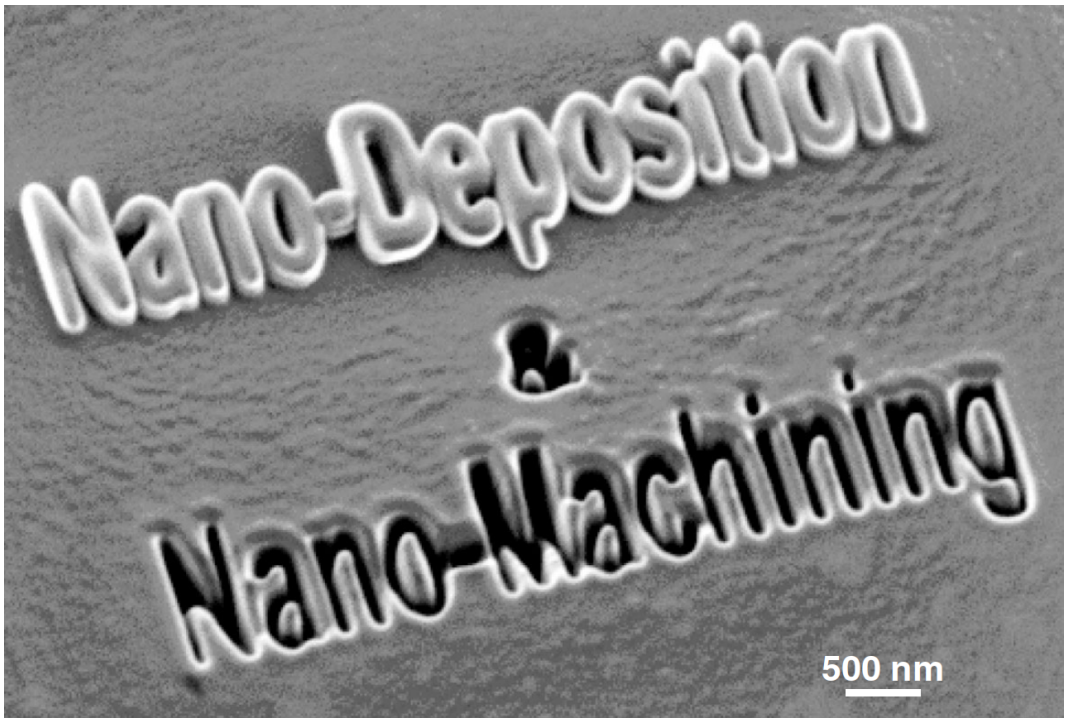

Figure 3.8: Focused Ion Beam Sample from Yao, 2007

because of the ion beam parameters, so the following examples are just suggestions for FIB applications.

- Open Defect
  By proper adjustment of the penetration depth and beam width it is possible to create open contacts of signal lines at a given layer of the integrated circuit. The easiest defect locations in terms of FIB are always the top layers of the device. The closer the open contact has to be placed to the substrate the more additional defects can be caused during the preparation. As all the preparations are made in a vacuum chamber the contacts at the open defect will instantly oxidize in the presence of air. The outcome of the open defect preparation from a FIB is quite unpredictable, because the indirect created oxide will make a clear difference to an open defect which originates in the production.

Additionally the potential of the open contacts is not directly defined without further material decomposition with the use of FIB and might lead to a floating contact. Artificially created open defects must be treated therefore with caution as no reproducible output can be ensured without further actions. Another application of particle removal could be to just slightly cut off a part from a signal line in order to decrease the size of the contacts cross sectional area. This manipulation would lead to an increase of contact resistance which can be verified much easier and prematurely in design simulators.

- Bridging Defect
  Just as it is possible to remove particles from a device structure it is also possible to decompose material on a desired device layer. With controlled deposition of particles there exist numerous ways of creating additional signal paths after production. The conducting resistance can be adjusted by controlling the dimensions of the deposited material as well as the chosen atoms for depositing. Deposition of material is not to be said a non destructive way of device manipulation because the particles have to be accelerated and are therefore colliding with the top particles of the device layer. Depending on the impact of the particles on the surface, atom displacements in the layer as well as micro cracks can be a result of the preparation. A further use of particle placement is the creation of probe pads for signal probing.

In the experiment chapter, preparations for artificial defect generation and it's result from an originally good device are going to be presented.

The literature research as well as the experience during DALS analysis have not revealed if the majority of defects is originating either from bridging or open defects. Moreover the impact of the defects on the IC's functionality are dependent of multiple factors whereby the severity of a comparable defect can alter from device to device.

The next sections will discuss the most used applications, techniques and effort in failure analysis and defect localization.

3.2 Beam Based Defect Localization

Defect Localization is always depending on the monitoring of a device's response at given supply parameters while it gets stimulated by an external light source. There exist two different device states for Beam Based Defect Localization. In the static domain the device remains in a defined state up until it gets affected by an external light source. In the dynamic domain the devices response due to the application of a specific input pattern, an alternating signal or an IC direct command is monitored and compared to the response while the device gets stimulated by an external light source. If any of the observed parameters is changing its state due to the influence of the light source and causes a transition from a passing to a failing parameter or vice versa the main purpose of this technique has been achieved. In each case, analog parameters just as

- Voltage
- Current
- Frequency
- Timing

or digital parameters

- Signal Amplitude (Low/High)
- Frequency
- Timing
- Duty Cycle

are monitored throughout the stimulation of the device and at the same time are being compared to the expected values of the device. Beam Based Defect Localization - BBDL techniques are now making use of the dependency of the presented parameters due to the influence of a external light source. By adjusting the wavelength of the light source there emerge two main techniques which are referred to thermal or electrical influences. "Beam-Based Defect Localization Techniques" from Jr., 2011 is giving a great overview of the existing BBDL techniques in a very compact form. Figure 3.9 is showing a basic setup for beam based defect localization. It mainly consists of a laser scanning unit, a prober or a device socket, a signal amplifier and an image processing unit. The laser beam is is positioned by the scanning unit across the DUT due the mechanical orientation of a mirror, an aperture unit and a lens. The DUT is either mounted on a Test PCB or contacted via a prober to give access to the necessary pins for observation purposes.

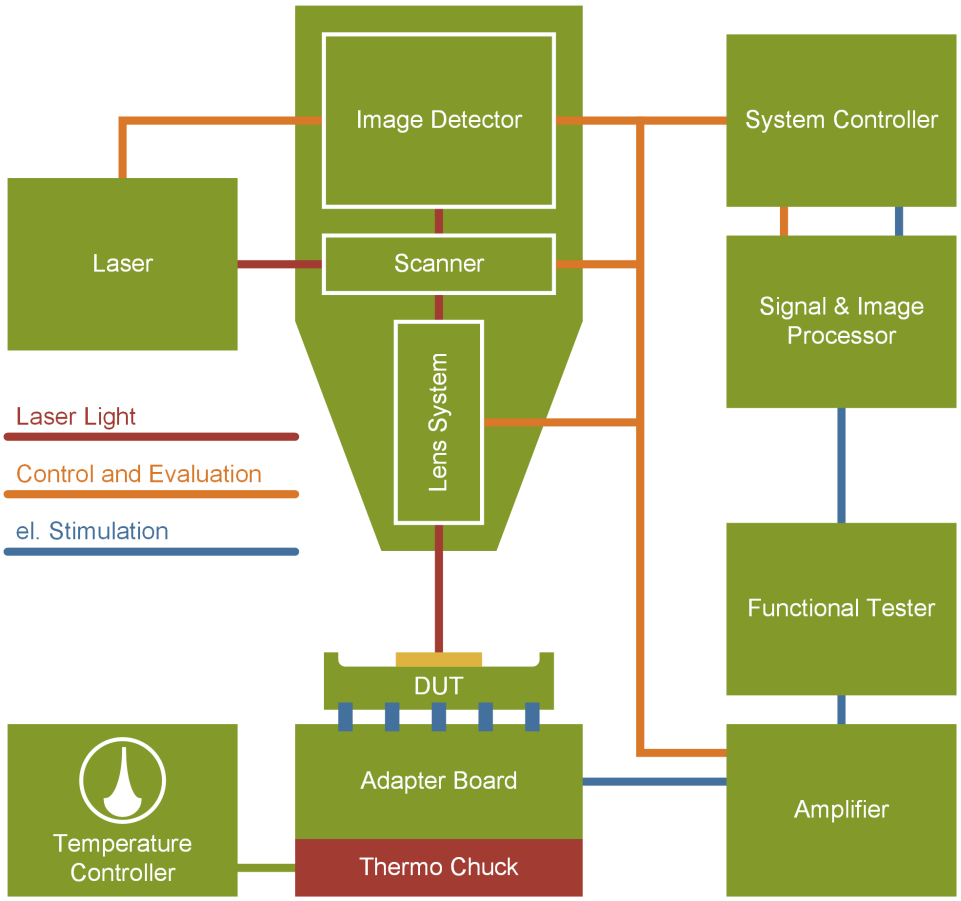

Figure 3.9: Beam Based Defect Localization Setup

The device can be powered externally or some signal amplifiers also serve the purpose of supplying the DUT directly as it is the case for the *Hamamatsu Phemos 1000* system. The used amplifier is always constructed to have a high gain, low noise as well as both the ability for constant current or voltage biasing in order to detect even the slightest change in an output parameter. The reflected light from the laser scanning process passes the same lens as the original stimulation laser beam. This preconditioned beam is afterwards converted into a picture by a CMOS sensor and the attached image processing unit. As the actual location of the laser beam is known at each time of a scan process, the collected information about possible parameter variations from the amplifier can be added to the reflected light image. All described components are placed in a closed chamber which aims to minimize external influences like light, electromagnetic fields as well

as ambient temperature. The literature research revealed that a huge effort has already been made to define the most influencing parameters for BBDL systems. The related works of Wu et al., 2011, Li and Wu, 2012, Chunlei, L. Zhai, Motohiko, Ma, et al., 2010, Phang et al., 2004, Liao et al., 2005 and Chunlei, L. Zhai, Motohiko, Liu, et al., 2009 have all in common, that the results of the laser scanning unit are mainly dependent of the following parameters:

- Wavelength
  As it already has been described, the desired stimulation effects heavily depend on the chosen wavelength of the light source. For thermal activation wavelengths around $\lambda = 1300\,nm$ have shown the best results, as the energy of a photon will not be sufficient to excite an electron in the silicon. Lewis, Pouget, F. Beaudoin, Beauchene, et al., 2004 have described, that for the generation of free electron hole pairs wavelengths around $\lambda = 800\,nm$ are the most effective ones. Other researches have shown, that even with lower wavelengths thermal stimulation of the desired materials can be achieved. Nikawa and Inoue, 1996 are reporting that the total energy conversion rates for $\lambda = 633\,nm$ and $\lambda = 1300\,nm$ wavelength lasers to thermal energy are nearly the same, but $\lambda = 633\,nm$ lasers are also creating electron hole pairs in the stimulated crystal at the same time.
- Laser Power
  Literature research has shown that there is no clear correlation between the used laser power and the effectiveness of defect stimulation. No recipe for which laser power has to be used for what kind of defect is available nowadays. There exist failure modes which are only stimulated at low laser powers and others which are stimulated at the maximum ratings. Therefore it is mandatory that each scan is carried out at least under two different laser powers. Accordingly to the results of Phang et al., 2004, higher laser powers are needed if the failure analysis is carried out at low magnification levels. The lower the magnification levels are, the bigger the spot sizes and the observed areas will be. Sanchez, R. Desplats, et al., 2006 note in their report, that during thermal stimulation of a DUT the maximum temperature due to the stimulation is directly linked to the available laser power. The higher the laser power is, the higher the temperature difference will be during stimulation.

Firiti, Lewis, et al., 2003 describe that the achievable temperature gain of a metal conductor in a silicon crystal is about

$$\Delta T = 0.55 \frac{^{\circ}C}{mW} \tag{3.5}$$

whereas the hottest temperature will occur directly at the laser spot center and the thermal spreading is limited to a region of about $r = 30\,\mu m$ around the beam spot. If the available laser power is not sufficient to stimulate the defect an additional heat source can be used to heat up the device preliminary. The heat source can be either a hand held heat gun or a thermo chuck but it definitely has to fit into the cabinet of the laser unit. Li and Wu, 2012 even used the ESD protection circuit for self heating of the DUT. They forced a current of $I = 150\,mA$ into the ESD protection unit which caused the device to heat up. By the use of this heat source they were able to preheat the device and furthermore cause a pass to fail transition of an output signal.

- Spot Size
  The spot size directly limits the spatial extension of stimulation and determines the precision of the defect localization. Small spot sizes in combination with a high precision positioning system result in a highly accurate failure localization. Unfortunately the spot size is influenced due to multiple factors of a BBDL system. Apertures in the beam path lead to diffraction which causes the spot size to increase while the use of magnification lenses will cause the beam spot to narrow if the magnification is increased. There exist special lenses for infrared and ultraviolet applications which allow the spot size to be reduced to a minimum. A good rule of thumb is, that the smallest achievable spot size is about half of the used wavelength. Phang et al., 2004 have reported, that after some modifications of the beam path of an infrared light laser source at $\lambda = 1340\,nm$ they could achieve a spot diameter of $d = 750\,nm$.
- Magnification Lens
  Modern manufacturing processes are using an integration size much smaller than $1\,\mu m$ whereby it is sheer impossible to detect a logic cell with the naked eye. For this reason magnification lenses are used to optically enlarge the spot of interest. By the use of high precision lenses which have to be built accordingly to their field of use regarding the used wavelength of the light source, optical defect localization has become much easier. With increasing magnification the spot size of a focused laser light source is decreasing which is a highly desired effect

in failure analysis as the highest optical detail at the lowest failure rate can be achieved. Unfortunately high magnification rates comes at a very high price. As the width of the used objective is spatially limited, multiple lenses in an objective are used to reach the desired magnification level. As each of the lenses in the objective has its own transmission and reflection rate, the intensity of a passing light ray will be decreased by the amount of lenses in the objective. In BBDL systems this means, that the output power of the laser is further decreased by the use of any magnification unit. For this reason most BBDL systems allow not only optical but also digital magnification. The collected data of the image sensor is then computer assisted enhanced due to pixel interpolation and other image editing techniques.

- Scanning Direction
  Depending on the positioning of the laser beam it is easy to differentiate between two scanning directions for a simple metal conductor. The first direction is in parallel and the other is perpendicular to the observed structure. For parallel scanning techniques thermal equilibrium will be reached faster as as for perpendicular scanning techniques. Most of the time the layout of the observed structure is unknown which leads to the fact, that the observed structure has to be scanned at least in two different directions. This alteration in the scanning direction will lead to different results in the failure analysis like Brahma, 2008 and Arkadiusz Glowacki, 2010 have both shown in their dissertations.
- Pixel Dwell Time
  Lewis, Pouget, F. Beaudoin, Haller, et al., 2005 and Chunlei, L. Zhai, Motohiko, Liu, et al., 2009 have shown in their works that thermal equilibrium due to thermal stimulation is reached within $t \leq 50\,\mu s$ or less regarding the metal density in the layer of the observed IC. As the spot diameter of a laser beam is most of the time well known due to the optical system configuration, a dwell time of $t = 50\,\mu s$ has shown to be a good choice for reaching thermal equilibrium. The influence of photo-electrical stimulation can be monitored almost instantly which allows the pixel dwell time to be reduced to a much lower level than for thermal stimulation. Experiments have shown, that depending on the circuit design properties and the resulting time constants, a settled influence can be measured within $t \leq 10\,\mu s$. Depending on the optical resolution of the image sensor the pixel dwell time multiplied by the amount of pixels will result in the total scan time of the system.

A configuration of a $1024x1024\,px$ image sensor and a pixel dwell time of $t_{single} = 50\,\mu s$ will lead to a total scan time of $t_{total} \simeq 53\,s$. To decrease possible measurement failures, it is most common to carry out multiple scans with the same settings and to combine the measurement results to the final outcome which can lead very quickly to a time consuming task

In the following section the basic BBDL techniques will be introduced and compared to each other.

3.2.1 Static Thermal BBDL

As it already has been discussed in earlier chapters, the energy of a photon is dependent of the wavelength of the used light. If the energy is lower than the band gap energy, then the stimulation will be of thermal nature. For this reason a laser at around $\lambda = 1300\,nm$ wavelength is used. Thermal stimulation is mainly affecting the resistive behavior of a material which can be monitored due to the current consumption or the resulting voltage drop across a given resistance. Depending on the temperature coefficient, thermal stimulation leads to an increase for positive and a decrease of the resistance for negative temperature coefficients. This can lead to a shift in the threshold voltage of a device due to the increased availability of free charge carriers in doped semiconductors. Static Thermal BBDL is referring to a thermal stimulation technique at which the state of the device is settled and not alternated by any factor except the thermal influence of the laser.

OBIRCH - Optical Beam Induced Resistance Change

OBIRCH is probably the most common Beam Based Defect Localization technique. The device is supplied by a low noise constant voltage supply in a static working condition while the devices current consumption is monitored. The laser is placed across the device by the laser scan unit which causes the device to locally heat up. If the laser beam is focused on a pure silicon structure, no heat will be absorbed because silicon is nearly transparent for infrared light. Otherwise, if the laser beam is focused on a metal line or a heavily doped region, heat will be locally absorbed in the affected structure at the first place. The induced heat will then cause neighboring structures to heat up. For this reason front side and back side

analysis of the device can be done very easily because most of the time only the metal layers in an integrated circuit will cause heat absorption. The comparison between the results of front side and back side analysis has been a task in many related works just as those from Phang et al., 2004, Lewis, Pouget, F. Beaudoin, Beauchene, et al., 2004 and A.M. Glowacki et al., 2007. They have shown that the results are most of the time the same for both observation directions. The application of the used technique is simply dependent on the layout structure, as for instance a redistribution layer can definitely alter the results for back side analysis or if the device is a light driven sensor which has an active region at the top layer. For this reason it can be necessary that the the DUT has to be prepared for any ongoing analysis by chemical or mechanical layer removal. Anyway, if an alteration of the current consumption can be detected by a low noise and high gain amplifier, the affected spot is very well known due to the position of the laser. The control unit furthermore colors the pixel of the image accordingly to the increase or decrease of the current consumption. By overlapping the information of all stimulation results of the laser and a normal image the failure spots are clearly observable as it is shown in figure 3.10. Basically the red colored spots mark areas where the current consumption increased, whereas the green colored spots indicate a decrease in current consumption. As the locally installed high gain amplifier in the LSM is AC-coupled, the red marked spot will most likely be an artifact from the intensity evaluation just as Quah et al., 2006 have described in "DC-Coupled Laser Induced Detection System for Fault Localization in Microelectronic Failure Analysis." Such artifacts are quite common for BBDL failure analysis techniques and can often mask the real defect spot. A solution to this problem would be to alternate bandwidth of the high gain amplifier, or to change the coupling principle. In the shown example the device damage was caused due to electrical over stress. OBIRCH can be used to detect open, bridging and short defects. The effectiveness of detection is mainly depending on the spot size and the power of the laser. As Li and Wu, 2012 have shown in their work, higher optical resolution and laser power lead to better results. Nikawa and Inoue, 1997 present that the main improvement in their setup was increasing the laser power from $P_{total} = 50\,mW$ to $P_{total} = 500\,mW$ by the use of a YLF-laser. F. Beaudoin et al., 2009 are describing that the influence of noise on OBIRCH measurements. Devices with high resistance defects should be powered with a voltage source where the current will be monitored. Low resistance faults at metallic lines or vias are better observable by the use of a current supply whereas the voltage will be monitored.

This alteration in current biasing would lead to another BBDL technique as we will see later on, but as most common amplifiers are capable of current as well as voltage biasing it is an easy to do task.

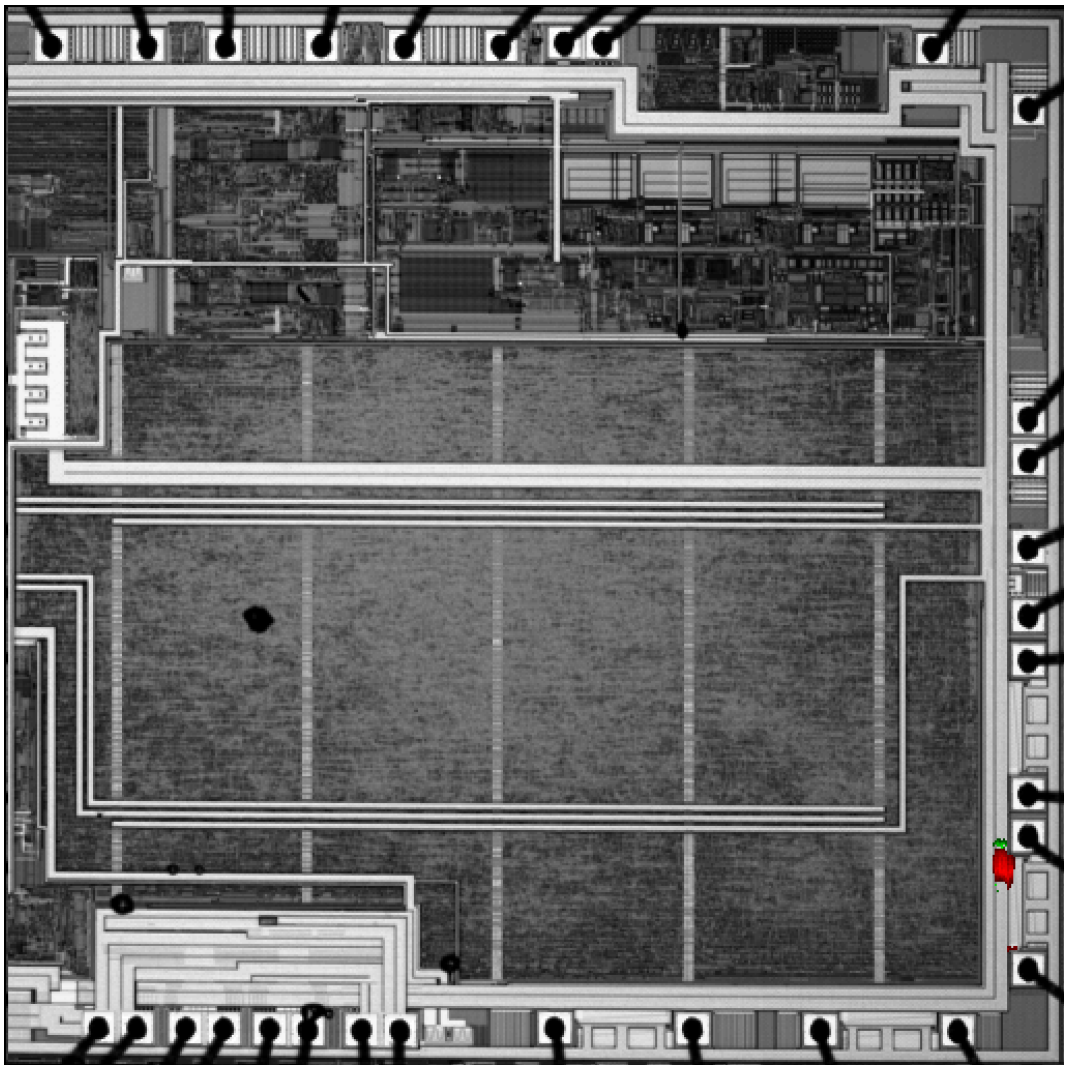

Figure 3.10: OBRICH Example ©ams AG

TIVA - Temperature Induced Voltage Alteration

TIVA represents another contact less stimulation technique in failure analysis which is based on the thermal stimulation with an infra red laser. It differentiates from OBIRCH in a way that a constant current bias is used to supply the device and the resulting voltage drop across the device is measured. By using this technique it is mandatory to implement a voltage compliance limit in order to avoid any damage during the analysis itself. As ammeters are converting the current to be measured by a shunt into a representative voltage anyway, the observation of a change in the voltage with a voltmeter is much exacter. Also voltmeters have a much lower input impedance than ammeters, therefore the measurement noise will be much less. As Quah et al., 2006 have shown in their work, TIVA is a much more sensible measurement technique than OBIRCH. TIVA is used just as OBIRCH for the detection of open, shorts and bridging faults. The best analysis results are again mainly affected by the spot size and the power of the laser. The higher the laser power, the bigger the temperature gradient in the device and therefore the shift in the measurement signal will be.

SEI - Seebeck Effect Imaging

Just as the name is already indicating the influence of the Seebeck effect is monitored by this failure localization technique. In direct comparison to OBIRCH and TIVA, no bias is used for this technique at all in the standard configuration. The main goal is to monitor just the potential gradient caused by the Seebeck effect. The stimulation and measurement setup is the same however as for any other thermal BBDL technique. Both Nordin, 2012 and A. Glowacki and Boit, 2005 have effectively shown the results of a SEI signal which were caused by a defective via. What all SEI signals have in common is, that they show opposite polarity signals depending on the scanning direction of the laser in a small region around the defect location. As the Seebeck potential is dependent on the thermal activity of a material, the thermal activation of the interconnecting materials is mainly influencing the quality of this analysis. If a single side of the Seebeck interconnection can be heated, the highest Seebeck potential can be detected. As Li, Linda Zhai, et al., 2011 and Firiti, Haller, et al., 2004 are reporting in their research, heavily doped regions such as source and drain, poly silicon gates, interconnections between tungsten and polysilicon, buried layers and interconnections of resisitve vias have the highest potential to lead to a SEI signal. SEI is

therefore mainly used to detect material discontinuities which include open conductor defects. As the resulting Seebeck potential due to thermal stimulation is in the best case around a few millivolts, measurement noise has to be avoided under each circumstances. Furthermore the signal quality is again heavily dependent of the spot size, the power and the scanning direction of the laser. In derogation to the standard configuration of SEI with no biasing, Félix Beaudoin, Romain Desplats, and Philippe Perdu, 2002 are presenting in "Thermal Laser Simulation for Direct Localization of Defects in Integrated Circuits" the results of SEI while the used sample was operated in the saturation regime at constant voltage biasing. Due to the local difference of potential resulting from the Seebeck effect they were able to pinpoint the defect spot by the typical polarity property of an Seebeck interconnection. The shown BBDL result from figure 3.10 is an exact match for the introduced analysis. Seebeck effects are often covered due to the deep integration depth of modern ICs and are therefore much harder to detect than other defects. As the optical resolution of a BBDL system is also limited, it is highly unlikely to detect a defective via for instance with the use of a $100x$ magnification objective. This is also the most common known drawback of commercially available BBDL systems.

3.2.2 Dynamic Thermal BBDL

In the dynamic domain of device stimulation the response of the device, whilst thermally stimulated with an infrared laser, is compared to the expected outcome for the chosen stimulation. If there is a difference between the observed and the expected output, the possible defect location is known due to the focus point of the laser. This analysis method gives rise to the robustness validation of design and layout of an integrated circuit. The device must not basically fail in operation while thermally stimulated, but if the device reveals a dependency on an external parameter just as temperature, a possible weakness of the device may be revealed.

Basically each device can be divided into two regions:

- the digital domain with clear defined states (low, tri-state, high) for each gate and
- the analog domain with multiple output states in each of its cells

The digital domain can be controlled with a functional tester by the use of scan chains which is a very common design for testability action. The analog domain allows many possible output states, so it is very common to check the output with a special evaluation board or an oscilloscope. There exist several parameters which can cause an analog circuit to fail which have been described at the very beginning of this chapter 3.2.

DALS - Dynamic Analysis By Laser Stimulation

Stimulation, observation and detection of soft defects like resistive vias, leaky gate oxides, process variations or timing marginalities can be a very hard to do task, as they can depend on several properties like

- Supply Voltage
- Clock Frequency
- Temperature
- Ambient Light

Often the errors are just caused in between a certain range and combination of the above mentioned parameters or by the application of special input sequences. It is therefore mandatory to check the devices functionality over the whole range of available parameters. The main goal of this analysis technique is again to detect the transition levels between the pass-to-fail or fail-to-pass events. In order to keep track of all the stimulation results it is most common to use *Shmoo plots* to indicate this dependency and transition events. Basically the same setup as for other thermal BBDL techniques is used, except that the signal validation is carried out in an external measurement unit. The external measurement unit may consist of an oscilloscope in combination with an alternating waveform generator or a functional ATPG tester. It is mandatory to synchronize the laser scanning unit with the external measurement tool. The length of a single input cycle or pattern will define the dwell time of a single pixel for the laser scan as it is desired to record and compare at least one full stimulation cycle of each available pixel. Soft defect localization has been covered in many publications. Chunlei, L. Zhai, Motohiko, Ma, et al., 2010 are reporting that a long pixel dwell

time in combination with a short test sequence, high laser power and high magnification rate is the most probable combination to reveal soft defects. Phang et al., 2004 show in their thesis "A Review of Laser Induced Techniques for Microelectronic Failure Analysis" that at a magnification of $100x$, a laser power of at least $P = 30\,mW$ at the defect spot is necessary for device stimulation. Without using a special infrared laser setup, because most high power lasers are often more expensive, pulsed laser testing can increase the induced energy densities as Lewis, Pouget, F. Beaudoin, P. Perdu, et al., 2001 are reporting in their work. A pulsed laser can easily be created by the insertion of a *Pockels Cell* or *Kerr Cell* into the beam path as Deyine et al., 2009 are mentioning. The biggest DALS signals are expected to appear for stimulations of transistor channels as they are most sensitive to temperature alterations as A.M. Glowacki et al., 2007 are presenting in their paper. Sienkiewicz et al., 2008 even say: *"Comparing PNP and NPN structures we observe, that as a function of the input voltage, PNP structures have a higher sensitivity to global temperature changes. Moreover, this sensitivity is independent on emitter dimensions in bipolar designs."* Modern oscilloscopes have the ability to set up customizable trigger events which give rise to the monitoring of multiple analog parameters as voltage, frequency or timing events. Wu et al., 2011, Li and Wu, 2012 and Li, L. Zhai, et al., 2011 use a standard BBDL system with basic OBIRCH functionality. By the extension of the measurement system with an oscilloscope they could map several analog parameters. They connected the trigger output of the oscilloscope directly to the output of the OBIRCH amplifier and used the trigger output as a current sink. This setup was setup in a way to work with the standard TTL-levels from the trigger output of the oscilloscope. Whenever the trigger event was active, they marked the failing scan cell indirectly by the alteration of the current from the amplifier. This is quite an easy to do task and is used in many failure analysis laboratories since it provides an additional analysis method and avoids the purchase of expensive synchronization equipment. It is also possible to draw the additional current by the use of a simple transistor which is connected to the output of the amplifier. The transistor is switched on and off accordingly to the evaluation result of the external measurement unit. An example for a possible trigger event is shown in figure 3.11.

Figure 3.11: DALS Trigger Event Example from Li, L. Zhai, et al., 2011

The failing signal can be detected by the voltage amplitude or by timing parameters as there occurs a glitch between the signal transition from the high to the low amplitude level. This example should present how easy it is to monitor an undesired signal event, but predicting and detecting such an event at a signal node in the first place is a much harder to do task. Therefore close cooperation between the designer of the device and the defect analyst is mandatory to point out possible weaknesses.

xVM - Analog Parameter Variation Mapping

Modern technology of integrated circuits have led to the development of very powerful failure analysis tools which are highly sophisticated and create the ability to map several parameters at the same time. Another expression for this ability is *concurrent testing* which also leads to the suppression of *sinc*-modulations which are known to occur from the determination of resistances. As there exists a vast amount of analog parameters (therefore the *x* in the abbreviation of the analysis techniques name), the newest development in failure analysis is to build a parameter map for all available parameters over the whole device. The resulting parameter maps must not necessarily include a failing parameter, but even slight shifts can lead to an undesired and unintended signal state. The maps are again a result of thermal stimulation of a device due to the influence of an infrared laser. Sanchez, P. Perdu, and F. Beaudoin, 2007 and P. Perdu, 2009 are showing the possibilities which arise from this analysis technique. The overlay of the recorded data to the 2D image of the device, lead to a multi

dimensional map of analog parameters. There are also many possibilities of how the collected data can be interpreted as the parameter maps must not be the same for the shut on versus the shut off sequence, or the static operating condition versus dynamic operating condition. One approach

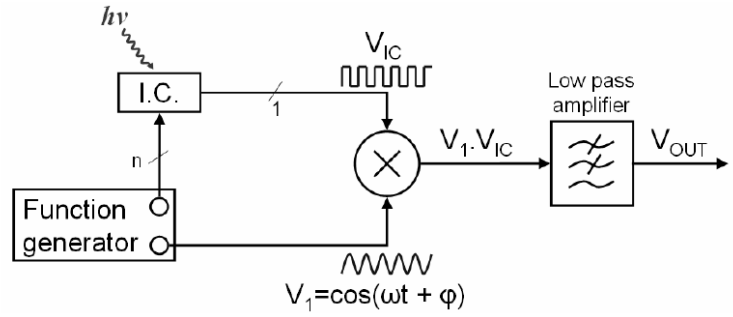

Figure 3.12: xVM Evaluation Circuit from Sanchez, P. Perdu, and F. Beaudoin, 2007

of data interpretation is that even the slightest change of timing signals can reveal instable regions. For this purpose even changes in the *picosecond* regime need to be detected by the measurement unit. It is also common practice to correlate the stimulation result with the input signal by the use of convolution. If the signals are showing even just a slight phase shift against each other, the convoluted signal will lead to a lower average amplitude which can be easily created by the use of a low pass filter as it can be seen in figure 3.12. xVM has emerged to be the most promising upcoming failure analysis technique and is under investigation by many researches.

3.2.3 Photo-Electrical BBDL

If the energy of a photon is higher than $E = 1.1\,eV$ electron hole pairs will be created in pure silicon. We can easy calculate the correlating wavelength for this band gap energy by the use of equation 2.3.

$$\lambda = \frac{hc}{Ee} = 1127\,nm$$

Lasers with wavelengths $\lambda \leq 1127\,nm$ will cause charge generation in silicon. If the electron hole pairs are created in a depletion region, the free charge will be instantly separated due to the built in voltage of the depletion region. By phonon assisted electron generation it is also possible for lasers

with wavelengths $\lambda > 1127\,nm$ to generate free electron hole pairs as A. Glowacki and Boit, 2005 are reporting and we have already introduced in this work. As phonon assisted electron generation will only occur for higher stimulation temperatures, this charge source will be neglected for Photo-Electrical BBDL. The technique also operates with the same setup than for thermal BBDL techniques. The absorption rate changes in a great extent since the fundamental absorption edge of silicon is located at around $\lambda = 1100\,nm$ as it can be seen in figure 2.4. For this reason it is mandatory to know that the electron hole generation will occur directly under the silicon surface which might give rise to the need of device preparation since the beam cannot pass through the device as in thermal stimulation. The device preparation might consist of mechanical grinding, chemical etching and polishing with the main goal of getting a thinner device and a smooth surface to avoid reflections and refraction. The method is mainly used to detect opens and leakage spots since the created charges can lead to the definition of the affected signal nodes.

EBIC - Electron Beam Induced Current

The main goal of EBIC is to identify defects in buried diffusions and silicon. In derogation to the introduced BBDL techniques the laser light source is exchanged for an electron beam source which is in many cases a thermionic cathode. The electrons are accelerated and focused by the use of an electrical field. If an accelerated electron hits the surface of a DUT, several electron hole pairs can be created depending on the initial kinetic energy of the electron. High energy electrons can cause lattice defects which may create the need of thermal healing after the device stimulation. A scanning electron microscope will detect the secondary electrons from the scattering interactions with the DUT and a current to voltage amplifier transforms the induced current with regards to its magnitude and direction. EBIC is most commonly in use as an unbiased technique although biased versions are available. A drawback of EBIC is definitely the limited penetration depth of the electrons and the accompanied crystal damage at higher energies.

OBIC - Optical Beam Induced Current

In contrast to EBIC, the Optical Beam Induced Current technique uses a laser light source at a wavelength $\lambda \leq 1127\,nm$. The main goal is to identify defects in buried diffusion regions, damaged junctions and gate oxide shorts. Nikawa and Inoue, 1996 report that OBIC signals are much stronger than OBIRCH signals although the change in the same parameter, the net current, is monitored by a sensitive amplifier. Unbiased versions of OBIC are used in cases where the additional current due to photoelectric stimulation is negligible small in comparison to the normal operating current. The most sensitive region for creating free electron hole pairs is the depletion region between highly p-, and n-doped silicon. As it was described in the introduction, the built in voltage of the semiconductor will lead into a separation of the created free charge, which alternates the net current of the device. Commercial available OBIC systems like the *Hamamatsu Phemos 1000* are available with the configuration of a IR-laser with a wavelength of $\lambda = 1064\,nm$. This creates the possibility to do backside analysis of a DUT as the absorption depth of silicon is still high for the used wavelength, but of course still lower than for thermal IR-laser stimulation.

CIVA - Charge-Induced Voltage Alteration Imaging

CIVA is mainly used to detect open defects in integrated circuits. As it will be presented in the experiments chapter, it is possible for devices to work with full functionality even if an open contact is present in the net of a device. The basic failure representation of an open defect is a capacitor. As the impedance of a capacitor is just low at high operating frequencies it would be expected that crosstalk only occurs within this configuration. In contrary to this known effect, quantum electron tunneling can be the source of significant crosstalk at low operating frequencies. Due to the tunneling effect which is heavily dependent of the properties of the open contact, like spacial the dimensions of the open, a significant amount of electrons can tunnel through the open contact and cause the open node to be defined within a specific settling time. It can be simulated, that open contacts have each a parallel capacitor to V_{DD} and V_{SS}. The loading of this parallel capacitors in combination with the capacitance of the open contact cause an additional load for the supply and lead to a defined time constant. The whole loading process is now monitored by CIVA. Again, by the creation of free electron-hole pairs due to the stimulation of a laser

with a wavelength $\lambda \leq 1127\,nm$ the net current will be influenced. If the charges are created in a fully functional region, the additional current will most probably not be noticeable because it will be in the range of some nano-amperes. If the laser is placed in the region with the open contact, the potential of the negative loaded node will be further decreased, which will cause an additional load for the supply. The time constant of the capacitive network will furthermore determine if this loading events can be detected by a measurement unit. For this reason it is mandatory to use an amplifier with high operating speed, high gain and low noise.

LIVA - Light Induced Voltage Alteration

The last introduced active Photo-Electric Beam Based Defect Localization technique is LIVA. In contrast to the other techniques described above, LIVA is biased with a constant current and a sensible voltage measurement unit detects even the slightest changes in the operating voltage. The scanning unit is again positioning the laser across the device. Due to locally generated free charges the potential in a signal node can be affected. This additional potential will cause a shift of the normally observed voltage. As the location of the beam is known by the settings of the scanning unit, the affected pixel of the device image will be marked according to the amplitude of the voltage change. The signal of LIVA will be maximal for defects in diffusion regions.

3.2.4 EMMI - Emission Microscopy

Emission Microscopy is a passive BBDL technique. This means that no laser is used for scanning and stimulation purposes of the DUT. Moreover emitted photons are detected by an image sensor which are created in the first place due to the recombination of free electron-hole pairs in the semiconductor. As the photons from the recombination process are emitted into several directions, high integration times are needed to effectively observe an emission hot spot because the photons need to pass through the used lens system in order to reach the image sensor. To furthermore reduce the background noise of the image sensor, which is in most cases a CMOS sensor, it is common to cool down the detection unit to a fixed temperature of about $T = -20\,^{\circ}C$. By the given description it is already clear that the introduced technique is used to detect abnormal leakage currents which can

be observed for instance at a defective inverter where both p-, and n-MOS transistors are switched on at the same time. A direct comparison between the results from thermal laser stimulation and emission microscopy for the given example lead to much weaker signal spots for EMMI. Emission Microscopy is furthermore heavily dependent of the used supply voltage and operating frequency of the device.

3.3 Non Beam Based Defect Localization

As BBDL techniques are highly sophisticated and directly linked with high investment costs, this chapter will address techniques which are using standard laboratory equipment. The defect localization will heavily depend on the analysts knowledge regarding the device design and behavior. Normally there are just a few probe pads realized on a device in the standard design if any are present. By making use of this probe pads, the potential of the signal lines can be observed by using a micro prober in combination with a reaction less measurement tool. An oscilloscope can be used if the probe has a high input resistance in combination with a low coupling capacity. Even active or differential probes can sometimes alter the measurement just by adding capacitive loading or inductive loading from the applied external wiring of the observed signal node. Furthermore it is also possible to define the signal nodes potential externally. This creates the possibility to power up just certain parts of the device. It is also common that the device can be forced into a certain state by applying a so called direct command. This direct command will cause the device to work for instance in a power down mode where only certain domains and gates are powered. Of course it is also possible to alternate the device layout again with a FIB (opens, bridging contacts, shorts). This examples already reveal that the failure analyst has to work in close cooperation with the designer of the device in order to work out a proper test routine for the device. The most basic analysis technique for non beam based defect localization is the optical inspection. Available optical microscopes allow a magnification higher than $200x$ which is a sufficient magnification level to observe via contacts. Via contacts are used for inter-metal connections between two different metal layers. By the use of an external light source it is also possible to make even the tiniest details visible for the human eye.

3.3.1 IDDQ - Quiescent Current Measurements

Monitoring the current consumption of a device is a very powerful tool because it can reveal a possible defect without much effort. The probability of detecting an abnormal current consumption is heavily dependent on the leakage current and the logic depth. With increasing logic depth it is possible that additional currents from defects can be masked and will only cause a change in the range of one percent. Furthermore it is possible that defects are only noticeable during a certain state of a gate. For this reason it is common practice to apply several test patterns to a device to change its state during testing. After the device occupies a quiescent state, the current consumption is monitored. This is the source for the naming of this technique: Quiescent Current Measurement. As Ferguson and Shen, 1988 are reporting in their paper, at least 72 % of all possible device defects can be detected with a proper IDDQ setup. Figure 3.13 is a very simple example for the dependency of an IDDQ monitor able defect. The source and gate

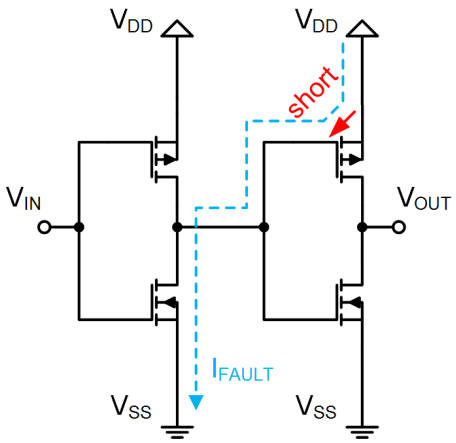

Figure 3.13: IDDQ Stimulation Example

contact of the second inverter are shorted which leads to an unchangeable output state where the p-MOS transistor will be always switched off and the n-MOS transistor will be always switched on. Therefore the output of the example circuit will always stay at 0 regardless the input state. If the supply current of the example current is measured, only leakage current would be expected. If the input of the circuit is set to 1 a direct path between V_{DD} and V_{SS} will be active where the current will only be limited due to the channel resistance of the n-MOS transistor of the first inverter. This state would lead

to an increase of current consumption which would then indicate a failure in the circuit. The pros and cons of this technique are very easy to identify

- very simple test method
- it can be linked with functional test patterns (ATPG)
- sometimes detecting a defect can be time consuming as it depends on the device states
- leakage currents mask failure currents
- only deals with quiescent states

A huge drawback of IDDQ testing is, that only quiescent states are monitored. Transient loading events which cause defect related settling times are neglected in this analysis technique. For this reason the next section will cope with the dynamic behavior of current responses from a device.

3.3.2 Current and Voltage Signatures

Observing current and voltage signatures can be seen as an advanced method of IDDQ testing. According to the application of a certain input voltage, the time behavior of the resulting current is monitored. Each device model has basically its own current signature which is influenced by the design and layout. Process variations in the production only lead to a slight variation, but will not cause a significant change of the shape from the current signature. The current signature will stay in between a confidence interval which can be determined by taking random samples of known good parts out of production. The presence of a defect will alternate the time behavior of the current signatures. An additional resistive path can cause a change in the amplitude or the settling time of a current. A parallel connection to a given structure between V_{DD} and V_{SS} will cause an increase whereas a serial resistance will cause a decrease of the monitored current. Furthermore resistive failures show a linear behavior if the supply voltage is changed for stimulation purposes. Open contacts come always hand in hand with capacitive loading. If a DC voltage is applied, the current response will almost instantly reach a maximum value and after a certain settling time will show a constant amplitude. A possible floating node has almost the same current signature than those for open defects. The only difference is that the time behavior of the current is not constant after a given settling time, it is heavily dependent on the DC supply voltage and will show an alternating behavior. Floating nodes can be also identified by the AC biasing of a signal.

It can be shown that each floating node has a coupling capacitance to V_{DD} and V_{SS}. In combination with the AC signal, the floating node can be kept constant at $V_{DD}/2$ which causes a constant current consumption regarding the state of the affected gate. Summarizing this effects it is mandatory to observe the the current responses of a device at different DC levels and for AC signals with different frequencies. DC measurements reveal clear results for floating node related defects. Figures 3.14... 3.16 are giving a short overview about possible device responses for AC and DC voltage supplies under varying ambient temperature.

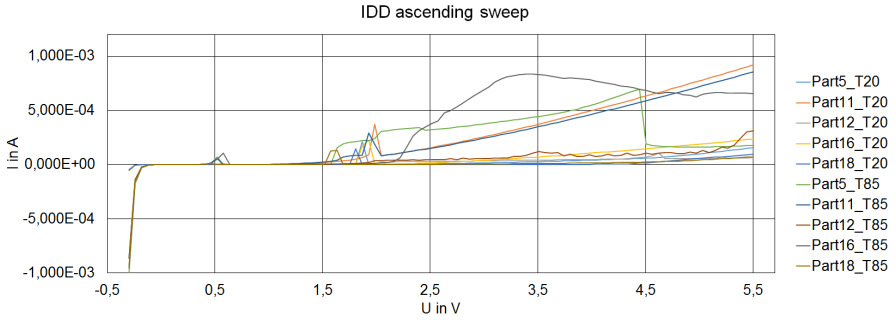

Figure 3.14: Ascending Voltage Sweep on Floating Node Defects with Thermal Stimulation

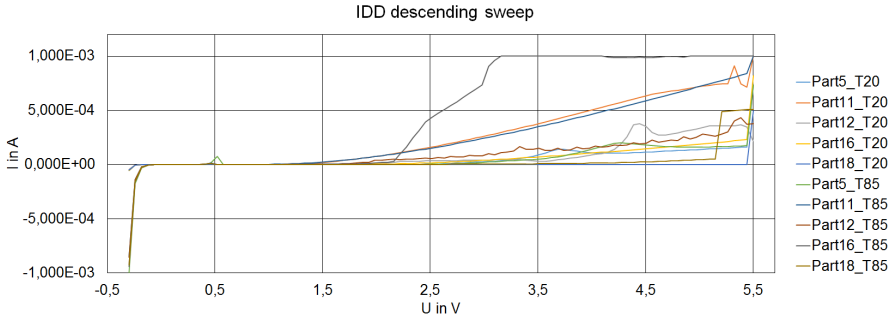

Figure 3.15: Descending Voltage Sweep on Floating Node Defects with Thermal Stimulation

The operating temperatures of the device have been alternated with a temperature chamber from $T = 20\,°C$ to $T = 80\,°C$ to test whether the device responses are changed due to a temperature dependency of the defects. Floating nodes reveal a very strong dependency on the ambient temperature which might be of use for further analysis. The AC measurements have been made from the negative suppressor diode voltage to up to the

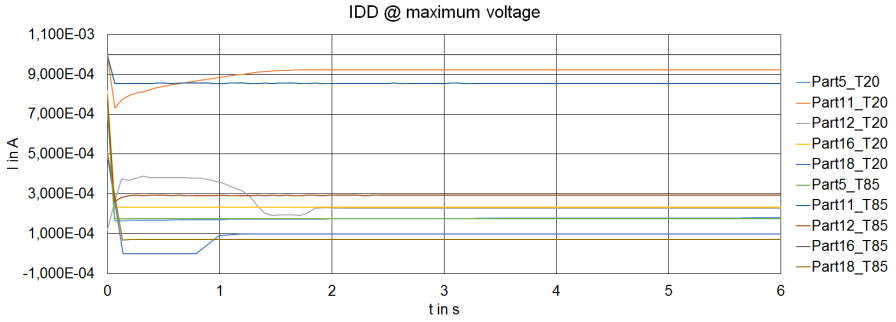

Figure 3.16: V_{max} on Floating Node Defects with Thermal Stimulation

maximum supply voltage and vice versa. A good device should show the same behavior in the current response for the ascending as well as for the descending sweep. Device specific events like a power on reset have to be neglected in the evaluation as they will only be noticeable in the ascending sweep. The amount of steps in between the upper and lower sweep voltage and the change rate $\Delta V/\Delta t$ or $\Delta I \Delta t$ will mainly affect the observed signatures (keyword: node impedances). The ascending and descending voltage sweep method can mainly be used to identify bridging contacts, shorts, floating nodes as well as to check the functionality of the suppressor diodes. Recommended DC voltages for the observation of current signatures are:

- Double Threshold Voltage
  By biasing the double threshold voltage each node of the circuit will be defined even if a node has an open defect. This is realized due to the capacitive coupling effect. For this reason each node of the circuit will be clearly defined. Possible cross flow currents between gates can affect the current consumption, which will be monitored by the time response. At higher biasing voltages the cross flow current can be masked, whereas possible bridging defects might stay unidentified.
- Minimum Operating Voltage
  Testing at the minimum operating voltage will ensure the full functionality of a device. Possible bridging defects might lead to a misbehavior of the device logic due to insufficient supply.
- Normal Operating Voltage

- Maximum Operating Voltage
  Disproportional high current consumptions can reveal floating nodes. The maximum operating voltage has almost the same influence as the operating temperature of the observed device.

In order to get high quality signatures a high high time and amplitude resolution is mandatory to record any transient behavior. Furthermore the measurement system should be reaction less and the test setup of the device should be designed to suppress parasitic capacitances as they will cause additional loading.

The author is actually working on defect models which arise from stimulation responses and transfer functions as it is used for parameter identification of automated systems. The basic theory behind this analysis strategy is to stimulate the device with an appropriate input signal (current/voltage) and to record the output response (voltage/current). By the use of this two time series a transfer function can be calculated

$$H(z) = \frac{Y(z)}{X(z)} = \frac{b_0 + b_1 z^{-1} + \ldots + b_N z^{-N}}{a_0 + a_1 z^{-1} + \ldots + a_M z^{-M}} \tag{3.6}$$

where

(z): denotes the z-Transform
$H(z)$: is the transfer function
$Y(z)$: is the output function
$X(z)$: is the input function
b_N: are the numerator coefficients
a_M: are the denominator coefficients

As the latest research results have shown, the numerator and denominator coefficients are directly linked with possible defects. To get useful evaluation results, it is mandatory that the two time series have been recorded concurrently and include no or very little noise.

Another promising technique for system identification is the use of neuronal networks. Neuronal Networks consist of neurons, signal weights w_{ij}, signal offsets and activation functions. The simplest configuration of a neuronal network consists of two layers as it can be seen in figure 3.17 where the output is calculated by:

$$x = \sum_{i=1}^{r} w_i^{(2)} s_i \left(\sum_{j=1}^{m} w_{ij}^{(1)} v_j + \Theta_i^{(1)} \right) + \Theta^{(2)} \tag{3.7}$$

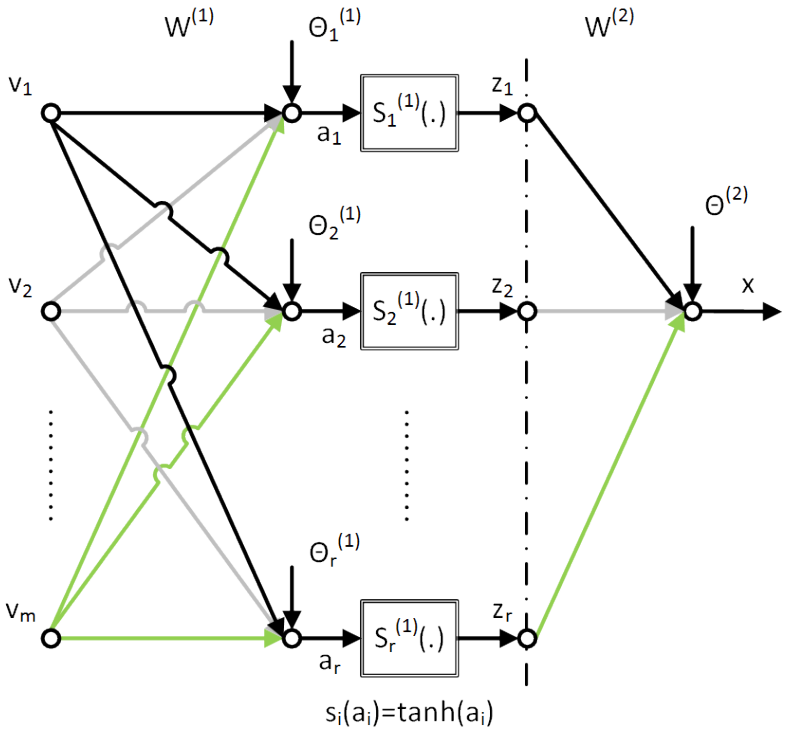

Figure 3.17: Structure of a Simple Neuronal Network

The first layer includes several neurons who define the first layer order and the second layer is inhabited by a single neuron which combines the outcomes of the first layer. The activation functions can be either:

- Step Functions

$$s(a) = \begin{cases} 1 & \text{for } a \geq 0 \\ 0 & \text{else} \end{cases}$$

- Symmetric Step Functions

$$s(a) = \begin{cases} 1 & \text{for } a \geq 0 \\ -1 & \text{for } a < 0 \end{cases}$$

- Sigmoids

$$s(a) = \frac{1}{1 + e^{-a}}$$

- Hyperbolic Functions

$$s(a) = tanh(a) = \frac{e^a - e^{-a}}{e^a + e^{-a}}$$

- Linear Function

$$s(a) = a$$

It has been shown that for most models the $tanh(x)$-functions are of best use. The neuronal system is then trained with regards to reach the minimum difference between the output of the neuronal network and the real system output. If the neuronal network has been properly trained, the signal weights w_{ij} and offsets Θ_i are representative values for device defects. Training neuronal networks is hard work since there exist no guideline for training techniques. Possible error sources are

- Over Training
- Too low or high layer orders
- Wrong neuron structure
- Useless or improper stimulation sequences

The presentation of results for the system identification on defective devices will be the topic of future research.

3.3.3 Liquid Crystal

Liquid Crystals are a very effective method to localize hot spots at a defective device. The observable defects are causing an increased current consumption and may originate from:

- Defective Oxide Layers
- Floating Nodes
- Shorts
- Leakage

The defects cause the device to locally heat up which leads to a transition event of the liquid crystal molecules. Just as water H_2O has four different physical states (gaseous, liquid, solid and plasma), liquid crystals have an additional second liquid physical state. The two different liquid phases are separated by a sharp transition temperature which is also called clearing point. Below the clearing point the liquid crystal optically appears to be milky white, whereas above the clearing point the liquid crystals appears

transparent. The underlying effect is that the molecules of the liquid crystals are rearranging. Another effect which comes hand in hand is the polarization of light. If linear polarized light is shining on a film of liquid crystals while the temperature is below the clearing point, the polarization of the reflected light won't be changed. Whereas if the temperature of the liquid crystal

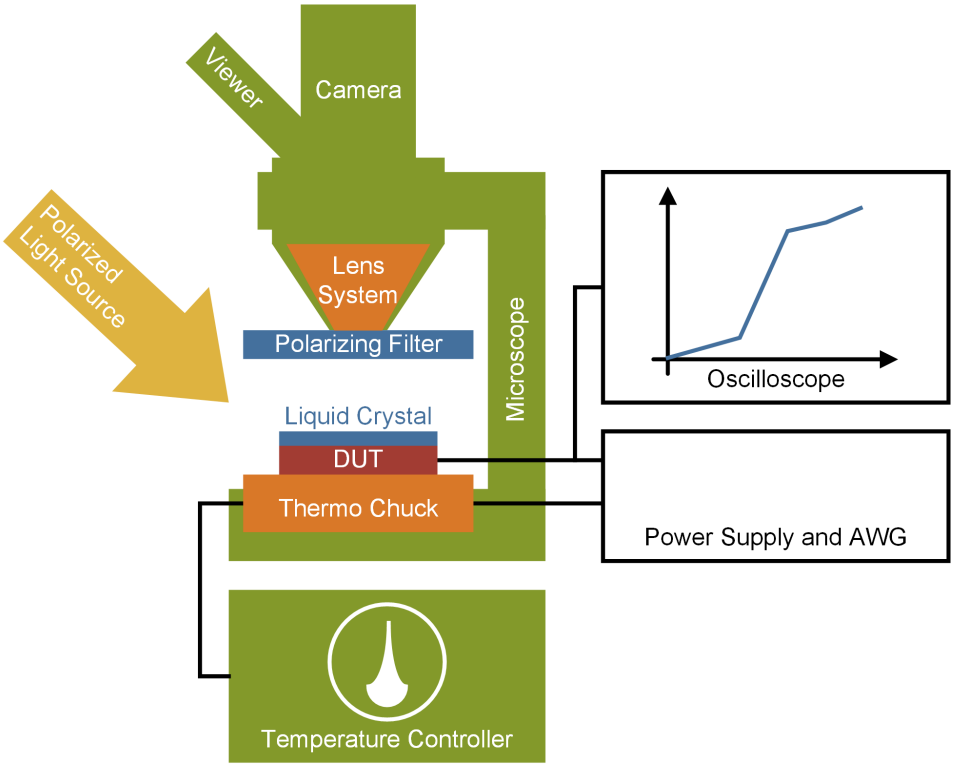

Figure 3.18: Schematic of Liquid Crystal Failure Analysis

is above the clearing point, the polarization of the light will be changed according to the thickness of the liquid crystal film. As it is shown in figure 3.18 it is very easy to observe this polarization effect by the use of a polarizer and analyzer. Local hot spots will cause the liquid crystal to change its liquid phase which leads to a change in the polarization direction of the light. As the analyzer will only allow light with the same polarization direction than that of the polarizer to pass through, the local hot spots will result in dark spots at the image sensor and the viewer. The main challenge of this technique is now to detect the device state in which the increased current consumption can be monitored and at which supply conditions the observable effect appears. An alternating voltage source causes a change

in the current and therefore the dissipated heat. This will also lead into a change of the liquid phase if the clearing point is exceeded. There exist a variety of liquid crystals according to the field of application. Also power dissipations of around $P = 1\,mW$ are detectable without much effort. If the change in temperature due to the defect is not enough to exceed the clearing point temperature, external heating can be applied to preheat the device. This technique almost instantly reveals possible defect spots of the device, but the failure analyst has to keep in mind that the observed hot spot must not necessarily correlate with the real defects location. Moreover most of the time only affected gates and conductors are dissipating heat due to the original defect.

3.3.4 Freezer Spray

A much cheaper and faster technique to detect hot spots is the use of a Freezer Spray. Commercial available freezer sprays allow the analyst to cool down the device to $T \approx -50\,^{\circ}C$ whereas at the same time a thin ice film is created. Again, due to the dissipated heat at the possible defect spot, the created ice film will be molten. As easy as this technique may seem, there are numerous undesired effects which come hand in hand with the cooling of the device. First of all the threshold voltages of the device will be changed as the coolant cannot be sprayed on small spots. This might mask possible device defects as for instance floating nodes. Additionally the molten ice will result into a small amount of fluid which can cause an electrical connection between two different potentials and will therefore lead into a false interpretation of the failure current. Another aspect is the affect of the cooler spray itself on the passivation layers of the treated device. It has been observed in laboratory environment that the extensive use of freezer spray may not only cause mechanical pressure but is also able to alter the properties of the passivation layer which causes additional defects.

3.4 Functional Test Pattern Generation

Each integrated circuit can be divided into two domains, namely the analog and the digital domain. As it has already been discussed, the possible number of errors in the analog domain is a multiple of the failure modes in the digital domain. Functional Test Pattern Generation is a well known design for testability technique which allows the verification of the digital domain within a few steps. The most common fault model in the digital domain is the stuck at fault model and offers the best experience. There also exist a variety of computer aided tools which allow the automatic generation of test patterns according to the schematic of a device. Furthermore other known faults as opens, bridging or floating nodes are covered most of the time in the digital domain with the stuck at fault model. For the analog domain and for memory devices other fault models have to be considered as they are not directly comparable to fault models in the digital domain. These faults include timing and other technology-dependent faults. The main goal of functional test patterns is to stimulate a device with a specific pattern and to compare the actual response against the expected response. If there is a difference between both responses, a clear fault is indicated. The effectiveness of this analysis technique is measured by the fault coverage which is represented in figure 3.19.

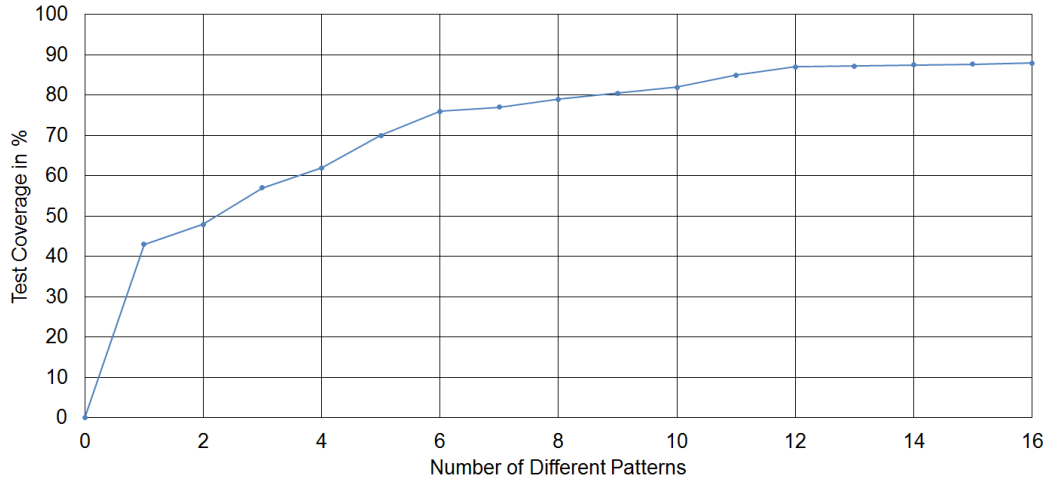

Figure 3.19: Fault Coverage with ATPG

Each pattern relates to a certain quantity of information from the device. If the amount of test patterns is increased, the fault coverage must not necessarily be increased too. Moreover the test coverage will settle at a certain percentage. Furthermore the patterns are created under the following requirements

- Pattern Length
- Analysis Time
- Cost of Test

as Versen, 2006 is reporting. Devices can consist of two domains. Combinational logic where very simple and effective algorithms can be applied according to the state of the device and sequential logic where highly sophisticated patterns are needed for stimulation purposes. By the application of ad hoc techniques and scan design, the design for testability can be improved extensively. The scan design of a device allows the formerly se-

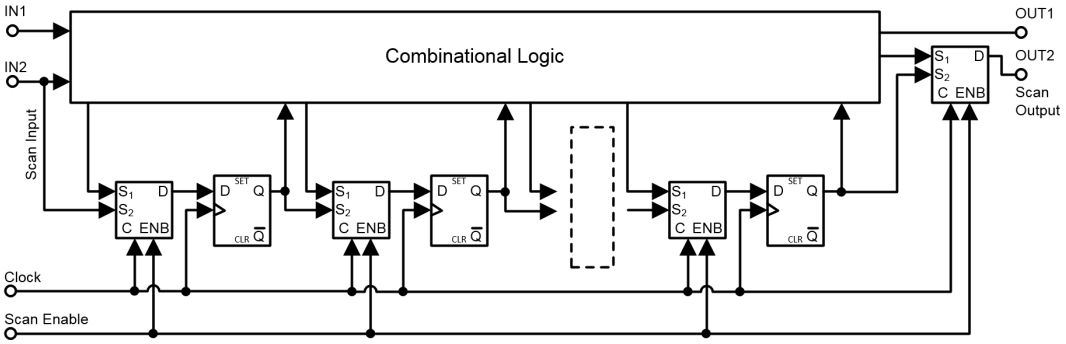

Figure 3.20: Scan Chain Example

quential logic to be converted into a combinational and partially sequential logic by increasing the observability and controllability of the circuit. An example for a scan chain design is shown in figure 3.20. For this purpose, additional scan flip flops, multiplexers, scan input, scan output, scan enable and a scan clock lines have to be added to the device design. This leads in the first place to an increase of die-size and therefore to an increasing probability of device defects due to the known production defect density. There exist two kinds of pattern generation techniques. The first one is a static technique which allows no alterations during the application of the test pattern. The dynamic technique will alter the input pattern sequence accordingly to the former response of the device.

The most used algorithms are:

- D-Algorithm
  It allows five different states of a signal node. Each state in a cell can be defined by setting an objective and using backward or forward implication to define further states. If the forward or backward implication is stopped and signal nodes are still undefined, assumptions are made in order to observe the desired objective.
  - 0: represents logic 0
  - 1: represents logic 1
  - X: indicates unknown or unused state
  - D: $D = 1$ is fault free, $D = 0$ is faulty
  - $\bar{D}$: $\bar{D} = 1$ is faulty, $\bar{D} = 0$ is fault free
- PODEM Algorithm - Path Oriented Decision Making
  This algorithm basically works just as the D-Algorithm. After defining the faulty node in the circuit (e.g. a stuck at zero fault), forward and backward implication is used in order to find a test pattern which will identify the faulty node. The generated pattern is therefore used to make the defined fault in the circuit observable and optimized to achieve a fast test time and simple test patterns.
- FAN Algorithm
  The fan-out of a signal node actually defines how how much load a certain output stage has to drive. By minimizing the amount of gates which are switching at the same time and by minimizing the gate switching rate itself, the fan-out of a signal node can be decreased significantly. This leads to a reduction in spikes in the supply and therefore distortion in the circuit. FAN Algorithms are used to produce so called power-aware patterns.

The main purpose of scan design is to increase the observability and controllability of a device without making any physical preparations like probe pads on the device. The device will be able to work in the normal mode where all gates operate under normal conditions and the scan mode where the internal states of a sequential domain is controllable and observable by multiplexers and scan flip flops. As Chunlei, L. Zhai, Motohiko, Ma, et al., 2010 are reporting, shorter test programs are preferred in combination with BBDL techniques and lead to much better analysis results. Due to the additional scan flip flops and the signal line area overhead the working frequency of the device will be reduced which has to be a recognized factor during the design of the device. If a test pattern is used to work with DALS

or another analysis technique it is mandatory to provide two additional informations for evaluation purpose. The comparison result between the real and the expected output of the pattern which can be a simple pass/fail flag and a synchronization clock which moves the laser from pixel to pixel.

The next chapter will present the results of the simulations and experiments in the laboratory regarding the DALS analysis technique.

4 Experiments

The first experiments will deal with the used system components for the DALS analysis technique. This will cover investigations on the functional tester *TESEDA v520* as well as the laser scanning microscope *HAMAMATSU Phemos 1000*. For each experiment the expectations as well as the results will be separately discussed and are based on the theory already given in the previous chapters. After this first contact with the system, a manipulation of an originally good part by the use of a FIB should reveal the failure analysis capability of the used analysis setup. Furthermore it is planned to discuss the application of the proposed setup on an unedited device, as the circuit editing with the use of a FIB always includes the possibility of unintended device damaging. Furthermore the difference to analog DALS will be highlighted.

4.1 DALS synchronization

The basic setup for the following measurements is shown in figure 4.1.

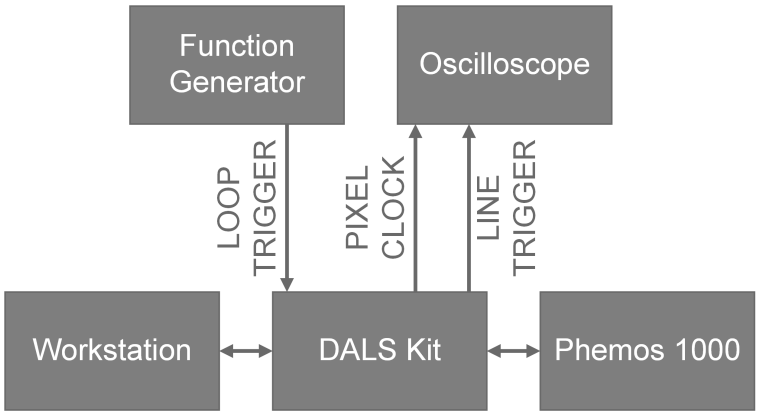

Figure 4.1: Experiment1 - Scan Setup

Each available DALS technique is dependent of the synchronization between the stimulation unit and the measurement unit. The desired behavior of the system is, that each pixel and therefore point on the DUT is independently scanned, but includes the same information then it's neighboring pixel. It is mandatory that each pixel is stimulated with the same sequence regardless its location. There exist two common synchronization methods which are internal and external clock reference.

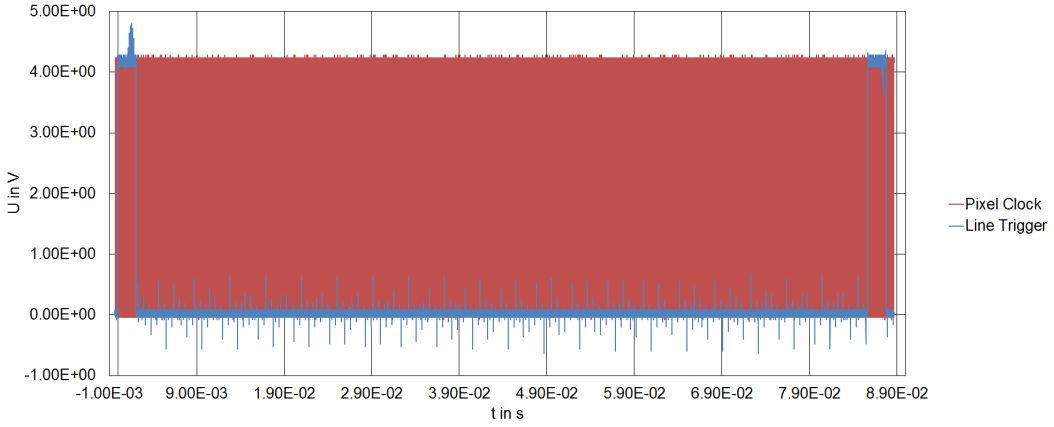

Figure 4.2: Experiment1 - *scan direction* $= 0|180$, *frame rate* $= 90\,s$

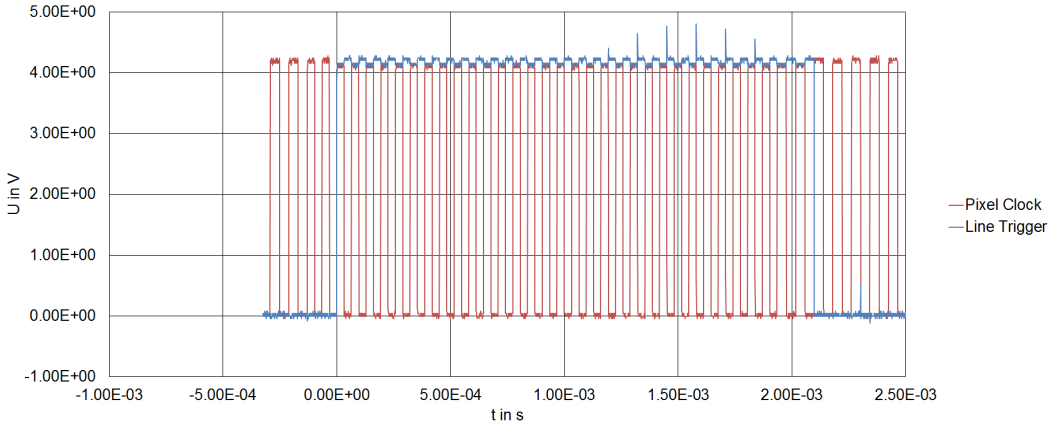

Figure 4.3: Experiment1 - DETAILS: *scan direction* $= 0|180$, *frame rate* $= 90\,s$

Figure 4.2 up to 4.5 represent the necessary synchronization signals for internal clock reference, which is defined by the scan unit of the LSM.

The HIGH pulse of the PIXEL CLOCK indicates the movement of the laser. Its period is defined due to the amount of pixels of the image, the overall scanning time, the area overhead which is also referred to as blind pixels as well as the scanning direction. The scanning direction represents the sequence in which the pixels of the image are stimulated by the laser. They can be observed in figure 4.6.

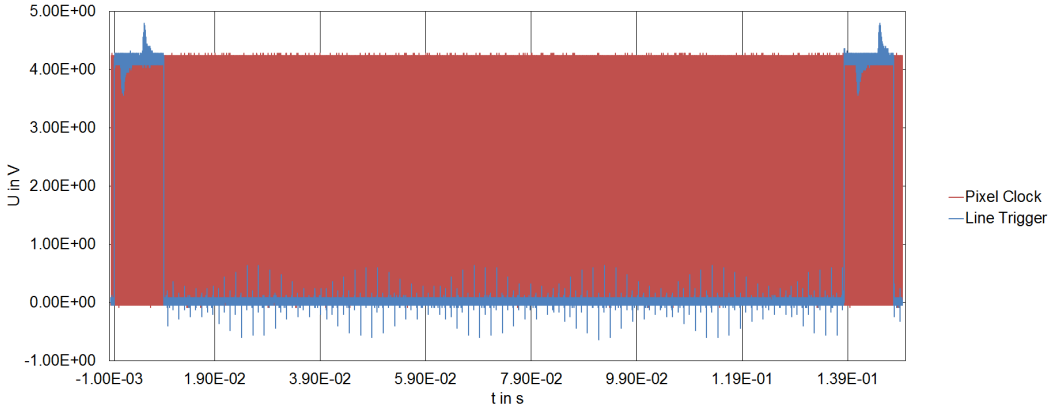

Figure 4.4: Experiment1 - *scan direction* $= 90|270$, *frame rate* $= 144\,s$

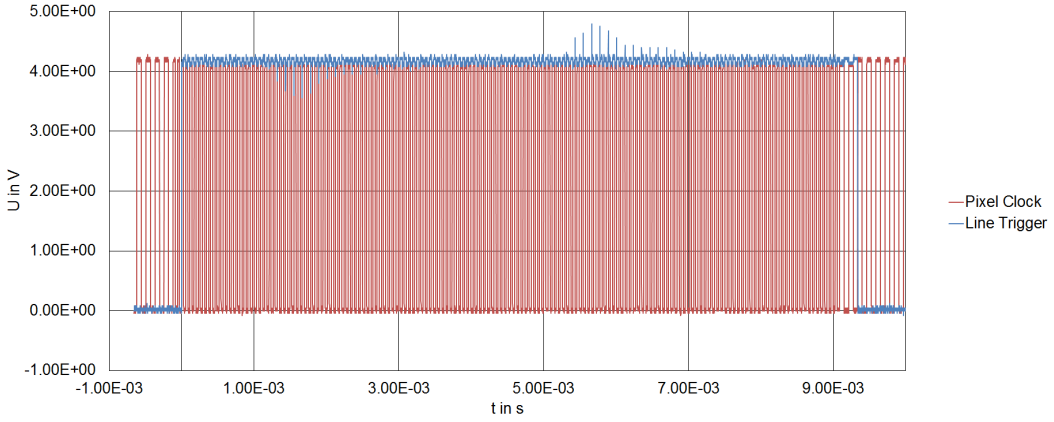

Figure 4.5: Experiment1 - DETAILS: *scan direction* $= 90|270$, *frame rate* $= 144\,s$

As it can be seen in figure4.2 to 4.5, the pixel clock is accompanied by the LINE TRIGGER signal. Whilst the line trigger is HIGH, the laser is active but not actually positioned on a defined pixel which results due to the

positioning into a new column or row. Regarding the used scan direction, the blind pixels can vary. For the setup frame rate which equals the total scan time, we observed a line trigger period of $t_{LINE\ TRIGGER} = 85.642\,ms$ for figure 4.2 and $t_{LINE\ TRIGGER} = 138.343\,ms$ for figure 4.4 respectively. The pixel clock varied according to the state of the line trigger signal. As this is an undesired behavior, it is recommended to use an external clock reference for synchronization purposes.

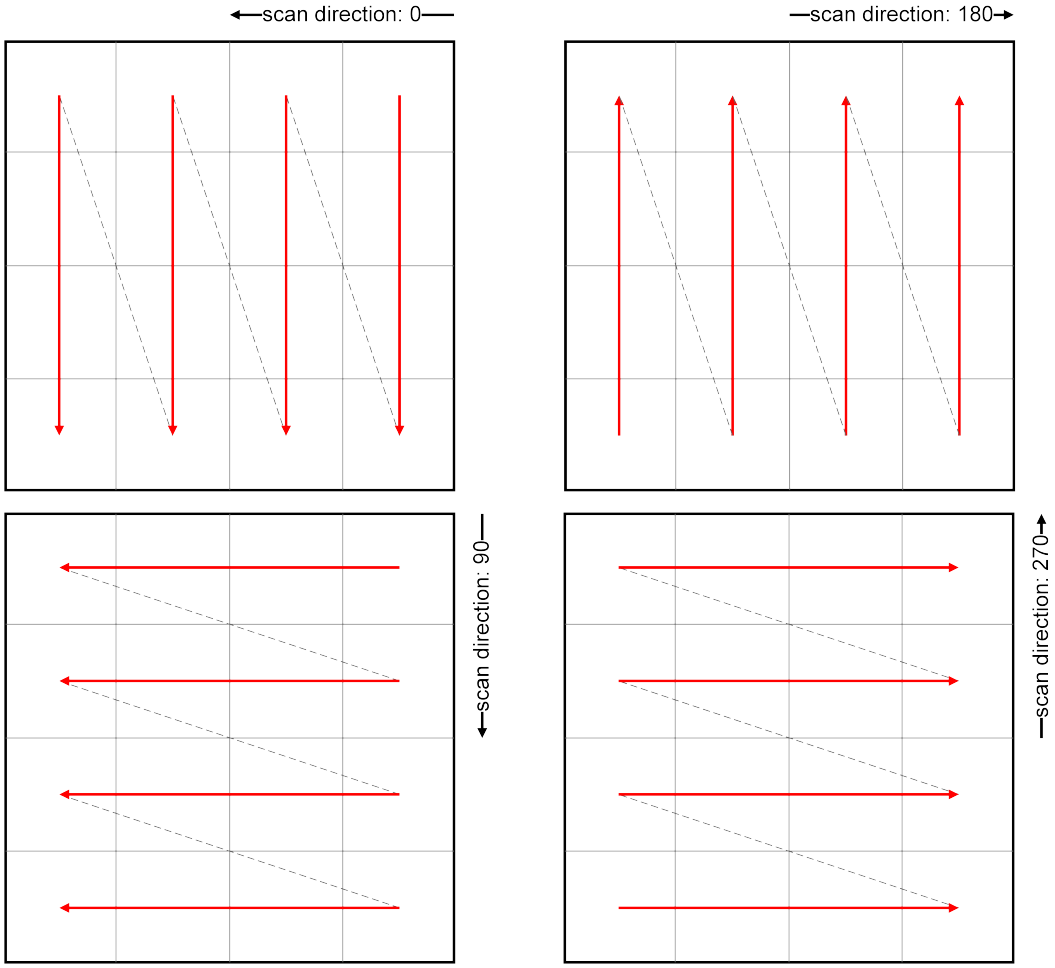

Figure 4.6: Scan Directions

Figures 4.7 up to 4.10 are showing the synchronization signals for an external clock reference for different scanning directions.

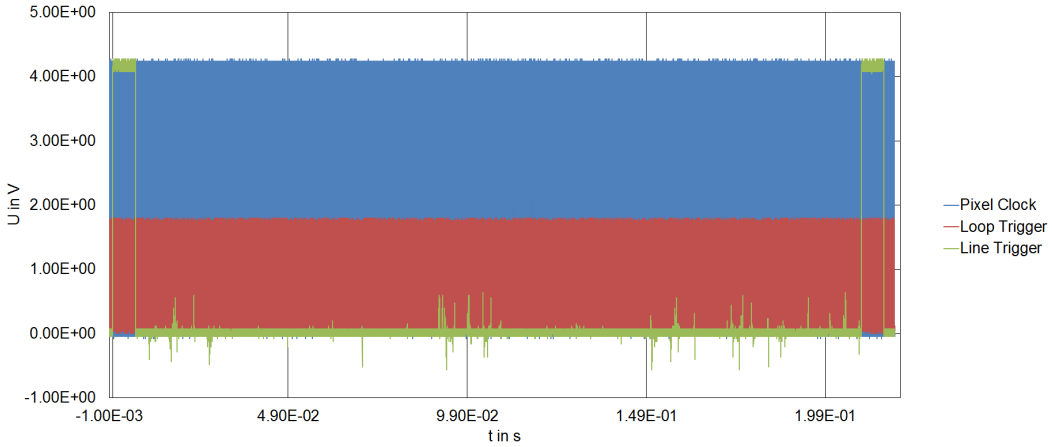

Figure 4.7: Experiment1 - *scan direction* $= 0|180$, $f_{IN} = 5\,kHz$

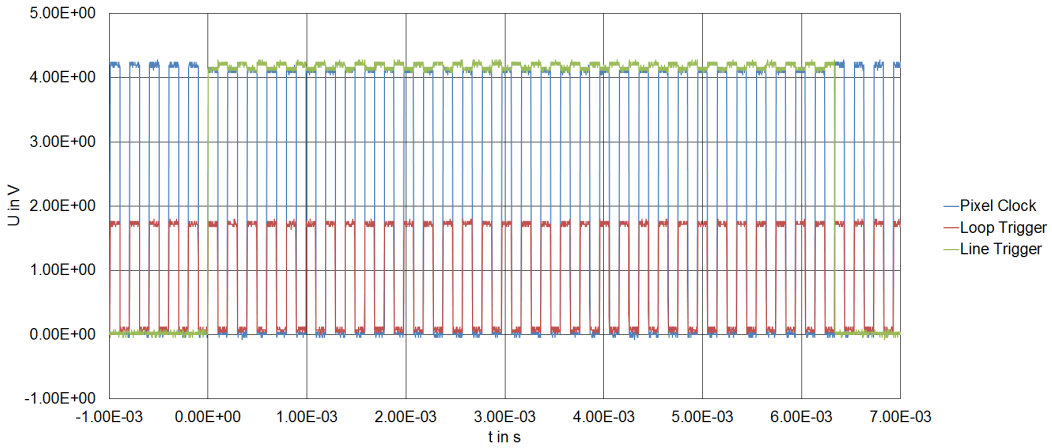

Figure 4.8: Experiment1 - DETAILS: *scan direction* $= 0|180$, $f_{IN} = 5\,kHz$

Due to the limited positioning speed, the external clock reference must be lower than $f_{CLOCK} = 8\,kHz$.

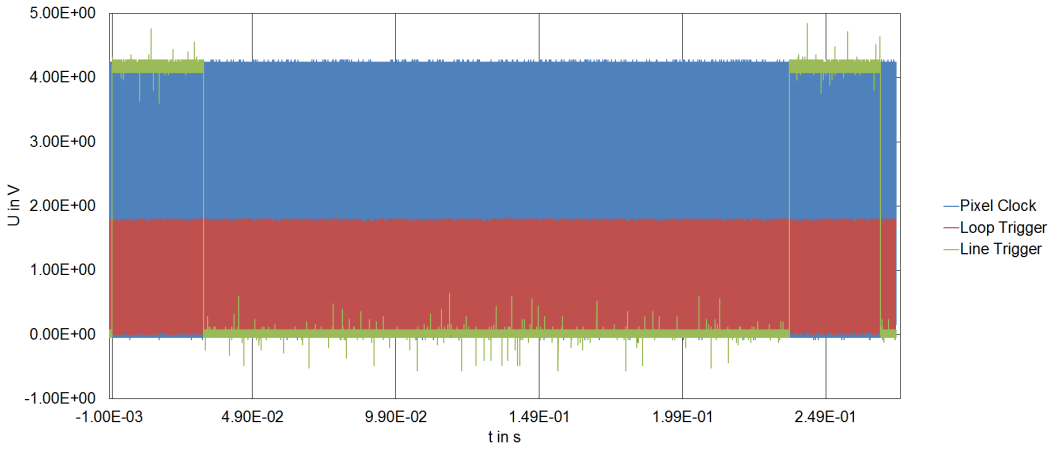

Figure 4.9: Experiment1 - *scan direction* $= 90|270$, $f_{IN} = 5\,kHz$

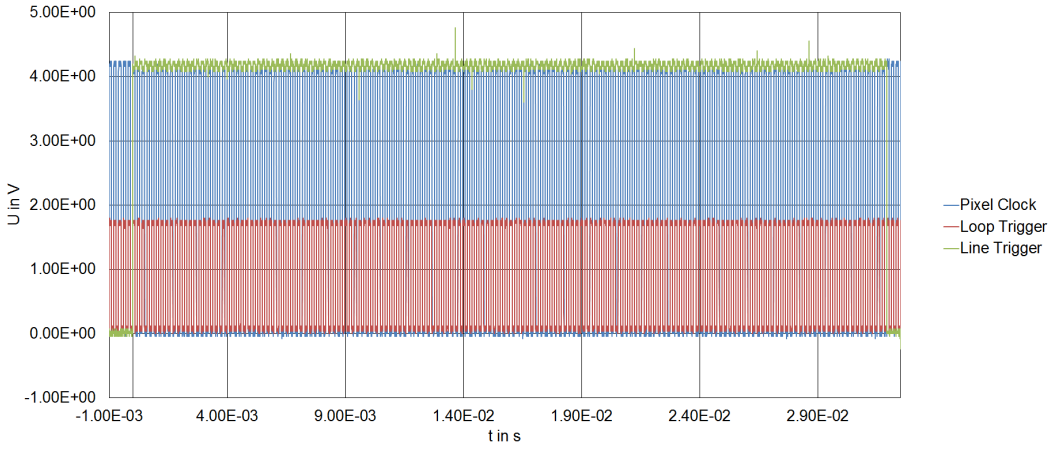

Figure 4.10: Experiment1 - DETAILS: *scan direction* $= 90|270$, $f_{IN} = 5\,kHz$

The external clock signal is furthermore referred to as LOOP TRIGGER. Figure 4.11 shows the used setup configuration for further investigations. A pixel will be marked if the TESTER SIGNAL is set to HIGH in between a single pixel clock cycle and therefore the test was failing from the external pass/fail evaluation unit.

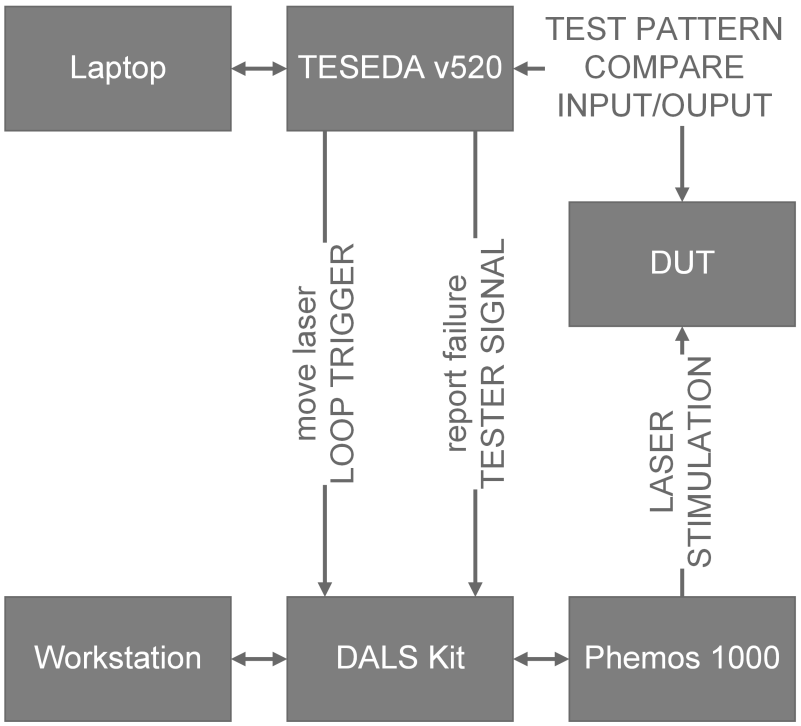

Figure 4.11: DALS Setup

There are several ways of how to interpret the pass/fail events according to the configuration in the control software *SemiShop*:

- Analog
  During the scan of a pixel, the input from TESTER SIGNAL is being integrated for the pixel dwell time. Therefore the resulting value is compare able to OBIRCH measurements.

- Latch A
  During the scan of a pixel, the input from TESTER SIGNAL is monitored. If the TESTER SIGNAL shows a HIGH within a PIXEL CLOCK, the corresponding image data of the pixel will be marked faulty. Otherwise if the TESTER SIGNAL shows LOW during the dwell time of the pixel, the pixel will be kept unmarked and therefore corresponds to a pass evaluation.
- Latch B
  During the scan of a pixel, the inputs from TESTER SIGNAL which shows a pass/fail evaluation from the functional tester as well as the TESTER TRIG signal are being monitored. Only if the TESTER TRIG is set to HIGH, a possible defect indicated with a HIGH at the TESTER SIGNAL is assigned to the image data. If the TESTER TRIG is LOW when the TESTER SIGNAL is at any possible level, the image data won't be changed and will therefore indicate a pass evaluation.
- Counter
  During the PIXEL CLOCK period, the amounts of HIGH pulses from TESTER SIGNAL are counted. Due to the counted fail states, the contrast of the influenced pixel is changed accordingly.

The preferred methods for the evaluation are *Latch A* or *Counter* as only two signals must be provided. Furthermore it is necessary to define the proper termination of $50\,\Omega$ or $HIGH$ at the SemiShop software. As we have now experienced the behavior of the synchronization unit, the upcoming sections will reveal the temperature influence of the IR laser with $\lambda = 1300\,nm$ and $P_{laser} = 100\,mW$ for several test structures.

4.2 Temperature influence of the IR laser

There exist several ways to monitor the temperature influence which include laser calorimeters, bolometers, photo diodes and so on. The easiest methods are to monitor either the resistance change of a test structure, or the shift in the threshold voltage of a semiconductor device. For this reason the Scribe Line Monitors - SLM on a wafer have been used because they provide several test structures in different configurations, while the device characteristics are well known.

The SLM structures are used to monitor process parameters and furthermore serve the purpose of spacings in between the manufactured integrated circuits for dicing. The width of the SLM is fixed at $80\,\mu m$ and the samples are produced in a $0.35\,\mu m$ process.

4.2.1 Scribe Line Monitor - Diode

The basic test setup is presented in figure 4.12 and consisted of n- and p-diffusion diodes of different dimensions and voltage structures. For the

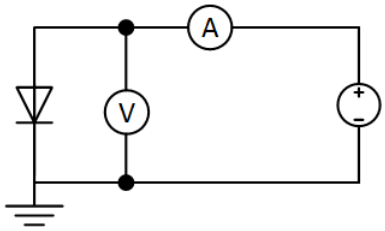

Figure 4.12: Experiment2 - SLM Diodes

test a simple voltage biasing in forward direction of the diode was chosen to be best practice, whilst the current was monitored with an ammeter. Of course the biasing was changed according to the p-, or n-diffusion diodes. Just by stimulating the devices with the IR laser at maximum output power, no influence on the diodes temperature characteristic could be noticed while the following settings were alternated

- laser power
- scan area setup: horizontal line scan, spot scan, area scan
- voltage bias: $0.1 - 0.8\,V$

As the test wafer was placed within the Phemos chamber upon a thermo chuck whilst the test structures have been contacted with prober needles we were able to externally apply heat to the test structures. For this combination, the temperature dependence could be clearly monitored, starting from temperature differences $\Delta T > 5\,^{\circ}C$. Apparently the laser could not heat up the test structures. This behavior can be explained as silicon is nearly transparent for wavelengths of $\lambda = 1300\,nm$. Additionally the metal lines next to the diodes test structures were located too far away in order to achieve indirect heating. The upcoming experiment was designed

to overcome the absorption issues by the use of transistor test structures. The doping concentration of the active regions were much higher and also metal lines at the gate of the transistor seemed to be a proper absorption location.

4.2.2 Scribe Line Monitor - Transistor

Figure 4.13 is showing an example transistor test structure. We have tested several structures for 3.3 V and 5 V configurations both for n-, and p-channel transistors of different W/L-ratios. The influence of the laser has been no-

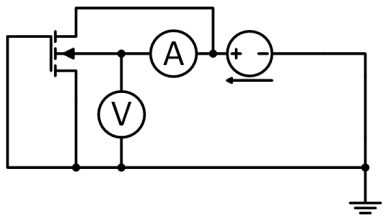

Figure 4.13: Experiment3 - SLM Transistors

ticed while the current-voltage characteristics of the parasitic diode between body and drain has been monitored. The following settings were alternated.

- laser power: Due to the small noticeable influence, the laser power was kept at 100 %
- scan area: The highest noticeable stimulation resulted from single spot stimulation. This behavior originates from the fact that the mechanical positioning of the deflecting mirror takes some time. Furthermore the scan direction of the laser significantly changes the temperature influence on a device structure. The highest influence was monitored to occur for scans parallel metallic structures while the lowest thermal influence was monitored for scans vertical to metallic structures.
- scan time: Longer pixel dwell times resulted in higher stimulation results. The minimum scan time for noticeable stimulation signals was about $t = 60\,\mu s$ while the laser power was set to 100 %.
- input current: The input current was set in order to monitor the characteristic diode voltage behavior within a range where self heating could be neglected.

- thermo chuck temperature: The temperature was set from $T = 27.34\,^{\circ}C, 40\,^{\circ}C$ to $60\,^{\circ}C$

We observed that the laser could heat up the device indirectly while the laser was focused on the contacting metal at the gate of the transistor as it is indicated in figure 4.14.

Figure 4.14: Experiment3 - Laser Location ©amsAG

Furthermore only the $20x$ lens was used for stimulation purposes. The highest temperature influence was monitored for structures with the largest metal covered areas. Figure 4.15 is showing the stimulation results for constant current biasing for the n-channel transistors. The current was set

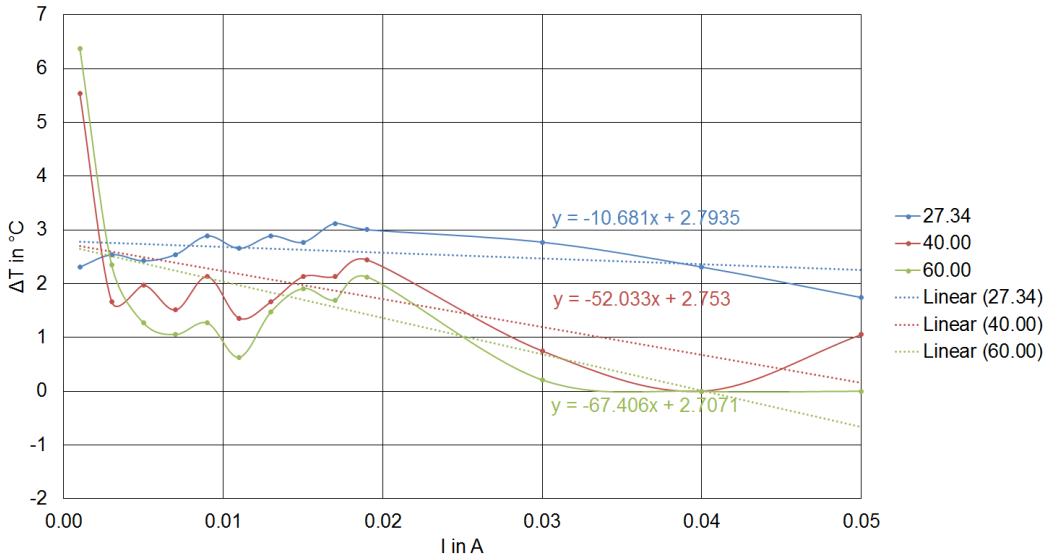

Figure 4.15: Experiment3 - ΔT n-Channel SLM Transistors

up in a way, that self heating was avoided. It was clearly observable that the temperature influence of the IR laser was maximum for lower current bias values and lower ambient temperature. Figure 4.16 is showing the same results for the used p-Channel SLM transistor structures at constant current biasing. A slight setup failure for the set up of the ambient temperature at $T_{ambient} = 40\,°C$ caused the device to heat up furthermore, therefore the average observed temperature influence of the IR laser is supposed to settle around $\Delta T \approx 5\,°C$. The temperature increase couldn't be noticed for all applied temperatures of the thermo chuck in the same way. The higher the temperature was set on the thermo chuck, the lower was the influence of the laser. This can be explained due to the limited thermal capacity of the test structure. Additionally, the device showed a greater dependence on the laser heating where a small current bias was applied. For currents $I \geq 0.05\,A$ the total temperature change was noticeable smaller.

Furthermore the temperature influence on p-channel structures was noticeable higher than those for n-channel transistors.

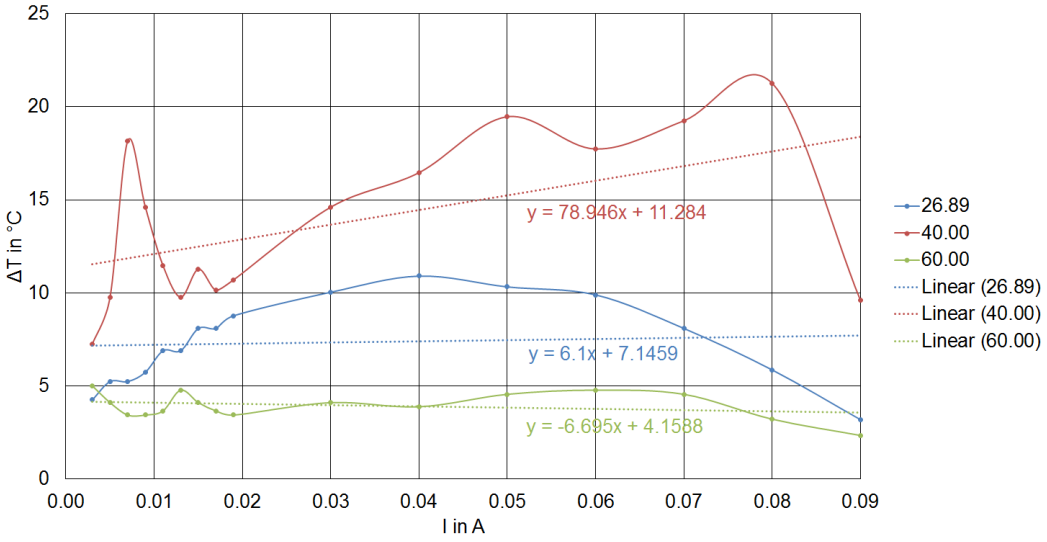

Figure 4.16: Experiment3 - ΔT Voltage Bias

The measurement results have been summarized in table 4.1. In order to

type	$T_{ambient}$ °C	ΔT °C
n-channel	27.34	2.61
	40.00	1.87
	60.00	1.57
p-channel	26.89	7.35
	40.00	$\approx$ 5.50
	60.00	3.94

Table 4.1: Average ΔT for n-, and p-channel SLM Transistors

prove the shown results, a test structure on a real device with several metal layers and mixed signal stages will be investigated in the next section.

4.2.3 Suppressor diode - Mixed Signal IC

The used mixed signal device for the final temperature test is made up of three metal layers and includes protective diodes on each of its inputs. As this suppressor diodes are very well characterized, the diode $D4$ as it can be seen in figure 4.17 has been used for further testing. The laser was chosen

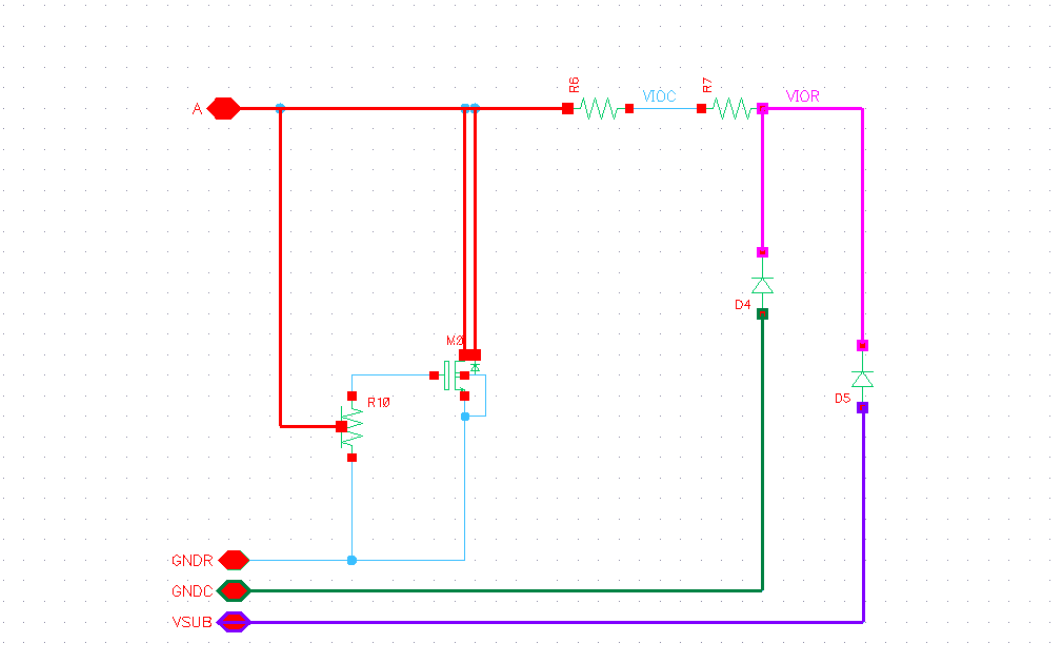

Figure 4.17: Experiment4 - Test Structure ©amsAG

to be focused on the most sensitive point of the test structure as it can be seen in figure 4.18 in the point scan mode, where the laser is not moved across the device. This location is actually directly above the suppressor diode $D4$. In the first test run again the temperature influence of the laser was monitored in addition to the variation of the ambient temperature with the thermo chuck and the biasing current. Figure 4.19 shows the corresponding measurement values. The used lens magnification was $20x$ whilst the laser power was kept at 100 %. The measurement revealed again a strong dependency of the temperature influence regarding the applied bias current and the ambient temperature. The higher the bias current and the ambient temperature were, the lower the influence of the IR laser was on the test structure.

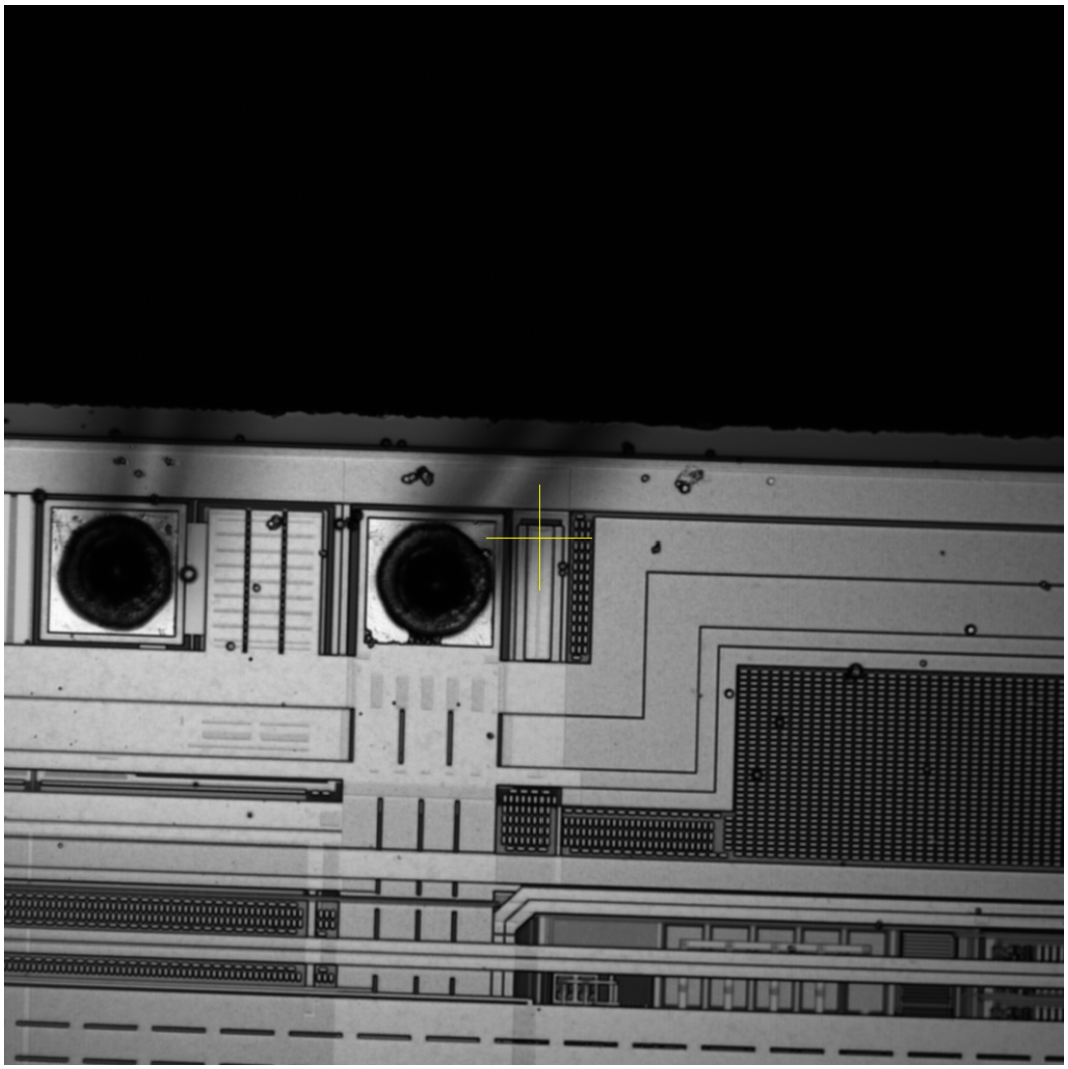

Figure 4.18: Experiment4 - Laser Location

This behavior was again in correlation with the already made observations. In the final measurement, the influence of the different lenses should be evaluated. For this reason, the laser power was again kept at 100% while the current bias was alternated. As figure 4.20 is revealing, the temperature influence is heavily depending on the used magnification lens. The best use lenses for further analysis are therefore $5x$ IR, $20x$ IR and $50x$ OBIRCH.

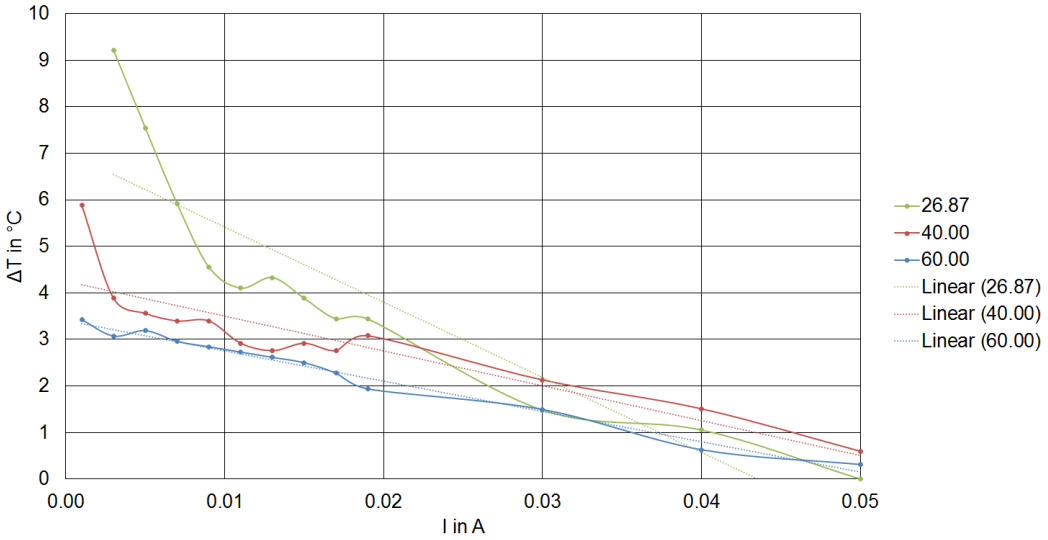

Figure 4.19: Experiment4 - ΔT Current Bias

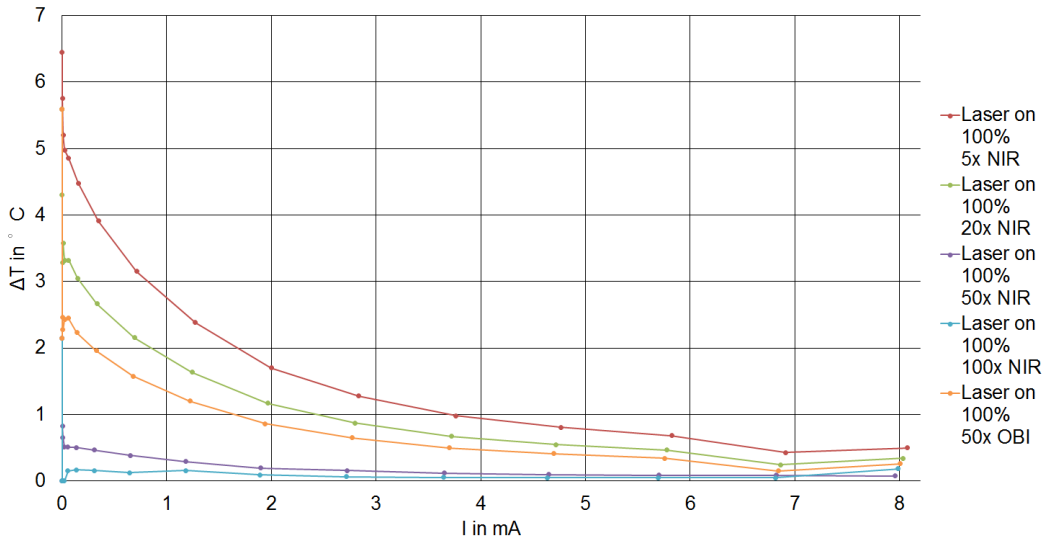

Figure 4.20: Experiment4 - ΔT Lens Influence

Related research has shown a similar behavior for the used setup. Boit et al., 2004 are reporting a maximum temperature influence of $\Delta T = 1.4\,°C$ at $P = 100\,mW$ laser power, while Liao et al., 2005 have monitored around $\Delta T \approx 10\,°C$ for their test structures and for the same settings. Finally we have already mentioned the rule of thumb in equation 3.5 to calculate the temperature increase for a given laser power.

4.2.4 Simulation of Temperature Influence

One of the questions which arise from the previous experiments is that how it is possible to achieve different stimulation temperatures when different lenses are used. Research has shown that the main influencing parameters are:

- Spot Size
- Transmission Rate of the Lenses

Due to measurements and the available data sheets of the used lenses we were able to calculate all relevant laser parameters. As it can be seen in table 4.2 the most promising evaluation results are expected when the lenses $5x$ IR, $20x$ IR and $50x$ OBIRCH are used because then the highest laser power can be provided on the DUT's surface which is in correlation to the experimental results. The available laser power on the surface of the DUT is strongly dependent of the optical path of the laser light. For this reason it has already been indicated by other researchers that the stimulation results can be enhanced if a laser with higher output power is used.

Type	Zoom	N.A.	WD	F	Spectral Transmittance	Spot Diameter	Available Laser Power	Intensity
	x		mm	mm	%	m	mW	$mW/\mu m^2$
M Plan Apo NIR	5	0.14	37.5	40	76	11.329 E-06	49.9	0.495
M Plan Apo NIR	20	0.40	20.0	10	70	3.966 E-06	35.6	2.883
M Plan Apo NIR	50	0.42	17.0	4	62	3.776 E-06	10.9	0.973
M Plan Apo NIR	100	0.5	12.0	2	57	3.172 E-06	4.3	0.544
Plan NIR 50	50	0.76	12.0	4	72	2.087 E-06	37.2	10.876

Table 4.2: Lens Overview for $\lambda = 1300\,nm$

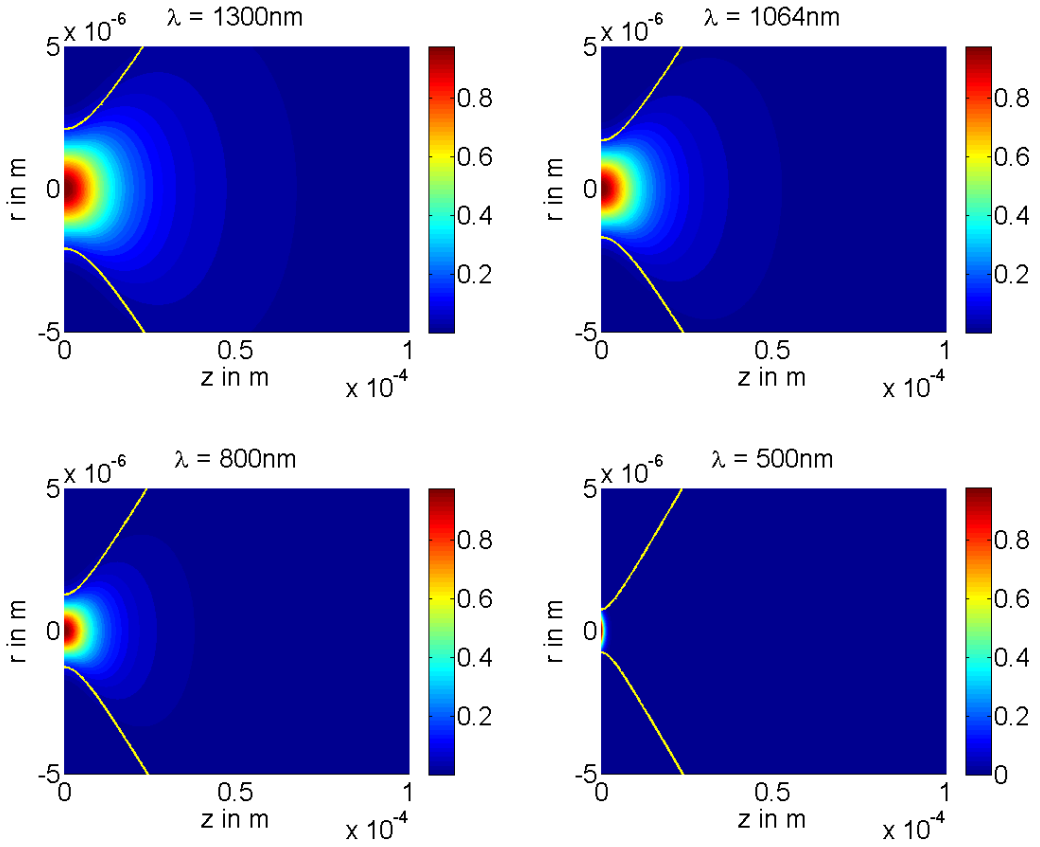

Figure 4.21: Simulation - Spatial Light Absorption

$$I(r,z) = I_0 \left(\frac{w_0}{w(z)}\right)^2 exp\left(\frac{-2r^2}{w^2(z)}\right) exp\left(-\alpha z\right) \quad \text{for front side} \tag{4.1}$$

$$I(r,z) = I_0 \left(\frac{w_0}{w(z-d)}\right)^2 exp\left(\frac{-2r^2}{w^2(z-d)}\right) exp\left(-\alpha z\right) \quad \text{for back side} \tag{4.2}$$

As Kiyan, 2010 has shown in her dissertation, equation 4.1 and 4.2 can be used to calculate the spatial intensity profile of a laser light beam, if the initial beam radius, the point of focus as well as the laser intensity are known. For simulation purposes figure 4.21 shows the spatial intensity distribution where the laser power has been normalized to 1 and the point of focus was set to be on top of the front side surface while the initial beam diameter was $w_0 = 2.1\,\mu m$. The dependency of the used laser wavelength λ can be clearly observed. The simulations are continued with a simple FEM based conductor rod with the dimensions $WxHxD = 1x0.6x11\,\mu m$. The rod

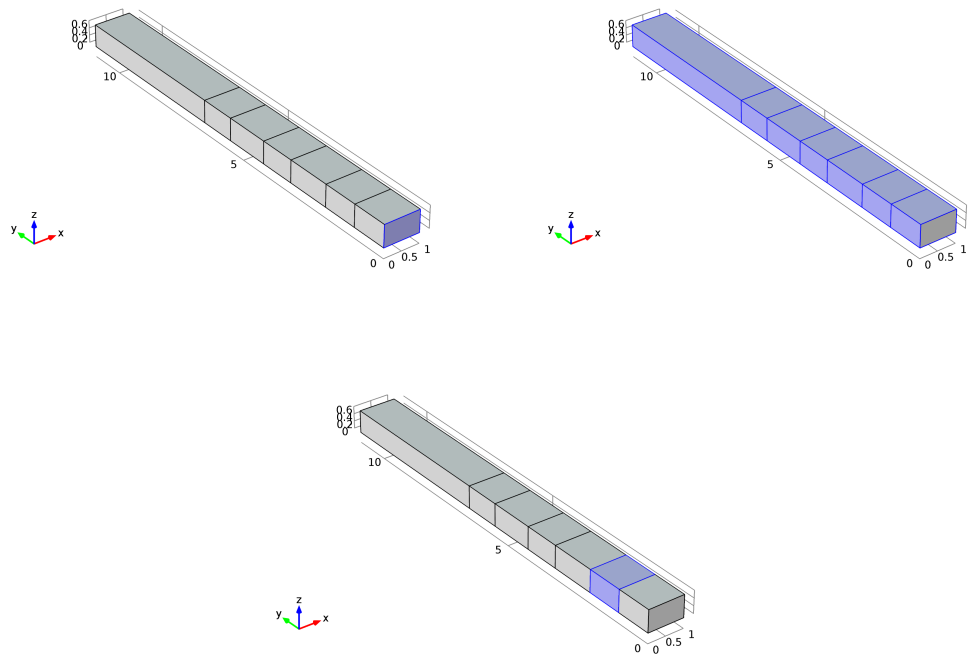

Figure 4.22: Simulation - Conductor Setup

was divided into several regions with one explicit region of the dimensions $WxHxD = 1x0.6x1\,\mu m$ where heat was directly applied. The upper left representation of the rod in figure 4.22 is showing the fixed constraint where the heat transfer was inhibited. The upper right representation represents the ambient heat flux area as if the rod would be surrounded by air. The bottom figure shows the position of the heat source at the rod. The heat source was chosen to be $P = 20\,mW$ as the optical path of the laser scanning microscope is not ideal and will lead to losses of the total available laser power of $P_{tot} = 100\,mW$. The results of the conductor simulation are shown in figure 4.23. As it was expected the temperature of silicon is increasing much faster in time due to the much lower thermal capacity if the same amount of energy is transfered (see also equation 4.3). Nevertheless, the thermal gradient on the rod was negligible low regardless the used material and was in each case below $\Delta T \leq 0.5\,K$. As the rod is very small in dimension in comparison to the surrounding area and the heat transfer factor was chosen to be very low, the temperature of the rod increased with increasing simulation time.

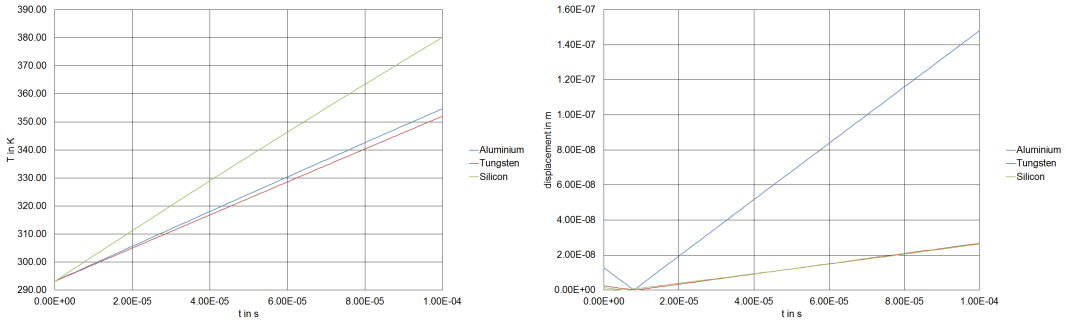

Figure 4.23: Simulation - Conductor Results

$$Q = \int c\vartheta\rho \mathrm{d}V \tag{4.3}$$

where

Q: heat quantity
ϑ: material temperature
ρ: material density
c: heat capacity

All material parameters have been used from the *COMSOL* library as they are proven by the distributor of the software and originate from present day research. The right hand diagram is showing the total displacement of the rod along the y-axis or the depth of the conductor. As aluminum has the highest thermal expansion coefficient from the three used materials, the result was also expected. If the thermal expansion of the aluminum rod is investigated for a temperature increase of about $\Delta T = 5\,K$ starting from a room temperature of $T_{ambient} = 298.15\,K$ as it is expected and measured in the previous experiments, the total displacement of the rod is $\Delta y \approx 1\,nm$. This leads to the assumption that defects which are caused by cracks in conductors have to be of limited width in order to be electrically dependent of thermal expansion. Furthermore friction will cause additional stress in the device whereby the maximum crack width will also be limited. The observed minimum in the right hand figure is caused due to the initial temperature of the simulation and can be neglected as the minimum dwell time of the laser is anyway limited by the laser scanning unit. In the next step of the simulation the rod has been surrounded by silicon substrate and silicon oxide in order to build up a simplified simulation of a real conductor in an integrated circuit.

The basic configuration can be seen in figure 4.24. The total dimensions of

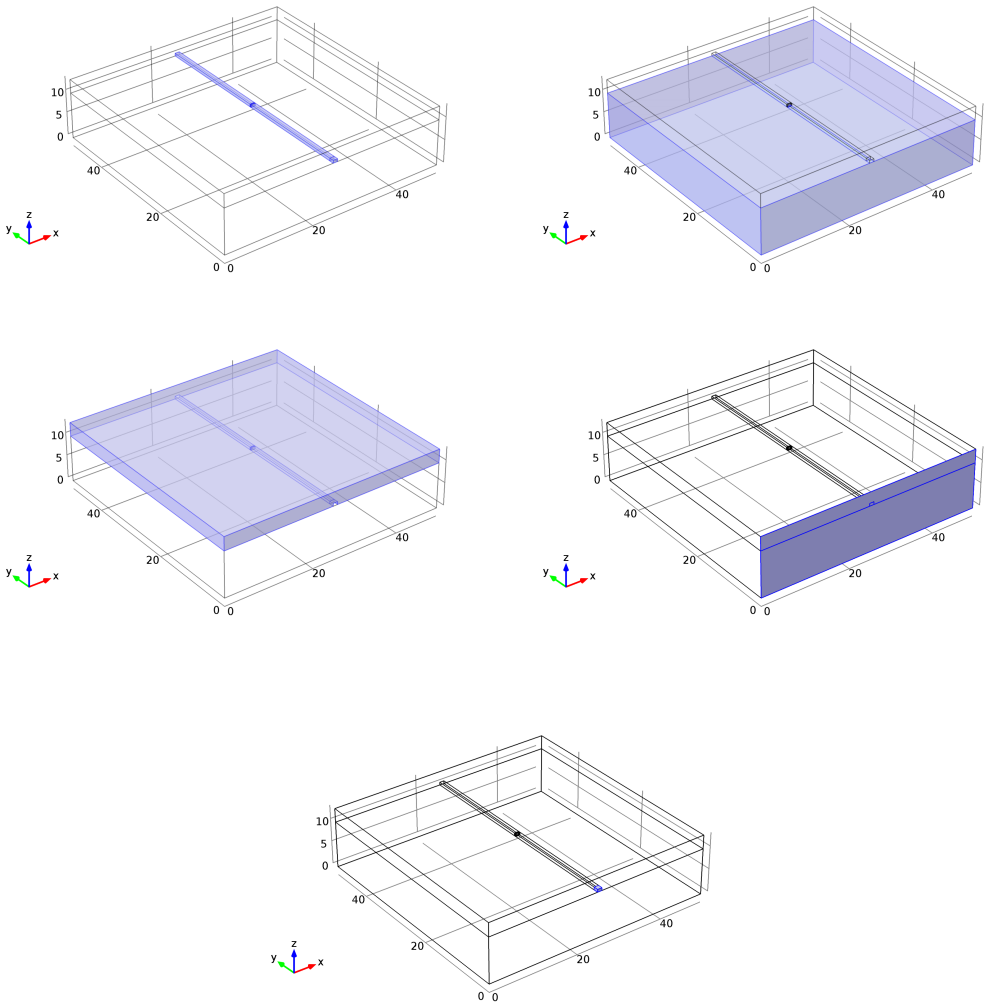

Figure 4.24: Simulation - IC Setup

the setup are $WxHxD = 50x13x50\,\mu m$ whereas the metal rod was made out of aluminum and included a simulated crack which was filled with silicon oxide. This simulation should reveal the temperature increase of the rod whilst stimulated with a $P = 40\,mW$ heat source as well as the mechanical stress on the introduced crack. There have been also used two different simulation methods, namely the *heat transfer module* and the *thermal expansion module*. Both methods lead us to the same results which are shown in figure 4.25. The heat was simulated to be absorbed in a region of the conductor of $WxHxD = 1x0.6x1\,\mu m$. The fixed region was chosen to be

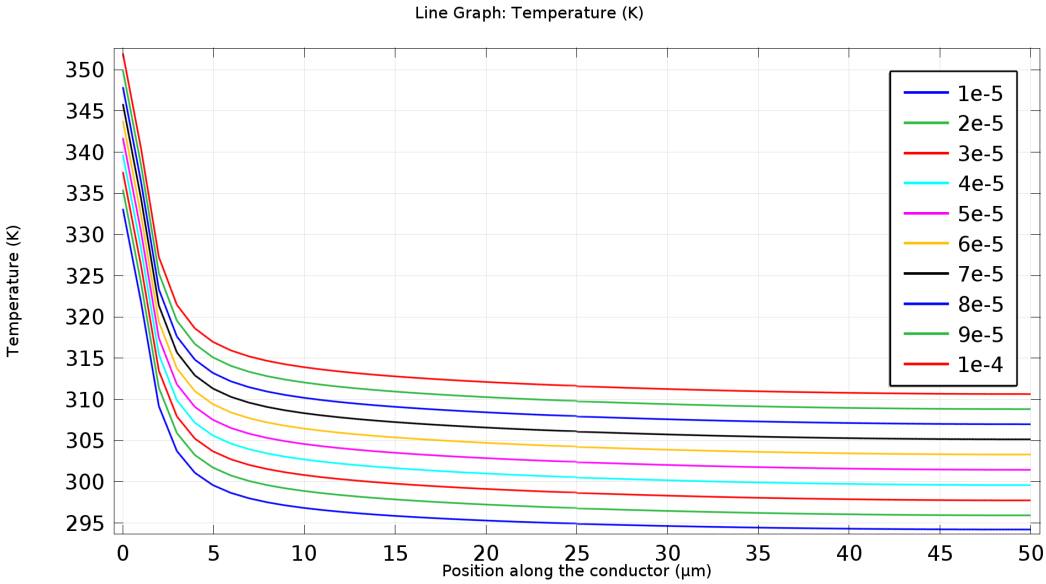

Figure 4.25: Simulation - IC Setup Results

attached directly to the heat source. For this reason the temperature increase nearby the starting position of the rod was definitely higher than expected and resulted from thermal insulation. Also the temperature drop in between the stimulated area is around $\Delta T = 10\,K$ whereby the temperature increase in a distance of $\Delta x = 2\,\mu m$ along the rod nearly meets the already give simulation results from before. It also was expected to see a temperature discontinuity at a length of $l = 25\,\mu m$ due to the introduced crack. As it can bee seen in the figure, the discontinuity due to the silicon oxide in between the aluminum conductor causes no significant temperature drop. The evaluation of the mechanical stress along the discontinuity showed, that the aluminum rod will not be able to cause enough stress on the silicon oxide in order to decrease the gap width. Even if the gap would be filled simply with air, the simulation showed no significant decrease in the gap width. Therefore it is expected that the thermal influence of the laser will not cause a gap of $x = 1\,nm$ to change significantly in its behavior.

4.3 FIB Circuit Line Editing on a Mixed Signal IC

The next experiment was made in order to artificially introduce a crack into a metal line of a test IC. Two different approaches have been used for this purpose. In the first preparation the circuit should be edited with the *normal* cut width of the FIB as it is used in other projects for failure analysis. This experiment was designed to identify the capabilities of the failure

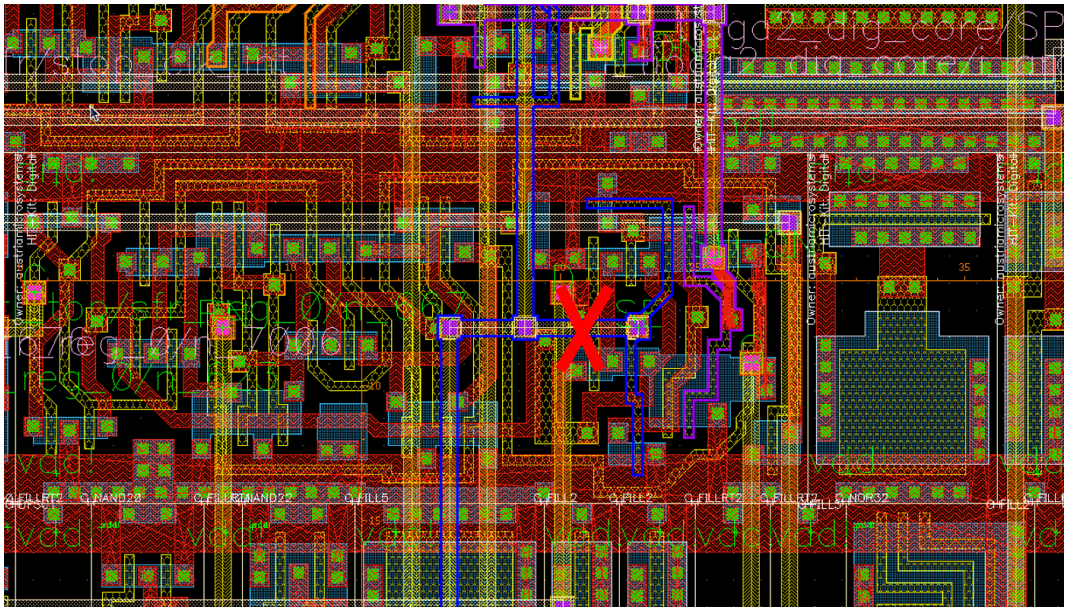

Figure 4.26: Experiment5 - Schematic FIB Modification

identification from the functional tester and to see whether laser stimulation can alternate the failure behavior. In order to get a clear fault behavior it is preferred to cut open either an input or output of a flip flop. During a scan test, the defective connection should lead to a unique failure in the scan test. Figure 4.26 shows the position of the cut in the schematic which is located at the *scan enable* input of a scan flip flop. For this experiment three devices have been used for verification purpose. Before the preparation, the devices have been tested for functionality and even at low/high temperature to ensure that no other fault is present. The cut with the FIB has been made in two steps as it is shown in figure 4.27. At first glance the passivation of the conductor is removed which is shown in the left hand picture. In the next step the conductor is separated by two FIB cuts. The outstanding contrast

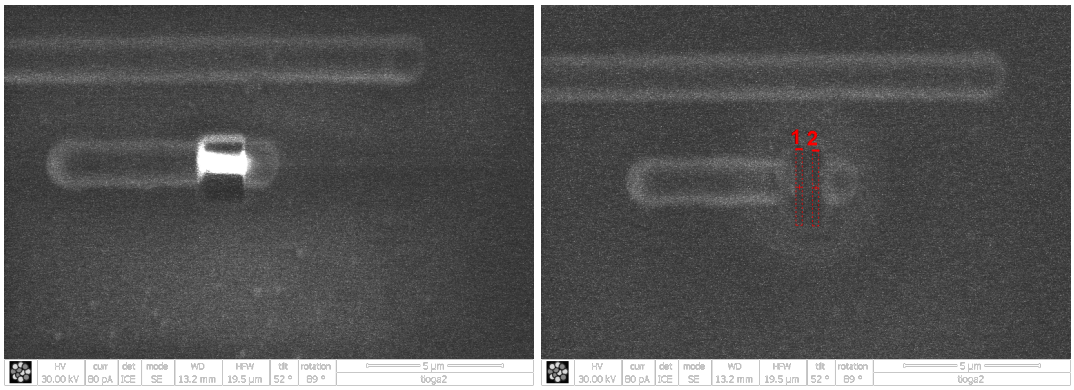

Figure 4.27: Experiment5 - FIB Cut

of the conductor indicates after each FIB cut whether the conductor has been separated. As it can be derived from the scale of the right hand picture in figure 4.27 the cut width is around $x = 200\,nm$. The analysis with the functional tester lead to the following results:

- There occur multiple fails for different scan cells at the device even if we have made only a single FIB preparation.
- The Defect is dependent on light, as the top side of the package is removed. The lower the ambient light, the better the defect identification of the tool.
- Temperature changes the failure identification significantly. Only for low temperatures the defective cell could be isolated in the scan test from other possible defective cells. At higher temperature the failure rate of the pattern does not significantly vary between all occurring scan failures.
- Increasing or decreasing the pattern speed does not change the fault behavior of the device.
- Changing the supply voltage does not change the fault behavior of the device.

Figure 4.28 is showing an example of the failure analysis result of the functional tester. In the left hand picture it can be observed that a single scan chain cell is failing at a much higher rate than other failure cells. By identifying this scan chain cell in the layout, the FIB preparation spot could be clearly identified which is presented in the right hand picture. In the next step the DUT's were mounted in the chamber of the laser scanning unit. All possible settings of the LSM have been used, but the influence of the laser has not been detected in this experiment.

Failures	Chain	Cell	X Origin	Y Origin
106	"co"	1054	8806	3276
72	"co"	1128	6342	676
61	"co"	270	7728	1.4196
61	"co"	907	742	1.3936
60	"co"	840	8316	2.0046
59	"co"	294	7014	1.3546
59	"co"	828	868	1.9266
58	"co"	1131	5586	936
57	"co"	825	8862	1.9526
56	"co"	1140	5586	1196

Figure 4.28: Experiment5 - Results Functional Test

This can be explained by the width of the introduced defect. The thermal influence of the laser is simply not appropriate to cause an alteration of the defect behavior. In the next step three new parts have been taken in order to introduce a defect with the minimum cut width of the FIB at the same position as before. During a small experiment the cut width could be decreased to about $x = 68\,nm$ as it can be observed in figure 4.29.

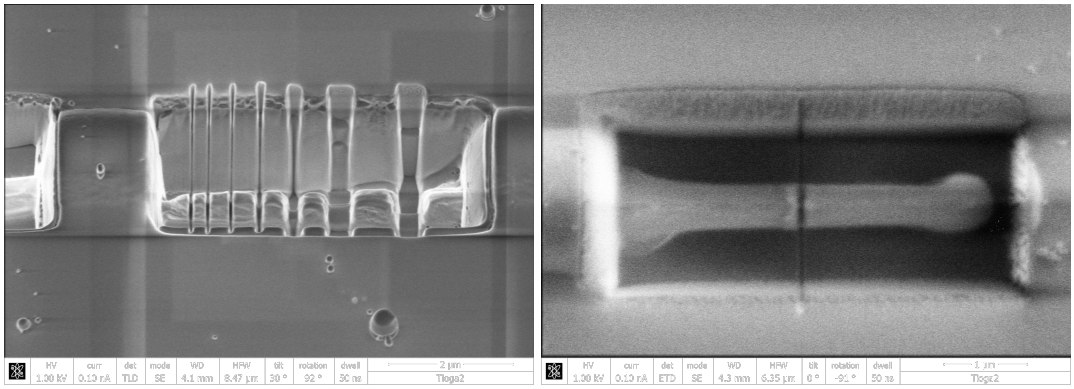

Figure 4.29: Experiment6 - FIB Cut

At first glance the modification of the parts has been controlled by the functional tester:

- Influence of Heat
  - Additional heat increased the amounts of failing cells in the scan chain. The failure localization was not successful for this reason.
  - Cooling the device with a freezer spray resulted in a decrease of failures on the IC.
  - Whilst cooling the device with a freezer spray, the device reached a pass situation during the regaining of room temperature.

- Influence of Light
  - Increase of ambient light resulted into an increase of failing scan cells. Therefore the failure location could not be identified.
  - Whilst decreasing the ambient light, the amount of failures in total has decreased. The FIB prepared cell showed although a clear fail behavior.
- Influence of Pattern Speed
  - The slower the pattern has been made, the less failures have been monitored. Nevertheless a pass/fail event could not be provoked. The pattern speed has been alternated by adjusting the *time scale factor* in the application of the functional tester Teseda v520.
  - A time scale factor $tsf > 1$ leads to a decrease of the scan frequency while a time scale factor $tsf < 1$ leads to an increase of the scan frequency.
    Per default, one period of the scan pattern lasted around $T_{pattern} = 23.88\,ms$ for the DUT. The time scale factor acts linear on the scanning speed. For instance a $tsf = 2$ leads to a scan pattern period of $T_{pattern} = 47.76\,ms$.
- Influence of Supply Voltage
  - Due to the application of an external voltage on the analog block of the DUT, the internal voltage regulator could be overruled.
  - Voltages $VDDA \geq 3.5\,V$ reduced the total amount of failures in the scan chain.
  - $VDDA \geq 3.8\,V$ increased the total amount of failures in the scan chain.
  - For $VDDA < 3.5\,V$ an additional current has been drawn out of the circuit. Except from the introduced voltage sink, the manipulation showed no further results.

As the device has clearly shown a temperature dependency the upcoming experiment included a temperature test where the effect of the freezer spray could be bypassed by the use of a temperature chamber. Figures 4.30 and 4.31 present that under a certain combination of ambient temperature and pattern speed, the device is passing the functional test, whereas the functional test fails for other test settings. The most probable configuration for the device to pass was for $T = 10 \ldots 20\,°C$ and a time scale factor $tsf > 3$. As it has been described in the chapters before, there exist several possibilities of why a pass/fail event has been created.

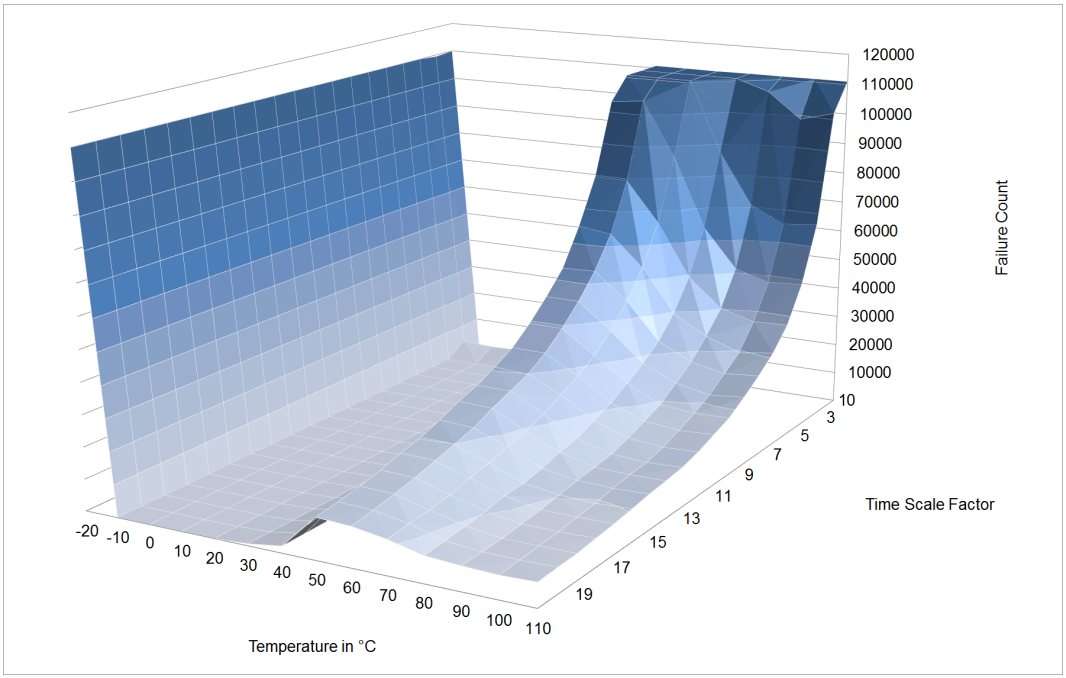

Figure 4.30: Experiment6 - Results Functional Test 1

- The influence of the supply voltage on the pass/fail event has not been noticed.
- The temperature of $T = 10\,°C$ will most probably not cause mechanical stress in the test structure. Even at higher temperatures where we would expect mechanical stress, thermal expansion doesn't decrease the width of the open which could alternate the failure behavior of the device.
- Capacitive coupling can also be excluded as a coupling effect would be expected four higher pattern frequencies only.
- The influence of ambient light was minimized, as the DUT's have been placed in the temperature chamber.

The most probable cause of the observed pass/fail event is electron tunneling over the introduced cut in the conductor. Jr., 2011 states in "Beam-Based Defect Localization Techniques" cite: *"CMOS ICs with open conductor lines may function at low to moderate $f < 50\,kHz$ frequencies. The reason for this functionality is that significant quantum mechanical electron tunneling across the open can transport enough charge at low frequencies to maintain functionality. The maximum operating speed depends upon the nature of the open."* As soon as the

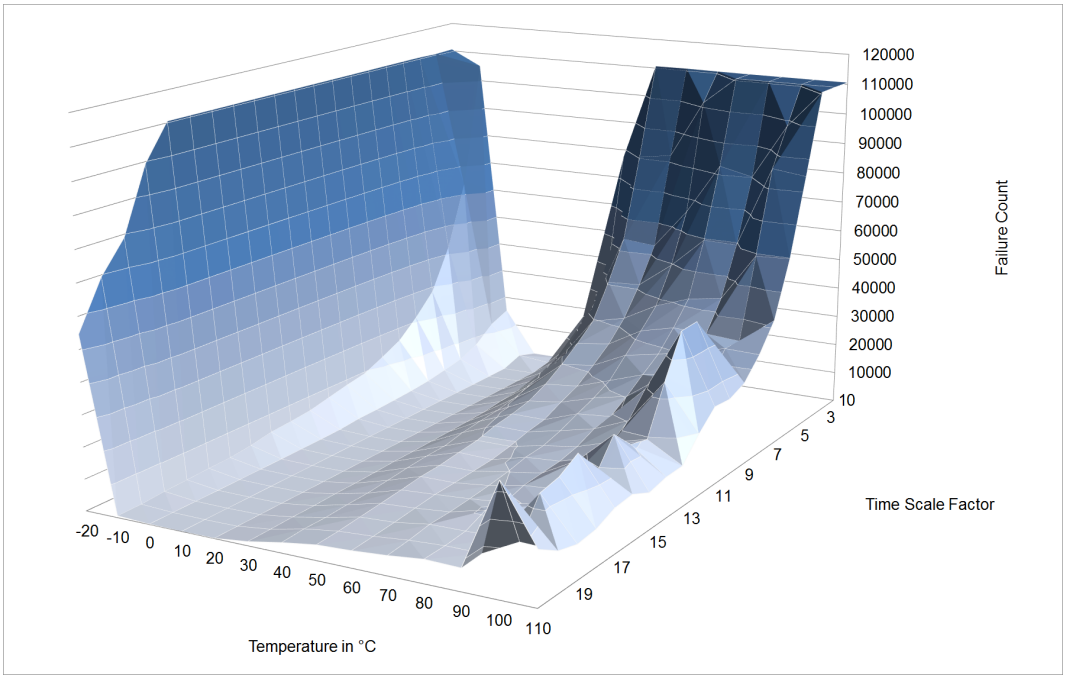

Figure 4.31: Experiment6 - Results Functional Test 2

DUT's leave the vacuum chamber of the FIB the open contact will instantly oxidate which leads to the creation of silicon oxide at the failure spot. Silicon oxide is a very good insulator which additionally supports the explanation for tunneling effects as the conductor has been removed completely during the FIB preparation process. In the following experiment the DUT's with minimal cut width have been tested in combination with the laser scanning microscope. Unfortunately the thermochuck which is installed in the LSM chamber is not suitable for cooling purposes. Several attempts to precool the device before DALS analysis have failed. Nevertheless an analysis with the DALS setup has been carried out, which showed the expected results, that no pass/fail event could be created. This experiment has shown how important it is to check the functionality of a device under each possible setup configuration. The pass/fail event occurred in between a rather narrow *temperature window* which indicates the importance of small parameter changes.

4.4 Analysis of a Mixed Signal IC

A series of experiments with a device out of production should highlight the application of failure analysis with DALS. The devices in use showed a pass behavior for a certain range of supply voltage and ambient temperature whereas it failed for other test conditions. For analysis purpose the package of the devices has been removed from the top side in order to be able to stimulate the device with the infrared laser of the LSM. The functional test has been made with an in house developed tester system called *BMS - Butterfly Measurement System*. The programmable analog and digital in,- and outputs allow the implementation of all thinkable test conditions for the DUT. Furthermore it is very easy to control the most important parameters just as:

- Supply Voltage
- Pattern Speed
- Pattern Length
- Signal Amplitude

The first test should evaluate the temperature dependence of the device. For this reason the DUT has been heated up with a hand oven while it was tested with the BMS. The temperature of the DUT has been measured with a built in thermostat of the hand oven. Of course the temperature of the DUT won't exactly comply with the setup temperature of the hand oven, but it is accurate enough to predefine the test condition for DALS. The dependency of the pass/fail region in dependence of the temperature is presented in table 4.3.

V_{BAT} V	T $^{\circ}C$
1.90	25
1.95	50
2.00	60
2.05	70
2.10	80

Table 4.3: Experiment7 - Test Condition for Fail Behavior

A dependency of the pattern failure regarding any other pattern related

parameter could not be monitored in the ATE environment in the first place. In the next step the DUT has been placed in the Phemos 1000 chamber while the tester was connected to the DUT via an interface board. The laser scanning unit was setup in a way that the laser movement was triggered by an external signal *LOOP TRIGGER* from the functional tester and the pass/fail evaluation result was connected to the *TESTER SIGNAL* input. The operation mode of the LSM was chosen to be *Latch A*. Figure 4.32 is showing

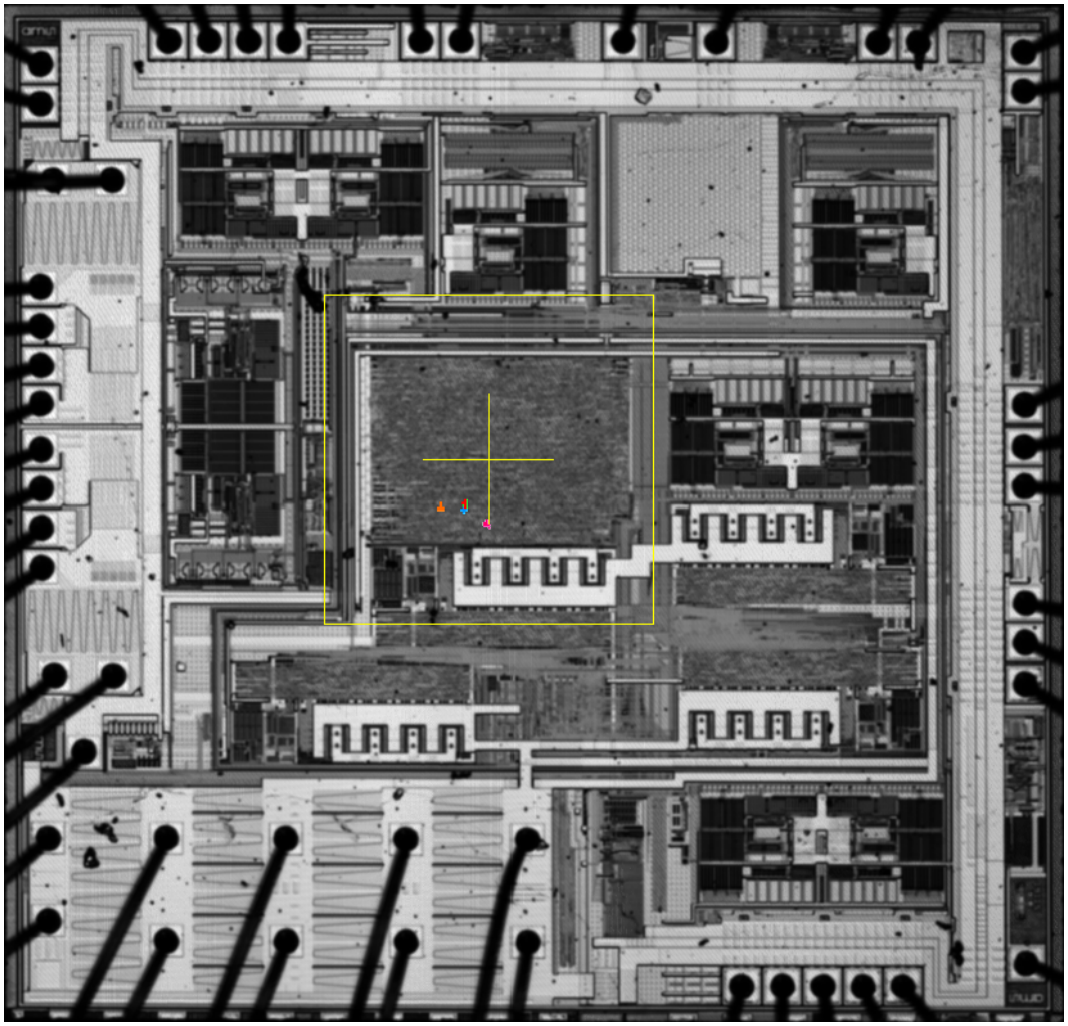

Figure 4.32: Experiment7 - DALS Result 5x ©amsAG

the first analysis result with DALS. As it was known from the functional test fails, the main area of interest has been the digital block of the mixed

signal IC therefore the scan area of the laser has been setup to decrease the overall analysis time. The following settings have been varied:

- Laser Power
- Pattern Speed
- Scan Direction
- Laser Magnification
- Supply Voltage

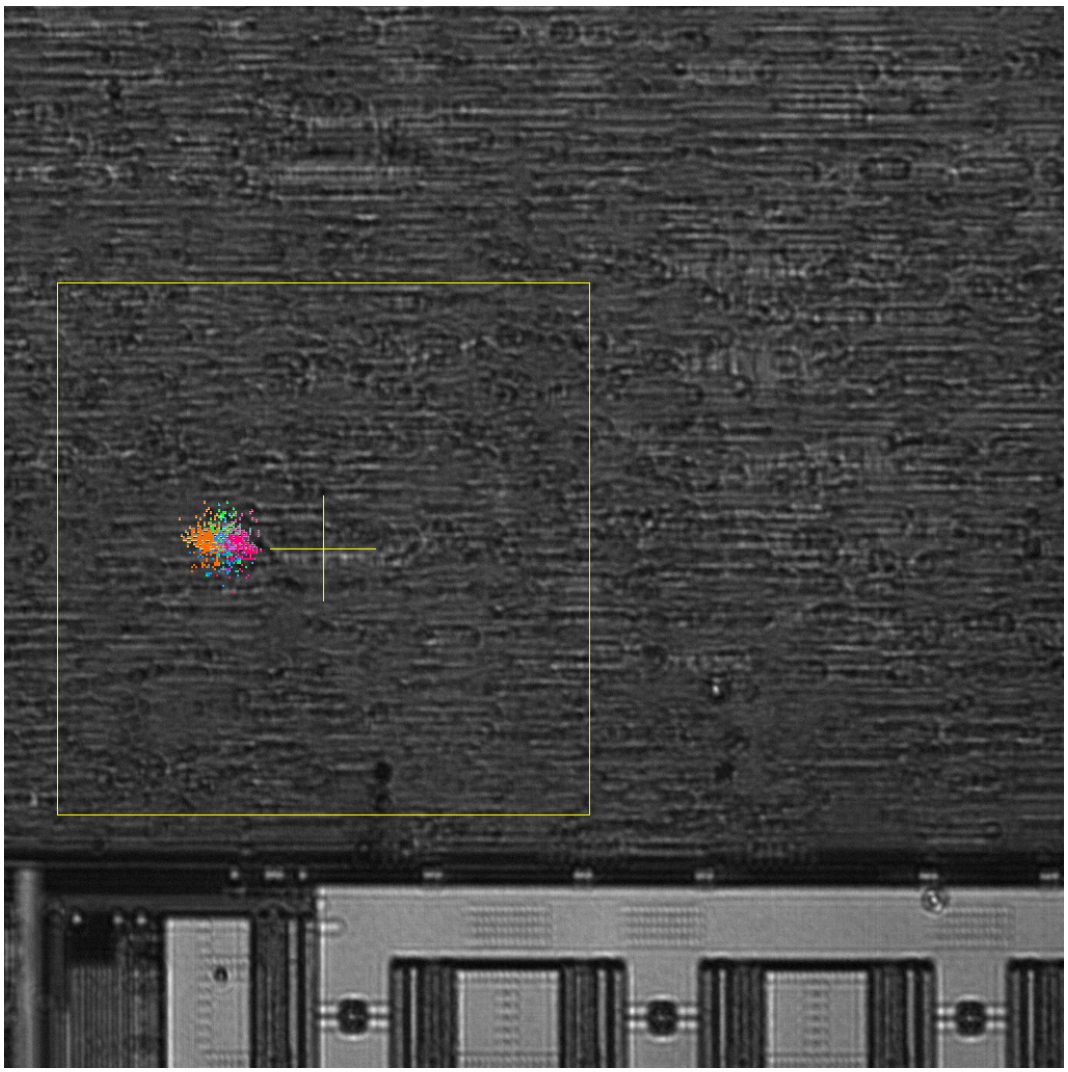

Figure 4.33: Experiment7 - DALS Result 51x ©amsAG

In total 4 possible defect spots have been identified which showed a clear dependency on the scanning direction of the laser scanning unit. In order to work out more detail and to overcome the limited resolution of the camera, the lens has been changed to *51x OBIRCH*. Figure 4.33 is showing the analysis result. Again the same parameters as before have been alternated but this time the failure spot concentrated on a single area of the IC.

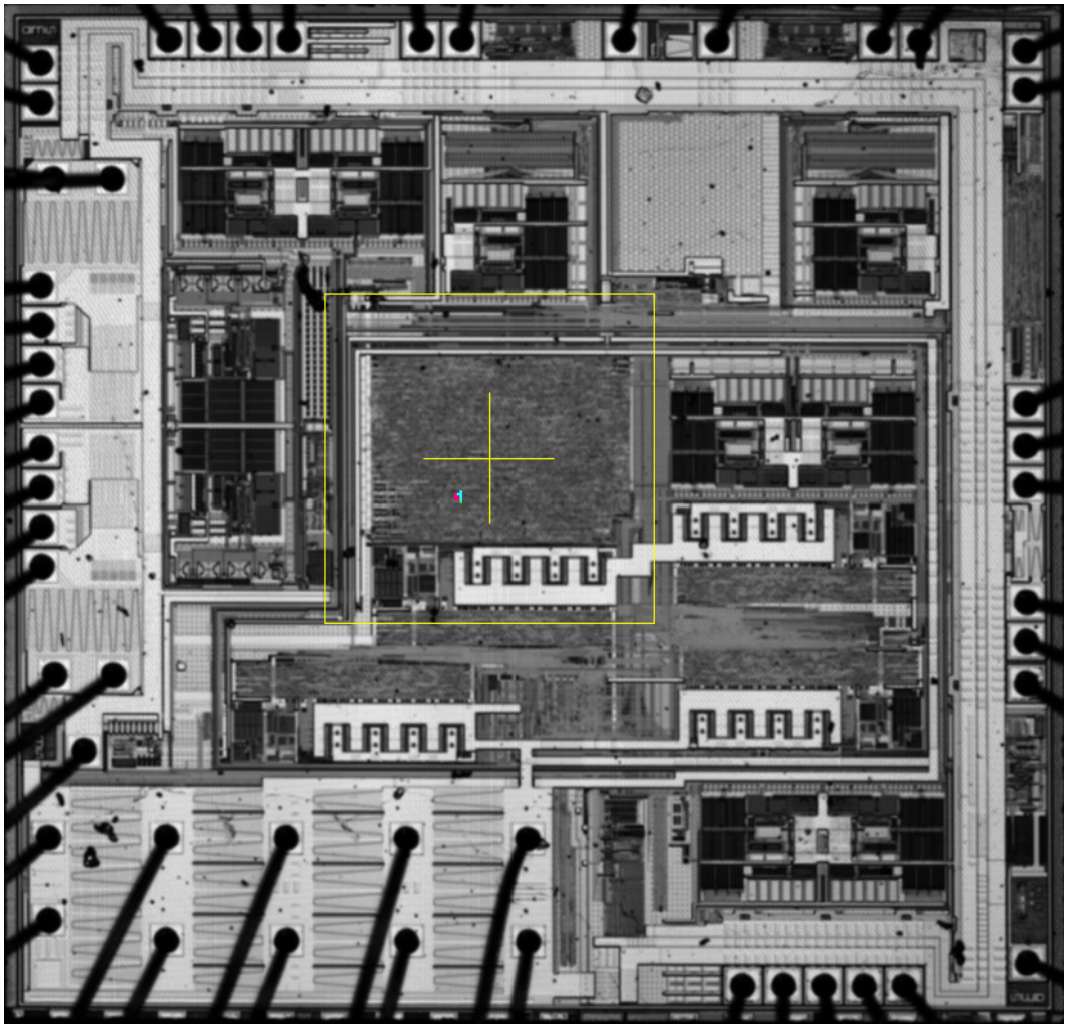

Figure 4.34: Experiment7 - DALS Result under ΔT ©amsAG

The result is most probably disrupted by a misalignment of the laser scanning unit as the functional test fail only occurred for a single cell in the digital block. Therefore the results for the scan direction angles of 90 ° and

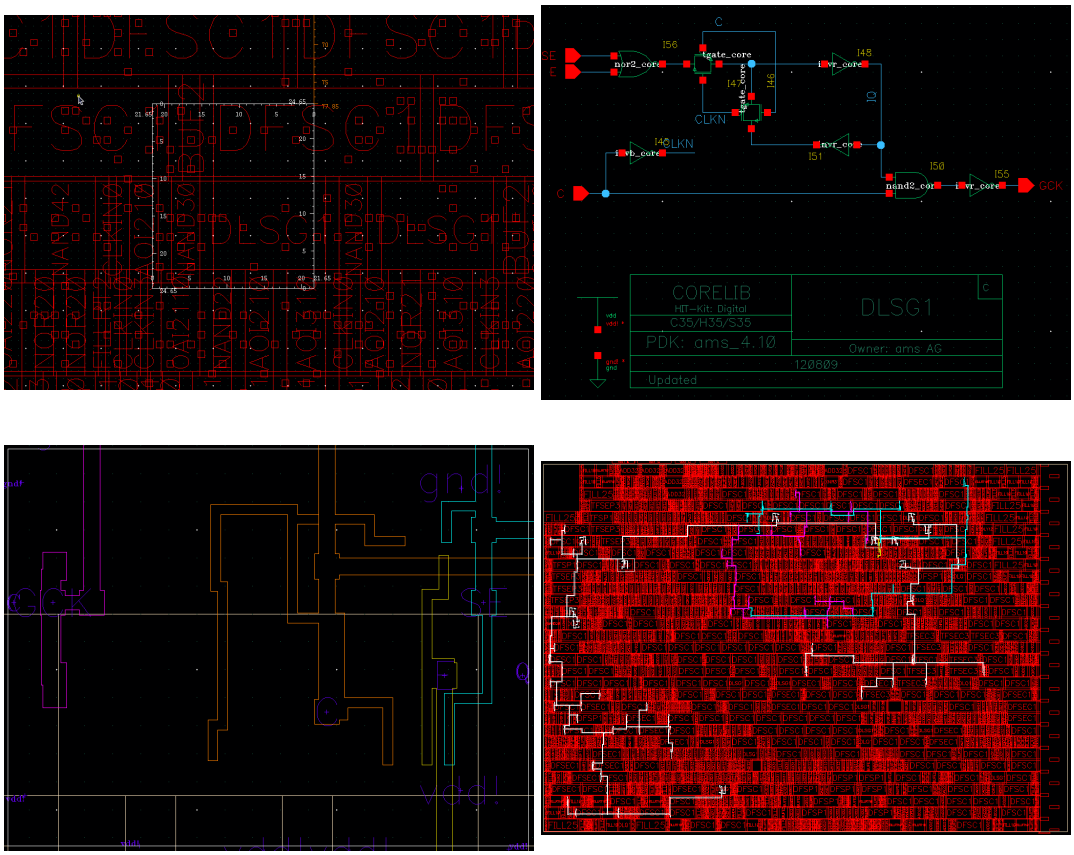

Figure 4.35: Experiment7 - DALS Spot Analysis ©amsAG

270 ° are faulty. Furthermore the physical rotation of the device did not reveal the same results as for the software based approach of changing the scanning direction. Before the failure spots have been analyzed in the schematic and layout editor tools, the dependency on the ambient test temperature has been checked by applying heat with the thermochuck. Figure 4.34 shows the DALS analysis results for ambient temperatures of $T = 40,\ 50,\ 60$ and $70\,°C$. In order to create the pass/fail events the supply voltage had to be changed according to Table 4.3. For $T = 70\,°C$ the failure mode could not be changed from pass to fail regardless the setup configuration. The failing pattern lead to the identification of a clock gating cell. Just as figure 4.35 is highlighting, the only electrical connection between the cell identified by the failing scan pattern and the marked cell by the use of DALS is the clock line. Simulation results in Cadence have not shown a correlation between both cells. Therefore the next experiment should prove

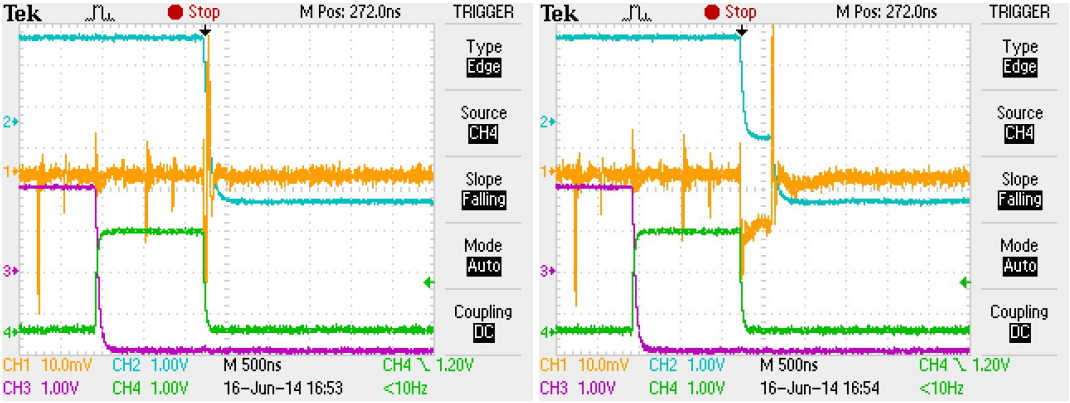

Figure 4.36: Experiment8 - Dynamic IDD Monitoring

the validity of the found DALS spot and reveal at the same time possible timing problems on the clock line. Before the test setup has been changed, a simple IDDQ test should reveal proper functionality of the DUT. Figure 4.36 is showing the analysis results. The used configuration of the channels from the oscilloscope is:

$$\begin{aligned} CH1 &\quad I_{DD} \\ CH2 &\quad Reset \\ CH3 &\quad Scan\ Input \\ CH4 &\quad Pattern\ Indicator \end{aligned}$$

It has been clearly observed that at the end of the indicator signal for the failing pattern the current consumption shows an unintended spike. The spike even varies in time. In collaboration with the designer of the device it has been worked out that the spike is resulting due to a load condition between the internal voltage reference of the device and the supply from the functional tester. This issue is not the root cause for the failing pattern, but it underlines the importance of monitoring even the simplest parameters just as the supply current. In order to observe a possible pattern dependency on the operation parameters a program has been designed which is looping all available test parameters. During multiple test runs it turned out that the pass/fail behavior is not only dependent on the supply voltage but also on the pattern speed as it can be seen in figure 4.37. This experiment shows the importance of failure verification before DALS analysis is conducted. The variation of pattern speed and supply voltage, lead to the identification of a clear pass/fail border. This experiments have been made with a reduced pattern, as the scanning time could be decreased significantly. To verify the validity of the result, the same parameter variation has been conducted

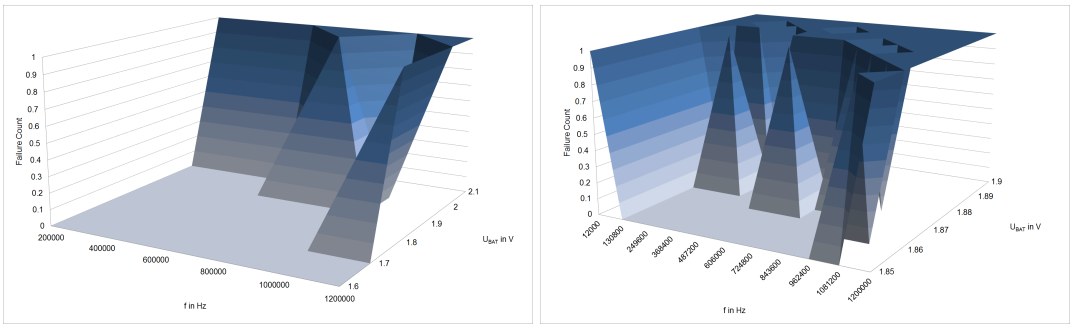

Figure 4.37: Experiment9 - Analysis Reduced Pattern

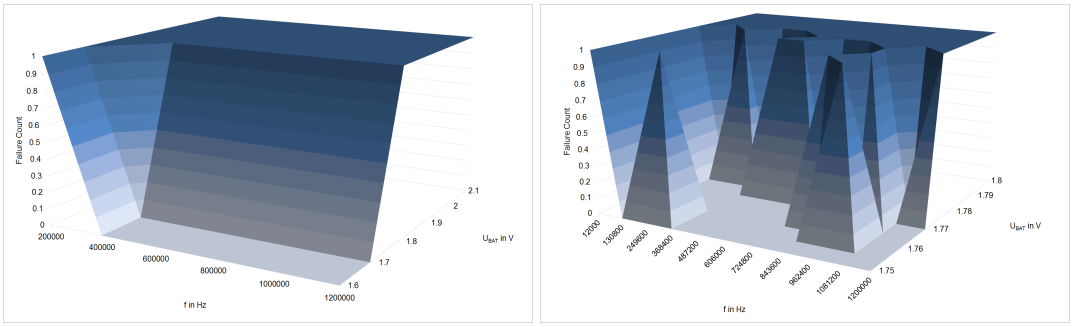

Figure 4.38: Experiment9 - Analysis Full Pattern

with the full and power aware scan test pattern of the device. With the power aware scan pattern no failure could be reproduced. Figure 4.38 is showing the analysis results for the full scan pattern. The pass/fail border has not been observed for the same setup parameters as it can be seen for the reduced scan test pattern. Nevertheless the same faults of the scan chain could be observed. In order to verify the test results it is mandatory to prove the detected parameter dependencies for at least three parts. This example confirmed that the defect stimulation is dependent on application parameters like:

- Pattern Speed
- Supply Voltage
- Pattern Type

as it has been described in related work like from Chunlei, L. Zhai, Motohiko, Ma, et al., 2010, Quah et al., 2006 and Burmer, Brillert, and Qian, 2007.

4.5 Analog parameter observation with DALS

The biggest challenge for analog DALS is to find a proper signal which can be monitored externally for instance with an oscilloscope and is at the same time dependent on the stimulation of the infrared laser. The measurement itself must not affect the behavior of the DUT. Furthermore the monitored parameter must be linked somehow to the device defect and consist of a unique identification parameter. This unique identifier might be:

- Amplitude
- Frequency/Period
- Rise/Fall Time
- Spike/Edge

which allows automated evaluation with the measurement equipment. Just as before, the evaluation result of the unique identifier is converted into a pass/fail signal which is then applied to the input of the *TESTER SIGNAL* of the synchronization unit. The pixel movement can be triggered by applying an external clock with a frequency generator to *LOOP TRIGGER* or by using the internal clock. This approach will lead the same analysis capabilities as it has been previously presented. The DUT in the following experiment showed some kind of reset behavior which lead to a faulty signal at one of the outputs. The faulty signal was periodic and could be described as an edge from HIGH to ZERO and vice versa. Lab measurements have shown, that the fault was dependent on several parameters:

- Supply Voltage
- Current Load
- Ambient Temperature

Under normal operating conditions, an ambient temperature of $T = 25\,^{\circ}C$ and without load, the edge could be observed at a period of $t = 550\,ms$. If the device was cooled down, the period of the failure increased, while the period decreased with increasing ambient temperature as it can be observed in figure 4.39. This failure behavior can be used as an unique identifier. Many oscilloscopes have the ability to create a pass/fail evaluation signal by using an external output. In figure 4.39 the observed period at ambient temperature varied in between a time range of $-40 \leq \Delta t \leq 40\,ms$. Therefore the trigger output of the oscilloscope can be set to HIGH if the period was not between $510 \leq t \leq 590\,ms$ and could therefore be used as a pass/fail indicator.

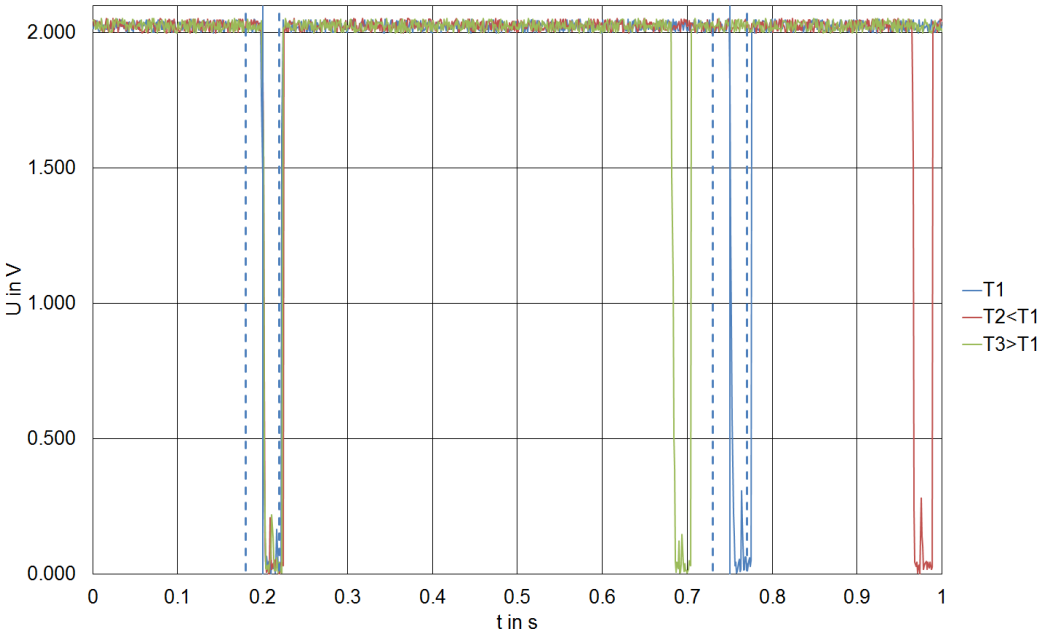

Figure 4.39: Experiment10 - Analog DALS Unique Identifier

5 Best Practice for DALS

Summarizing the findings of the experiments and the simulations, this chapter will conclude this thesis. The described analysis setup will consist of the functional tester *TESEDA v520* as well as the LSM *HAMAMATSU Phemos 1000* with a $\lambda = 1300\,nm$ infrared laser and $P_{total} = 100\,mW$ laser power. The analysis itself will cope with a defect in the digital region of the device. As it already has been shown in figure 3.1 the best way to approach defect location is made step by step in combination with simple considerations.

5.1 Verification

Before hurrying into the defect analysis itself it is mandatory to collect as much data about the reported failure as possible. As not only failures in the production, but also wrong handling, processing as well as the wrong application itself can cause damaging to IC's this starting information already includes very valuable information. This information gathering process is also known as failure anamnesis or error history. Possible questions are:

- Is a single part/lot/date code affected?
- Is the failure reproducible on site?
- Have there already been made experiments with defective devices?
- If the parts originate from a reel, a tube or simply a wafer, is there a pattern for the defective devices?
- At which percentage is the failure observed?
- Is it the first time the failure has been observed?
- Have the devices been stored before use?

Regardless the nature and origin of the failure, the next step is to reproduce the failure reported by the customer or your coworker on your own in a controlled lab condition. The data sheet of a device always includes the standard setup as well as the assured operating conditions for a device.

- Check the test setup with a fully function part in order to verify testing capability.
- Start off with testing the defective device.
- Note what parameters are failing.
- Has there been a history on the device?

If the failure has been reconstructed, does it show any dependency on an operating parameter? Again, the data sheet includes the assured operating ranges from production. The following parameters are indicators of which parameters might be useful to take a look at.

- Supply Voltage
- Load Condition
- Operating Mode / Test Mode
- Operating Speed
- Scan Pattern Type
- Ambient Temperature
- Ambient Light

Soft defects which have been localized with DALS have clearly shown a dependency on at least one of the above mentioned parameters during the presented experiments. It is mandatory to know precisely where the pass/fail transitions appear. For this purpose some parameter analyzers and functional testers have the ability to create Shmoo plots. During the DALS analysis, the device should operate as close as possible to the border where it changes it's behavior from pass to fail or vice versa as the power of the used infrared laser and therefore the capability of influencing the device's behavior is limited. This is one of the most critical points during the failure localization with DALS as it has been shown in section 4.4.

5.2 Preparation

The identified locations of possible defects with DALS will not automatically lead to conclusions about the defect's origin. It is therefore mandatory to prepare access to layout and schematic files of the analyzed device.

- Get access to the schematic and layout files of the project.
- Inform about the failing parameter from the previous measurements.
- Can the failing parameter be monitored somehow easier?
- Are there test points available or do we rely on the available outputs?
- Can we delimit the possible defect area from the failing parameter?

If there already exists a project for the device on the functional tester it can be used with only two restrictions:

- Pass/Fail Evaluation Signal
  Somehow the evaluation setup of the device must tell the LSM when laser stimulation has caused a change in the evaluation result. For this reason the pass/fail evaluation signal has to be connected to the *TESTER SIGNAL* input of the *HAMAMATSU Tester Signal I/F Box*. If the device evaluation has passed, the signal must stay at $A = 0\,V$ whereas the signal will indicate a failure if $A = 2\,V$. The signal itself ideally has the shape of a rectangular pulse with a duration of $100\,ns \leq t \leq 1\,\mu s$ and an amplitude of $A = 2\,V$. The duration of the failure evaluation signal has to be limited or reset if the *Move Pixel Signal* is set to HIGH. This will prevent that the evaluation result from the actual pixel will be merged to it's neighboring pixel in the scan direction of the laser.
- Move Laser Signal
  If the test has been completed at least once for a single pixel of the LSM, the tester needs to instruct the LSM to move to the next pixel. The duration of the failure evaluation is determining the signal period for the move pixel signal. Ideally it is a rectangular pulse with a width of $100\,ns \leq t \leq 1\,\mu s$ and an amplitude of $A = 2\,V$. The signal frequency is limited to $f = 8\,kHz$ due to the input synchronization unit of the LSM. The signal has to be connected to the *LOOP TRIGGER* input of the *HAMAMATSU Tester Signal I/F Box*.

otherwise the following steps will show how a set up a project with the functional tester *TESEDA v520*. There are at least four files needed to create the project.

- DEF - Design Exchange Format file
  Basically there is only one *.DEF* file necessary which is describing the used standard cells and macros as well as their locations and connections in the integrated circuit.
- LEF - Layout Exchange Format file
  Standard cells, macros and project related objects have to be exported as *.LEF* files. They include the dimensions as well as definitions for layers, vias and other process relevant objects.
- STIL pattern
  The test pattern needs to be provided in a special format: *write_patterns* ${*RESULTS_DIR*}/${*DESIGN_NAME*}*.stil -replace -internal -format stil99*
  Additionally it would be neat to include commands into the test pattern to put the DUT into the correct test mode. Most devices can be controlled via *I2C* or *SPI* commands. Of course it is also possible to create a separate pattern for the test mode commands. With this configuration the device can be initialized once instead of each time the pattern is called. The minimum length for the test pattern is defined by the maximum frequency of the LSM. Therefore the pattern must have a length of at least $t = 125\,\mu s$. If the length is nevertheless smaller, the pattern can be called multiple times before the laser is moved again, or placeholders with no evaluation purpose are added to the used test pattern. There exist several types of test patterns which can be created problem related.
  - Full Pattern
    The full pattern will cover all scan cells of the device. As the pattern length is dependent on the amount of scan cells in the IC, the application of the pattern itself can take quite a time. Furthermore if the fault can not be restricted to a certain area, it is recommended to always use the full test patterns.
  - Reduced Pattern
    Accordingly to the area of interest, the test pattern can be reduced to a minimum set of sequences. In this combination only the scan cells of interest will be evaluated in the functional test.

– Power Aware Pattern
  Based on the logic operations of the device during the change from one sequence to another, a specific amount of gates is switched. During the build of the test pattern it is possible to choose to build a power aware test pattern where the amount of gates which are switching at the same time is minimized. Therefore the total power dissipation of the device will be reduced.

If the pattern has been created in the *STIL* format it will be necessary to include additional sequences into the test pattern which do not contribute to the pass/fail evaluation directly, but which are needed for synchronization with the LSM. The next line is showing the code example of the last capture-cycle in a *STIL* formated pattern.

```
Call "capture_MODE_CSCL" {
  "_pi"=0101; "_po"=L; }
"end 175 unload": Call "load_unload" {
  "LINL"=LHXLHLLHLHHHHLLLLLLLLLLHHHHHHLLLLLLLLL...
  LHHHXLLHLLLLLHLLHHLLLLLLLLHLLHHLLLLLLHHLLLLLL...
  LLLLLLLLLLLLLLLLLLHHHHHLHHLLLLLLLLLLLLLLLLLHXLL...
  LLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLLL...
  LLLLLHHLHHHHHLLHLLLLLLLLLLLLLLLHHHLLHHHHHHHHH...
  LLL; }
```

Synchronization sequences must be inserted before the last "}" of the pattern. By copying the last capture cycle and replacing both possible evaluation results *H* and *L* with a series of *X*, the synchronization sequences can be added without further effort.

```
Call "capture_MODE_CSCL" {
  "_pi"=0101; "_po"=L; }
"end 175 unload": Call "load_unload" {
  "LINL"=XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX...
  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX...
  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX...
  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX...
  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX...
  XXXXXX; }
```

The synchronization sequences will furthermore ensure, that the pass/-fail evaluation results won't be applied to the wrong pixel stimulated by the LSM. It is recommended to add at least 10 sequences.

- pinout list
  The pinout list must have the format provided in the next code example and must be stored as a *.csv* file. The amount of pins is directly defined by the scan pattern file. The names in the *.csv* list must match those of the scan pattern file. The first entry is denoting the pins name, the second column entries denote the pins which have to be used on the functional tester *TESEDA v520*. It is recommended to use only *DATA_XXX* pins as they provide sufficient accuracy for each necessary scan signal.

```
V520
"scantest",     J1-U33
"scandi",       J2-J57
"sclk",         J2-A49
"scanmode",     J2-J49
"por",          J2-J21
"scando",       J2-G27
```

The *.DEF* and *.LEF* files can be exported with all possible layout editors as they are very common exchange file formats. *CADENCE Virtuoso* is offering this option for instance with the *Encounter Tool*. It is highly recommended to work in close cooperation with the designer of the product as he is familiar with all the used cells in the IC. In the last steps of the preparation the project files will be created for the functional Tester. The *TESEDA Work Bench* is used to run the test patterns and capture the device responses. To run the project properly it is recommended to take care of the following action points

- Create New Project, Import STIL, Rename the Scan Pattern properly, Import Pin Map, Add Pin Voltage Configuration, Add Power Configuration, Connect to Tester
- Compile, Download, Run, Run Mode: Failure Capture, Set Triggers
  If synchronization sequences have been added to the STIL pattern, a Trigger of choice can be set to one of the available pins:
  - Trigger1: $J1 - A41$
  - Trigger2: $J2 - W41$
  - Trigger3: $J2 - W47$
  - Trigger4: $J1 - A47$

  It is recommended to set the trigger to the third last sequence of the test pattern. This signal will be used to trigger the movement of the

laser. Therefore the signal has to be connected to the *LOOP TRIGGER* input.

The functional tester also includes a global fail signal which is always activated. If any test is failing during operation, pin $J1 - C47 \ldots GLBL\_FAIL$ is set to HIGH. In between the real failure of the pattern and its indication about three pattern cycles can pass by. With the *TESEDA Diagnostics Manager* the failing sequences of the functional test can be analyzed. The tool offers

- Brocken Scan Chain Analyzer
  This tool allows to test whether the scan chain is operating as intended. The stuck at failure model is used to identify possible defects.
- Top Failing Cell Report
  From the response of the device stimulation an analysis can reveal the scan cell with the most failing parameters.

To make use of this functions, the following points should have been covered in the Diagnostics Manager:

- Create New Project, Add *.LEF* and *.DEF* files
- Run Check Files Now
  The function is very useful to check if a macro or a process related object is missing in the definitions of the *.DEF* or *.LEF* files of the project. There will be a clear indicator for the missing object.
- Add STIL, Resolve Scan Chains
  If naming conventions between the imported design and the test pattern are not met, the function *Resolve Scan Chains* or *Advanced Scan Chain Resolver* is very useful to get rid of wrong definitions without the effort of manual file editing.

The preparations can be concluded by placing the tester and the DUT with its test setup board into the Phemos chamber and connecting the *Pass/Fail Evaluation Signal* with *TESTER SIGNAL* input and *Move Laser Signal* with *LOOP TRIGGER* input of the *HAMAMATSU Tester Signal I/F Box* as it can be seen in figure 5.1.

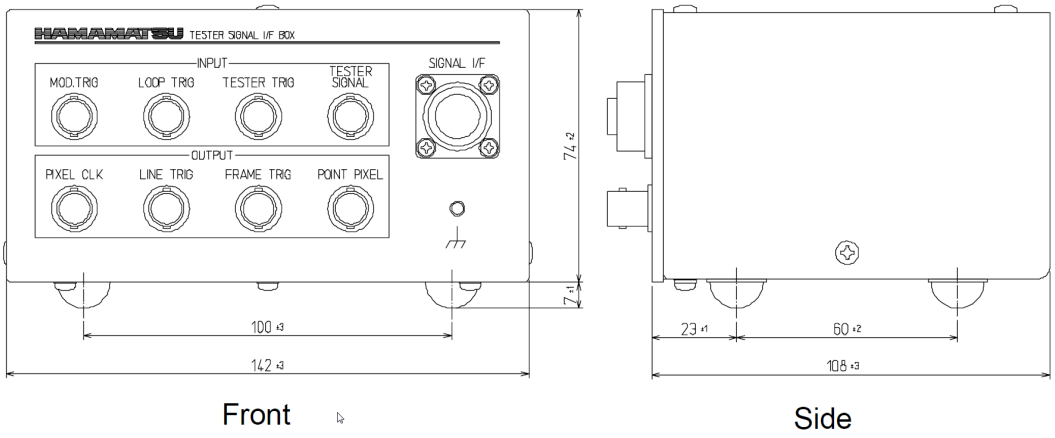

Figure 5.1: Tester Signal I/F Box

Before starting off the measurements make sure to avoid measurement failures like:

- Ground Loops
- Capacitive and inductive loading due to long wires
- Weak connections in the signal path
- Couplings from external power supplies or personal computers
- Drill cables to minimize inductive area
- Avoid stacking measurement devices over each other
- Try to place the DUT as close as possible to the thermochuck to decrease the thermal capacitance

5.3 Analysis

The *HAMAMATSU SemiShop* software is shown in figure 5.2 The first thing to do is to check whether the device is properly placed under the LSM. For this reason activate the menu *LASER* in the tool bar and then navigate to the *Reso* tab in the menu list and choose the following settings

- Scan Mode: Normal
- Resolution: 512x512px
- Zoom: 1x
- Speed: 8s
- Direction: Normal

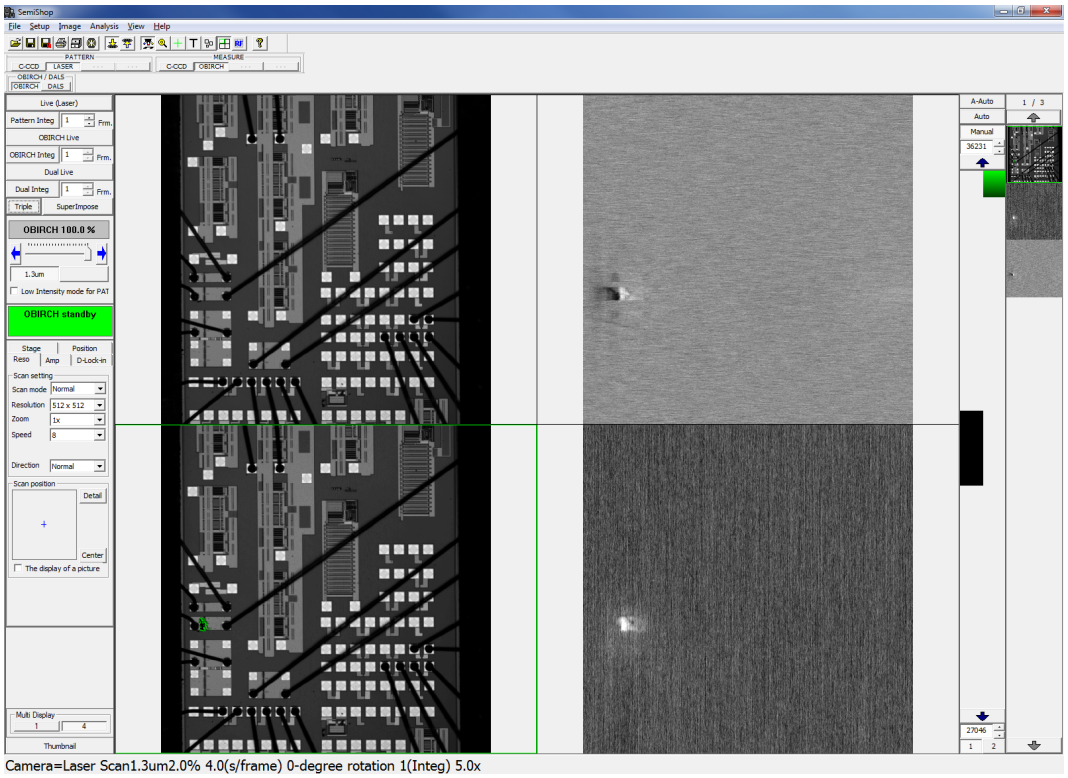

Figure 5.2: HAMAMATSU SemiShop Software

Record a simple image with the *Live (Laser)* or the *Pattern Integrator*. A laser power of $P = 2 \ldots 5\,\%$ is sufficient to record a pattern image. Adjust the stage *X, Y, Z - Coordinate settings* in a way that the recorded picture appears focused. The point of focus is reached where the image appears in maximum contrast and brightness without putting the laser power to a higher setting than recommended. If the lenses are changed, the stage has to be adjusted again, as the point of focus and the working distance for each lens is different. Furthermore record the first picture either with the $0.8x$ or $5x$ lens depending on the size of the DUT. This settings as well as the positioning of the LSM can be adjusted and accessed in the *Stage* tab in the menu list. To get a better overview of the recorded images and measurements change the amount of images to 4 in the *Multi Display* tab located at the lower left bottom of the SemiShop window. Of course the stage can be also controlled manually at the input panel located at the front of the Phemos chamber.

DALS analysis options can be activated either by pressing the DALS button in the tool bar, or by navigating through *Setup→Laser Scan Controller Properties→Capture→DALS Image*. After activating the DALS scan mode, the menu *DALS* will appear in the menu list on the left hand side of the software. By activating this menu the following settings have to be applied:

- Synchronization
  The option *External* ensures that the laser is inly moved when the input of *LOOP TRIGGER* is set to HIGH. Furthermore the termination can be adjusted in the software. When using the functional tester TESEDA v520 it has been shown that the *HIGH Z* termination has to be used.
- DALS mode
  The setting of the DALS mode will determinate how the pass/fail evaluation signal will be evaluated for each pixel. For the best use system *Latch A* mode is recommended.
- Trigger level
  The trigger level adjusts the voltage of the signal comparator and decides whether the rising or falling edge of a input signal is used for control purpose. $1.5\,V+$ denotes that the rising edge of the input signal is observed and identified as HIGH if it exceeds $A = 1.5\,V$.
- External Output
  The external output settings must not be changed. They could be used to indicate the position of the laser with the *POINT PIXEL* output.

Note: As the positioning of the laser is now dependent on the external trigger signal, even the *Live (Laser)* measurement option will only record an image if the external trigger is active. To record a simple image, it is recommended to toggle the synchronization mode in the *DALS* menu accordingly between *External* and *Internal*. After activating the external synchronization the evaluation of the DUT with the functional tester has to be started. Then a DALS image can be recorded by pressing either the menu button *DALS Live* or *DALS Integration*. After the recording of the DALS image has finished, both pictures need to be superimposed by pressing the button *SuperImpose* in the recording menu. As an analysis will consist of several alternations of the available settings to work out great detail of a possible DALS spot the following approach can be used:

- Resolution
  The described settings are located in the menu tab *Reso* on the middle in the left hand side of the software.
  - Start off with the *Normal* scan mode and a low resolution of 512x512 px. This settings are sufficient to record possible defect spots in a short time as the amount of pixels can be reduced. Superimpose the DALS image to the pattern image. In normal scan mode, the pattern image and the DALS scan image must always have the same resolution settings, otherwise the pattern data cannot be superimposed to the pattern image.
  - If a defect spot has been found the scan area can be reduced significantly. Change the scan mode to *Area* and a proper resolution to include the recorded failures. Hint: Record the pattern image at a high resolution in the scan mode *Normal*. Then switch the scan mode to *Area* and activate the option *The display of a picture* below the *Reso* menu. The displayed yellow rectangle marks the area where the laser will be scanning across the DUT. It can easily be moved via a drag and drop mouse click.
  - Finish the analysis by choosing the highest resolution either in *Normal* or *Area* scan mode.
- Lens
  The settings for the lens can be accessed in the *Stage* menu tab.
  - The best use lenses for DALS analysis are $5xNIR$, $20xNIR$ and $51xOBIRCH$ in ascending order.
  - Use the $5xNIR$ lens to work out basic detail. If a failure can be stimulated it must be observable with this lens as it offers the highest transmission rate of all used lenses.
  - If a spot has been found, the scan area can be reduced by changing the lens to $20xNIR$ or $51xOBIRCH$. Take care if the lens is changed to $51xOBIRCH$ as the working distance of this lens is dramatically lower and might cause a collision with the DUT which can cause severe damage. Using lenses with higher magnifications will lead to an increase of detail of the analysis.
  - The marked DALS spots will be dependent on the used lenses. Each lens is calibrated and aligned to the laser scanner. As it has been shown, there might exist a small offset from one lens to another.
  - In this software version it is not possible to superimpose images which have been recorded with different lenses.

- Laser Magnification
  The described settings are located in the menu tab *Reso* on the middle in the left hand side of the software.
  - The laser magnification should be used to work out greater detail at the end of the analysis.
  - Increasing laser magnification reduces the step width from one pixel to another. Therefore more detailed data can be collected about an area of interest.
  - This option will not increase the optical resolution, it will only improve the data quality.
  - A DALS image recorded with laser magnification can be superimposed to a pattern image.
- Laser Power
  - The laser power can be adjusted seamlessly from $0 \ldots 100\,\%$. The available power on the DUT is dependent on the used lens like it is shown in table 4.2.
  - Most failures will occur for laser powers of $P = 100\,\%$.
  - Weak soft defects might be stimulated only in a small stimulation range. Therefore a second measurement at lower laser power is recommended.
- Scan Direction
  The described settings are located in the menu tab *Reso* on the middle in the left hand side of the software.
  - It is recommended to use only the *Normal* scan direction.
  - As defect stimulation is dependent on the scan direction the device has to be rotated physically. It is recommended to record at least pictures for a rotation of $\alpha = 0\,^\circ$ and $\alpha = 90\,^\circ$. Two recorded DALS images of different scan directions can be superimposed to the pattern image at the same time by pressing the *Triple* menu button in the recording menu. To use this function both recorded DALS images have to be placed in the right hand image boxes in the SemiShop software.
  - As most of the signal lines are anyway placed either horizontally or vertically on the integrated circuit, fast evaluation results can be gained by rotating the DUT against $\alpha = 45\,^\circ$ to the thought x and y coordinate system.

  - Alternating the scan directions per software to 180 °, 90 ° or 270 ° can lead to wrong evaluation results, as there has been an offset of the laser scanning unit reported.

- Functional Test Parameters
  - Start off the analysis by using the static parameters found in the preparation of the DALS analysis.
  - If a defect has been found, try to alternate the point of operation to see whether the defect is dependent on external operating conditions.
  - Creating a Shmoo plot can reduce the analysis time significantly.

As it has been shown the DALS analysis mainly depends on the 6 noted settings above. If DALS spots have been identified the next step is the interpretation of the possible defect locations. Make sure that each measurement step is well documented. There are several possibilities that no spot could have been detected.

- Check all DALS signals from the functional tester to the LSM with an oscilloscope.
- Make sure the right software settings have been applied.
- Check if the pixel trigger is working properly by recording a pattern image with external synchronization. Also a standard function generator can be used to create the move pixel clock.
- Test the functionality of the Phemos system by measuring the OBIRCH reference sample in the *OBIRCH* operation mode. Even if this is another operation mode, the function of the laser scan unit can be proven. The expected failure spot of the OBIRCH reference sample can be seen in figure 5.2 in the lower left hand picture.
- If the synchronization does not work or no spot in the OBRICH analysis can be found, restart the Phemos system and carry out the above mentioned steps once more.
- Furthermore it is possible that the laser power is not sufficient to stimulate the pass/fail transition.

5.4 Interpretation

The interpretation starts off with a precise notation of the dimensions and location of the DALS spot on the integrated circuit. With the *ruler tool* it is possible to measure directly in the superimposed image in the *SemiShop* software. If no scale is given for the used lens, the best approach is to search for a unique structure nearby the located spot which can be afterwards identified easily in the layout editor. Then the dimension of the observed spot can be compared to the known dimensions of the chosen reference structure. After the DALS spot has been identified as a cell in the layout editor the in-, and outputs of the stimulated cell must be highlighted. Furthermore the failing patterns during the laser stimulation indicate which scan cells have been failing. By highlighting the in-, and outputs of these conspicuous cells, the best result would be an electrical connection between the cell stimulated and identified by DALS and the failing cell of the scan pattern or if it is the same cell. Possible questions which can improve the interpretation are:

- Do the DALS spots show any correlation to the cells identified by the scan pattern?
- If the analysis has revealed several cells, are they anyhow linked to each other?
- Does the failure occur in multiple devices at the same location, or is it a single failing device?
- If a reference design has been used, does the failure occur in other device models too?
- Is the pass/fail evaluation additionally dependent on an operating parameter? And if yes, would it affect the circuit logic in a simulation?
- Are the DALS spots depending on scan directions? Is the evaluation consistent?
- What are the spots denoting anyhow?
- Which functional part of the device has been stimulated?
- Are there probe pads or other connections available to continue the identification with signal probing?
- Is it possible to edit the circuit with a FIB to change its behavior?
- Is it possible to simulate the recorded failures in the circuit editor?

5.5 Confirmation

There exist several ways of how to confirm a defect in a device. The following list should give an idea about the necessary steps

- Make sure that the test setup is working fully functional and does not show any abnormalities. Verify it with a passing device.
- Simulate the failure with the same settings used to create the pass/fail transition.
- Measure the failure directly on a probe pad or another already available test point.
- Optically inspect the DUT at the marked DALS spot.
- Before starting any physical analysis methods, conduct the analysis with alternative possible measurement techniques. The behavior of the device might be alternated due to physical preparation.
- Deprocess the DUT layer by layer and optically inspect the device.
- Alternatively carry out a SEM analysis or FIB cross section.
- Try to alternate the behavior of a passing device with the FIB in order to get the same result as the failing devices.
- Place additional probe pads on the device which can give access to suspicious signal lines.

The analyzed examples in the previous chapter have clearly shown the importance of schematic analysis for the identified DALS spots. The marked spots by DALS analysis must not necessarily directly point out the failure location, as the laser stimulation might just alternate a clock signal which leads furthermore a failing signal in a subsequent cell.

5.6 Analysis Flowchart

The analysis flow chart which is presented in figure 5.3 and 5.4 is also available as an HTML file with detailed informations and step by step instructions as it has been presented in the previous chapters.

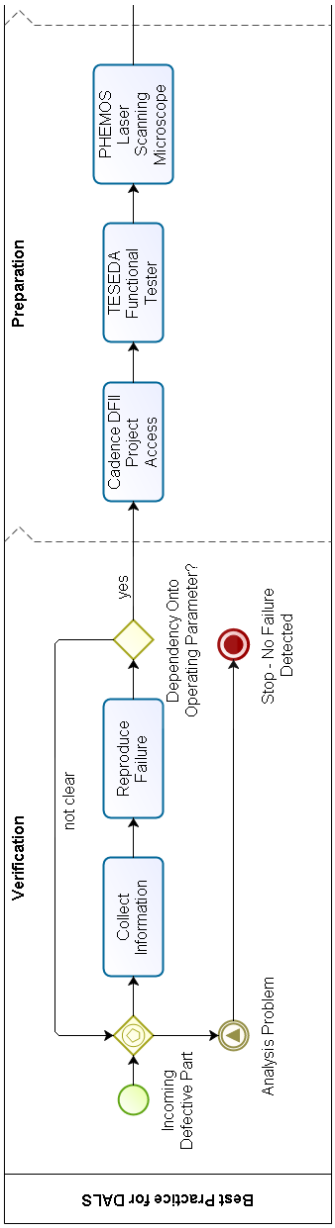

Figure 5.3: Best Practice for DALS - Analysis Flow Detail 1

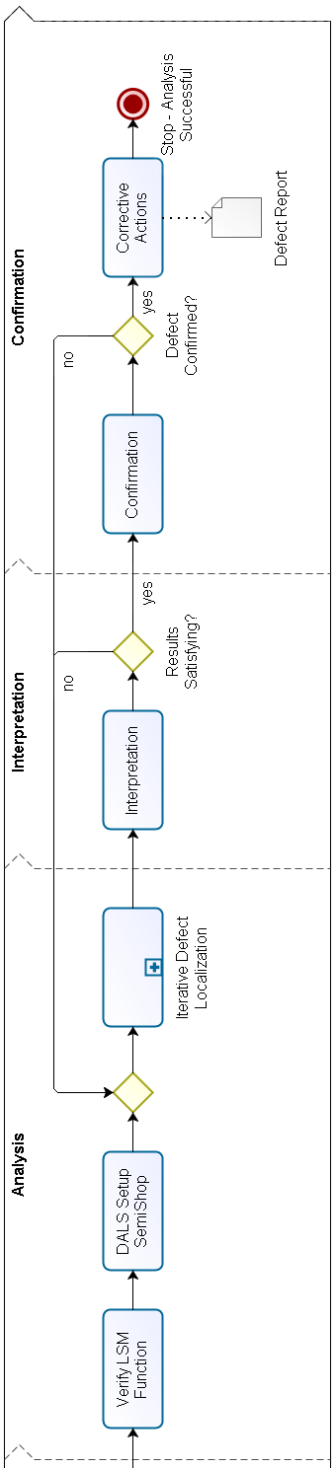

Figure 5.4: Best Practice for DALS - Analysis Flow Detail 2

6 Further Work

The main focus is to introduce failure analysts into the use of the laser scanning microscope and the functional tester to get evaluation results with DALS on soft defects. It is a clear goal, that DALS will become a regular to use failure analysis technique during lab investigations. As it has been shown one of the main drawbacks of the used system for the experiments is the limited laser power and the missing interpretation of GDS files within the LSM software itself. Furthermore it would be neat to gain the ability of cooling the devices with the thermochuck installed in the Phemos chamber and also to carry out photoelectric stimulation with a laser of a wavelength around $\lambda = 1064\,nm$ or lower. From a technical point of view the limited optical resolution could be overcome by installing for instance a SIL lens or other more sophisticated lenses with an increased magnification and numerical aperture. During the investigations on other DUT's the instructions and therefore best practice operations will be further improved as more and more failure analysts will work with this technique. If it turns out that the written instructions are not sufficient for a best practice guidance, a small video tutorial with an example could be recorded. Additionally the test vehicles could be analyzed with a pulsed laser source, as the presented experiments have only been analyzed with a continuous wave laser and related research has shown, that weak soft defects are easier to detect with high time resolution DALS analysis. As it has been presented in section 3.3.2, the possibilities of defect interpretations by creating device models with neuronal networks and parameter identification will be furthermore discussed. The actual results from the proposed identification methods unfortunately lack in data quality from the device stimulation. For this reason a new test setup will be created to collect suitable data.

Appendix

Glossary

AC	Alternating Current.
ADC	Analog to Digital Converter.
ATE	Automatic or Automated Test Equipment.
ATPG	Automatic Test Pattern Generation.
BBDL	Beam Based Defect Localization.
CCD	Charge Coupled Device.
CMOS	Complementary Metal Oxide Semiconductor.
DALS	Dynamic Analysis by Laser Stimulation.
DC	Direct Current.
DUT	Device Under Test.
ESD	Electro Static Discharge.
FEM	Finite Element Method.
FIB	Focused Ion Beam.
GDS	Graphic Database System.
HTML	Hyper Text Markup Language.
IC	Integrated Circuit.
IR	Infra Red.
LSM	Laser Scanning Microscope.
MOS	Metal Oxide Semiconductor.
PCB	Printed Circuit Board.

SEM	Scanning Electron Microscopy.
SIL	Solid Immersion Lens.
SLM	Scribe Line Monitor.

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